1 Features

- 8-Channel, Configurable ADC/DAC/GPIO
- 8 12-bit DAC Channels
- 8 12-bit ADC Channels
- 8 General-Purpose I/O Pins
- Integrated Temperature Sensor
- 16-Lead MIS 3x3 and 16-ball WLCSP 2x2 Package
- I^2C Interface

2 Applications

- General-Purpose Analog and Digital I/O
- Multi Channels Control and Monitor

3 Description

The TPAFE0808 has eight input/output pins, which can be configured to be ADC input, DAC output, or General-purpose I/O pins.

A 12-bit ADC is integrated into TPAFE0808, which can be connected to each input/output pin by an eight-channel multiplexer. The ADC input range is 0~VREF or 0~2*VREF.

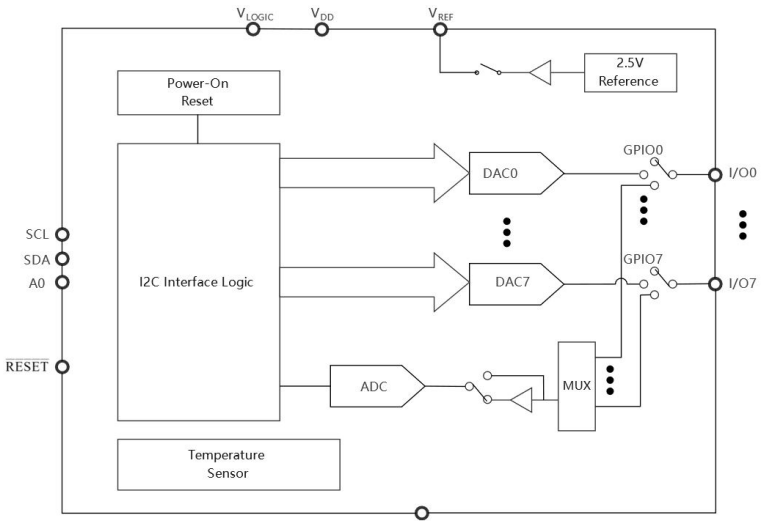
TPAFE0808 has an eight-channel 12-bit DAC, which can be connected to the corresponding input/output pin. The DAC output range is 0~VREF or 0~2*VREF.

TPAFE0808 has an internal 2.5-V reference, and it can also use external reference when the internal reference is turned off.

It also has an internal temperature sensor that can measure die temperature.

The TPAFE0808 is available in 16-lead MIS 3x3, as well as a 16-ball WLCSP, and operates over a temperature range of −40°C to +125°C.

4 Functional Block Diagram



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5 Product Family Table

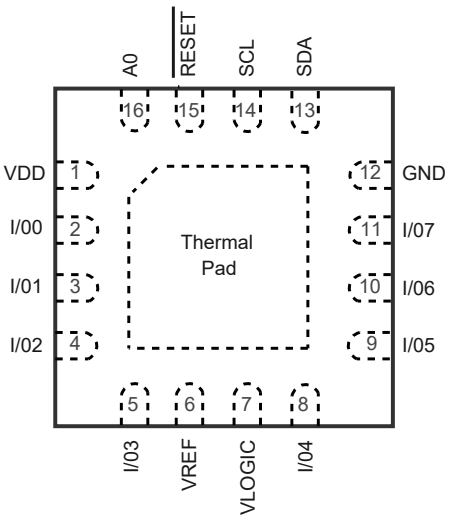
Order Number	VDAC Channel	IDAC Channel	ADC Channel	Package
TPAFEA008-WLPR	4	4	4	WLCSP

6 Revision History

Date	Revision	Notes
2020-08-02	Rev.A.1	1.0 Version
2020-09-11	Rev.A.2	Refined parameters, and updated register definition details
2021-01-19	Rev.A.3	Updated serial interface diagram
2021-05-20	Rev.A.4	Updated Product description and diagram
2021-07-22	Rev.A.5	Updated t3 tLOW Max limit
2022-07-28	Rev.A.6	Updated tape and reel information
2024-04-08	Rev.A.7	Updated MIS package POD
2024-12-03	Rev.A.8	Updated to a new datasheet format Updated the Package Outline Dimensions.

7 Pin Configuration and Functions

TPAFE0808
QFN3X3-16 Package
Top View



TPAFE0808
WLCSP Package
Top View

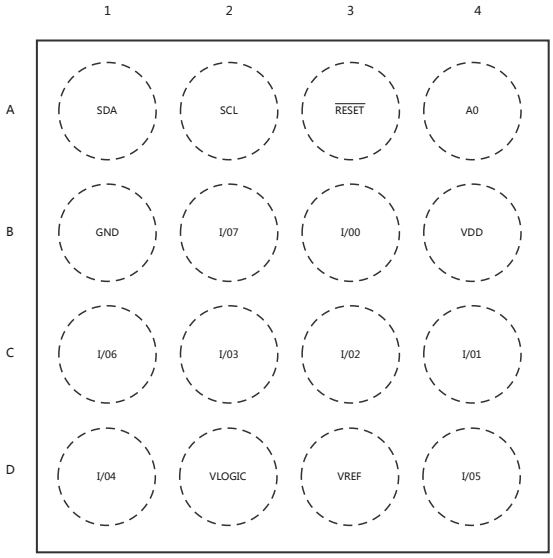


Table 1. Pin Functions: TPAFEA008

Pin No.		Pin Name	I/O	Description
MIS3X3-16L	WLCSP 2x2-16L			
1	B4	VDD	P	Power Supply Input.
8 to 11 2 to 5,	B3, C4, C3, C2, D1, D4, C1, B2	I/O0 to I/O7	I/O	Input/Output pin. These pins can be configured as DACs, ADCs, or GPIO independently.
6	D3	VREF	I	Reference Input/Output. When the internal reference is enabled, the 2.5 V voltage is available on the pin. When the internal reference is disabled, an external reference should be used and connected to the pin.
7	D2	VLOGIC	P	Digital interface Power Supply.
12	B1	GND	GND	Ground.
13	A1	SDA	I/O	Serial Data Line. This pin is open drain input/output.
14	A2	SCL	I	Serial Clock Line. This pin is open drain input.
15	A3	/RESET	I	Reset Pin. Low effective. When this pin is tied low, the chip is reset to the default condition.
16	A4	A0	I	Address pin. It can be connected to GND or VLOGIC. It sets LSB of the I^2C address.

8 Specifications

8.1 Absolute Maximum Ratings (1)

Parameter	Min	Max	Unit
VDD to GND	−0.3	7	V
VLOGIC to GND	−0.3	7	V
Analog Input Voltage to GND	−0.3	VDD + 0.3	V
Digital Input Voltage to GND	−0.3	VLOGIC + 0.3	V
Digital Output Voltage to GND	−0.3	VLOGIC + 0.3	V
VREF to GND	−0.3	VDD + 0.3	V
Operating Temperature Range	−40	125	°C
Storage Temperature Range	−65	150	°C
Junction Temperature (T_J max)		150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

8.2 ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	6	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
MIS3X3-16L	100.1	37.4	°C/W
WLCSP 2x2-16L	70	28.6	°C/W

8.4 Electrical Characteristics

All test conditions: V_{DD} = 2.7 V to 5.5 V, V_{REF} = 2.5 V (internal), T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Parameter	Test Conditions	Min	Typ	Max	Unit
ADC DC Specifications (1)					
Resolution		12			bit
Full-scale Input Range		0		2xVREF	V
		0		VREF	V
INL				±2	LSB
DNL				±1	LSB
Offset Error				±5	mV
Offset Error Temperature Drift			10		uV/°C
Gain Error				±0.3	%FSR
Gain Error Temperature Drift			±20		ppm/°C
Conversion Time			2		us
Acquisition Time	500 K SPS conversion rate	500			ns
Signal-Noise Ratio			60		dB
Total Harmonic Distortion			80		dB
SFDR			80		dB
Channel-to-Channel Isolation			-70		dB
Full Power Bandwidth			8		MHz
Input Buffer Dead Band	from 0 or VCC		20	40	mV
DAC DC Specifications (1)					
Resolution		12			bit
Full-Scale Output Voltage Range	power up or reset through auto-range detection	0		5	V
INL				±3	LSB
DNL				±1	LSB
Offset Error	End point fit between codes 16 to 4031. DAC outputs unloaded.		±2	±15	mv
Offset Error Temperature Drift	Mid-scale output		8		uV/°C
Gain Error	full temp		±0.1	±0.5	%FSR
Gain Error Temperature Drift			±20		ppm/°C
Zero-Scale Error	Code=000h full temp		4	10	mv
Zero-scale Error Temperature Drift			±2		uV/°C
Load Current 1	sink or source Middle code, drop out=2 mV,	10			mA
Load Current 2	sink or source VDD=3.45 V, drop out=0.45 V,	11			mA

8.5 Electrical Characteristics (continued)

All test conditions: V_{DD} = 2.7 V to 5.5 V, V_{REF} = 2.5 V (internal), T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Parameter	Test conditions	Min	Typ	Max	Unit
Short Circuit Current	Normal mode(default)		25		mA
Capacitive Load Stability	RL = ∞			1	nf
Output Voltage Settling Time	RL = 2 kΩ, Cl = 200 pf 1/4 to 3/4 scale settling to ±0.5 LSB.		10		μs
Slew Rate	Transition: 1/4 to 3/4 scale, 10% to 90%. RL = 2 kΩ, Cl = 200 pf		0.5		V/μs
Output Noise	0.1 Hz to 10 Hz, DAC code at mid-scale		200		μVpp
Output Noise Density	10 kHz, DAC code at mid-scale		700		nV/√Hz
DAC Enable Overshoot			50		mV
DAC Enable Time			100		uS
DAC Glitch			20		nV*S
Temperature Sensor					
Accuracy			±3		°C
Update Time			45		ms
Reference Voltage					
Internal Reference Voltage		2.49	2.5	2.51	V
Internal Reference Temperature Coefficient			20		ppm/°C
Capacitive Load Stability		0.1		1	uF
Load Regulation	No load ability		NA		
GPIO					
Voh	ISOURCE = 1 mA	VDD − 0.2			V
Vol	Isink = 1 mA			0.4	V
Vih		VDD*0.7			V
Vil				VDD*0.3	V
Hysteresis			0.2		V
Logic Input					
Vih		VLOGIC* 0.7			V
Vil				VLOGIC* 0.3	V
Logic Output					
Output High Voltage, VOH	VDD = 2.7 V to 5.5 V ISOURCE = 200 μA;	VLOGIC − 0.2			V
Output Low Voltage, VOL	ISINK = 200 μA			0.4	V

8.6 Electrical Characteristics (continued)

VDD = 2.7 V to 5.5 V, VREF = 2.5 V (internal), $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted., unless otherwise noted.

Parameter	Test Conditions	Min	Typ	Max	Unit
Power	internal reference @500 kHz VCC = 3 V, ADC enabled,		2.15	3.5	mA
	external reference @500 kHz VCC = 3 V, ADC enabled,		1.85	3	mA
	VCC = 3 V, DAC enabled		2.9	4.5	mA
	VCC = 3 V， ADC + DAC + Bg		4.5	7	mA
	VCC = 3 V， ADC + DAC + Bg + temperature sensor		5	7.5	mA
T_{ready}	Ready Time after Hardware Reset		1	2	ms

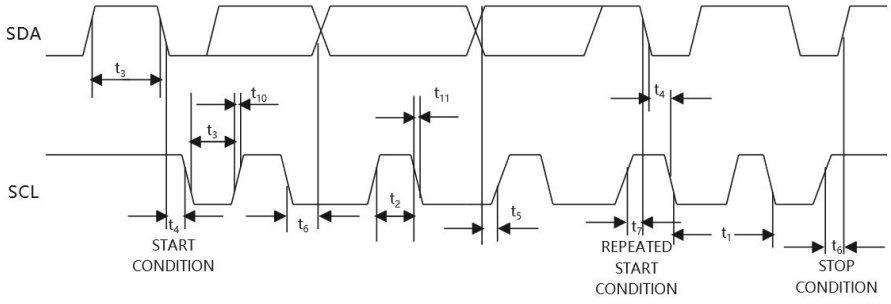
8.7 Timing Characteristics (1)

All test conditions: V_{DD} = 2.7 V to 5.5 V, V_{REF} = 2.5 V (internal), T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Parameter	Conditions/Comments	Min	Typ	Max	Unit
tscl	SCL cycle time	2.5			μs
t_2 t_{HIGH}	SCL high time	0.6			μs
t_3 t_{LOW}	SCL low time	1.3		13000	μs
t_4 $t_{HD,STA}$ (2)	start and restart condition hold time	0.6			μs
t_5 $t_{SU,DAT}$	data setup time	100			ns
t_6 $t_{HD,DAT}$	data hold time			0.9	μs
t_7 $t_{SU,STA}$	setup time for repeated start	0.6			μs
t_8 $t_{SU,STO}$	stop condition setup time	0.6			μs
t_9 t_{BUF}	bus free time between stop and start	1.3			μs
t_{10} t_R	Data and clock rise time			300	ns
t_{11} t_F	Data and clock fall time			250	ns

(1) Specified by design and characterization.
(2) If the hold time is < 10 nS, a start condition may be recognized.

8.8 Timing Diagrams



8.9 Typical Performance Characteristics

All test conditions: VDD = 2.7 V to 5.5 V, VREF = 2.5 V (internal), $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

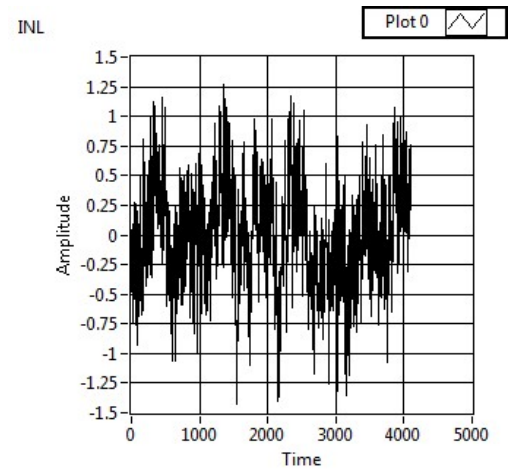


Figure 1. ADC INL

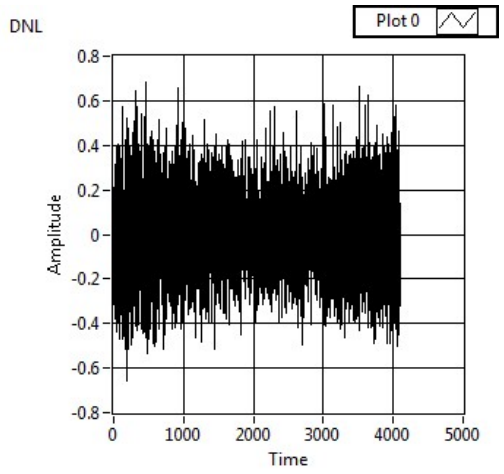


Figure 2. ADC DNL

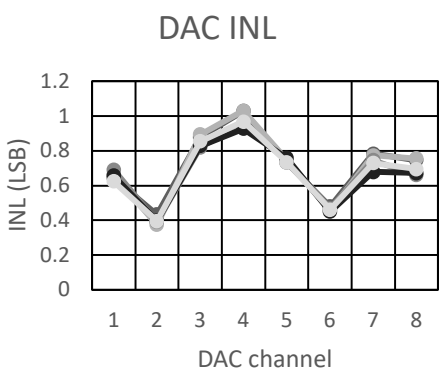


Figure 3. DAC INL

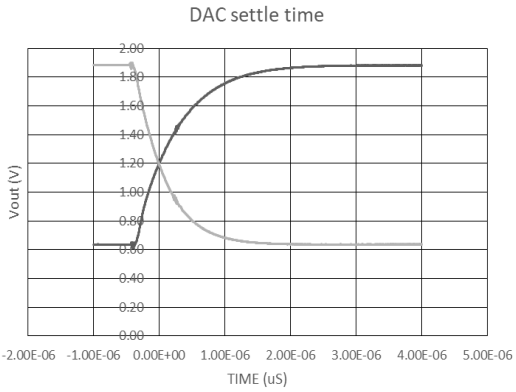


Figure 4. DAC Settling Time, Output Range = 0~Vref

9 Detailed Description

9.1 Overview

The TPAFE0808 has eight input/output pins, which can be configured to be ADC input, DAC output, or General-purpose I/O pins.

A 12-bit ADC is integrated into TPAFE0808, which can be connected to each input/output pin by an eight-channel multiplexer. The ADC input range is 0~VREF or 0~2*VREF.

TPAFE0808 has an eight-channel 12-bit DAC, which can be connected to the corresponding input/output pin. The DAC output range is 0~VREF or 0~2*VREF.

TPAFE0808 has an internal 2.5-V reference, and it can also use external reference when the internal reference is turned off.

9.2 Register Maps

Table 2. Pointer Byte Configuration

D7	D6	D5	D4	D3	D2	D1	D0
Mode bits				Mode-dependent data bits			

Table 3. Mode Bits

D7	D6	D5	D4	Description
0	0	0	0	Configuration mode
0	0	0	1	DAC write
0	1	0	0	ADC readback
0	1	0	1	DAC readback
0	1	1	0	GPIO readback
0	1	1	1	Register readback

Table 4. Configuration Register Table

Pointer Byte	R/W	Default Value	Register Name	Description
8'h00	R/W	16'h0000	NO	No operation is available
8'h02	R/W	16'h0000	ADC sequence	Selects ADC sequence
8'h03	R/W	16'h0000	ADC DAC general configuration	ADC and DAC configuration
8'h04	R/W	16'h0000	ADC selection	Selects ADC channels
8'h05	R/W	16'h0000	DAC selection	Selects DAC channels
8'h06	R/W	16'h00ff	Pull down selection	Selects which pins have 85 kΩ pull-down resistor
8'h07	R/W	16'h0000	LDAC control	Selects load DAC operation
8'h08	R/W	16'h0000	GPIO write selection	Selects general purpose outputs

Pointer Byte	R/W	Default Value	Register Name	Description
8'h09	R/W	16'h0000	GPIO write data	Writes data to general-purpose outputs
8'h0a	R/W	16'h0000	GPIO read selection	Selects general purpose inputs
8'h0b	R/W	16'h0000	Power down control	Powers down control of the ADC, DAC, and reference
8'h0c	R/W	16'h0000	Open drain configuration	open drain or push-pull control for general-purpose outputs
8'h0d	R/W	16'h0000	Three state selection	Select three stated output
8'h0f	R/W	16'h0000	Software reset	Resets the chip
8'h7e	R	16'h0808	Chip ID	Chip ID for readback

9.3 Register Explanations

Table 5. ADC Sequence

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Reserved						REP	TEMP	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0

Table 6. ADC Sequence Descriptions

Bits	Description
D15 to D10	Reserved, set to 0.
D9	REP: sequence repeat 0 = disable repetition (default) 1 = enable repetition
D8	Temperature selection 0 = disable temperature read back 1 = enable temperature read back
D7 to D0	1 = includes corresponding ADC in conversion sequence 0 (default) = not selected in the conversion sequence

Table 7. ADC DAC General Configuration

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Reserved						Pre-charge	ADC Buffer	GPIO Lock	DAC write all	ADC range	DAC range	Reserved			

Table 8. ADC DAC General Configuration Descriptions

Bits	Description
D15 to D10	Reserved. Set these bits to 0.
D9	Precharge. 0: No ADC precharge function(default). The ADC buffer is always powered up if it is enabled. 1: ADC buffer is used to precharge the sampling cap and then powered down until the next conversion.
D8	ADC buffer 0: the ADC buffer is disabled (default). 1: the ADC buffer is enabled.
D7	GPIO Lock 0: the IO selection registers can be changed (default). 1: the IO selection registers cannot be changed.
D6	DAC write all 0: DAC value is written to DAC channels according to DAC address bits. 1: all DACs channels are updated with the same data.
D5	ADC range. 0: 0 to VREF (default). 1: 0 to 2 × VREF.
D4	DAC range. 0: 0 to VREF (default). 1: 0 to 2 × VREF.
D3 to D0	Reserved;

Table 9. LDAC Control

D1	D0	Description
0	0	Data written to the input register is copied into the DAC register, and the DAC output is also updated (default).
0	1	Data written to an input register is not copied to the DAC register, and the DAC output is also not updated.
1	0	Data in the input registers are copied to the DAC registers, and the DAC outputs are updated simultaneously. The LDAC control bits return to 01 after the operation is done.
1	1	Reserved.

Table 10. DAC Pointer Byte Address

DAC Address	D7	D6	D5	D4	D3	D2	D1	D0
DAC0	0	0	0	1	0	0	0	0
DAC1	0	0	0	1	0	0	0	1
DAC2	0	0	0	1	0	0	1	0

DAC Address	D7	D6	D5	D4	D3	D2	D1	D0
DAC3	0	0	0	1	0	0	1	1
DAC4	0	0	0	1	0	1	0	0
DAC5	0	0	0	1	0	1	0	1
DAC6	0	0	0	1	0	1	1	0
DAC7	0	0	0	1	0	1	1	1

Table 11. DAC Data

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	DAC address			12-bit DAC data											

Table 12. ADC Data

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	ADC address			12-bit ADC data											

Table 13. GPIO Write Selection

Bits	Description
D15 to D8	Reserved;
D7 to D0	GPIO output selection 1: set to be output pin 0: determined by pin selection registers (default)

Table 14. Open-Drain Configuration

Bits	Description
D15 to D8	Reserved
D7 to D0	GPIO output Open-drain selection 1: open-drain output 0: push/pull output (default)

Table 15. GPIO Write Data

Bits	Description
D15 to D8	Reserved
D7 to D0	1: Set GPIO output to 1. 0: Set GPIO output to 0

Table 16. Three-State Selection

Bits	Description
D15 to D8	Reserved
D7 to D0	Set pins as three-state outputs 1: set GPIO to three-state output 0: determined by pin selection registers (default)

Table 17. Pull-Down Selection

Bits	Description
D15 to D8	Reserved
D7 to D0	Set pins as weak pull-down outputs 1: pulled down by 85 kΩ pull-down resistor 0: determined by pin selection registers (default)

Table 18. Power-Down Register

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	PD_ALL	EN_REF	0	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

Table 19. LDAC Mode Register Descriptions

Bits	Bit Name	Description
D15 to D11	Reserved	Reserved
D10	PD_ALL	0 = Determined by D0~D9 (default). 1 = all analog blocks are powered down.(REF, ADC, DAC)
D9	EN_REF	0 = Internal Reference is powered down (default). 1 = Internal reference is powered up and available on the VREF pin.
D7 to D0	PD7 to PD0	0 = the channel is in operating mode (default). 1 = the channel is powered down if it is selected as DAC.

9.4 Feature Description

The TPAFE0808 has eight input/output pins, which can be configured to be ADC input, DAC output, or General purpose I/O pins.

DAC Section

TPAFE0808 has eight channel 12-bit DACs, which can be connected to the corresponding input/output pin. Each channel has a resistor-string DAC with an output buffer. Following is the DAC diagram:

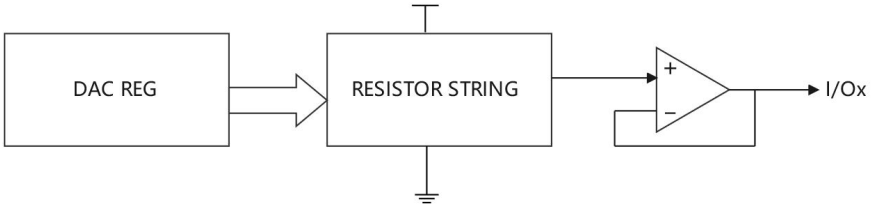


Figure 5. DAC Architecture

The DAC range is 0 V to VREF or 0 V to 2 × VREF, controlled by the DAC Range bit.

The output voltage is:

$$V_{OUT} = V_{REF} \times \frac{D}{2^{12}} \text{ or } V_{OUT} = 2 \times V_{REF} \times \frac{D}{2^{12}}$$

Where *VREF* is the 2.5 V internal reference or external reference voltage,

D is the DAC register value.

ADC Section

TPAFE0808 has a 12-bit ADC, which can be connected to each I/O pin by a multiplexer. The conversion time is 2 μs. The ADC can scan selected channels automatically by setting the selection register.

ADC input range is 0 V to VREF or 0 V to 2 × VREF, controlled by the ADC range bit. All input channels share the same range.

The input/output pin can be set to be both ADC and DAC. In this case, the DAC output voltage can be monitored by ADC.

The following figure shows the ADC input structure:

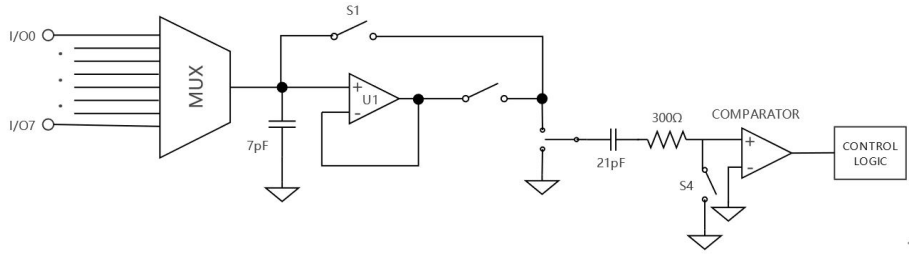


Figure 6. ADC Input Structure

The current flowing into the ADC input pins varies with the sampling rate and differential voltage. It can be calculated as follows:

$$f_s \times C \times V_{DIFF} \quad (1)$$

where: *fS* is the ADC sample rate.

C is the sampling capacitance (7 pf in buffer mode, 7+21=28 pf in un-buffered mode)

VDIFF is the voltage difference between successive channels.

For example:

f_S = 10 kHz, previous ADC input is 0.5 V, and current ADC input is 2 V, the ADC input current in unbuffered mode is as follows:

$$\left(10000 \times 28 \times 10^{-12} \times 1.5\right) = 420 \text{ nA} \quad (2)$$

GPIO Section

By controlling the GPIO selection register, each of the eight input/output pins can be configured as a digital input or output pin. general-purpose digital input or output pin by programming the GPIO control register. Logic levels for general-purpose outputs are relative to VDD and GND.

Internal Reference

The TPAFE0808 has an internal 2.5 V reference. The reference is powered down by default. When the reference is powered down, an external reference must be connected to VREF.

When the internal reference is powered up, it appears on the VREF pin , but can not be used as a reference source for other components. When the internal reference is used, it is recommended to not decouple between VREF to GND, or use a capacitor >=100 nf.

Reset Function

The TPAFE0808 has two reset functions, hardware reset by RESET pin and software reset by writing to specific register 0x0F.

A falling edge on RESET resets all registers to default values, and input/output pins are set to status with 85 kΩ pull-down resistor to GND. The reset function takes 250 μs maximum; do not write new data to the TPAFE0808 during this time.

The TPAFE0808 has a software reset function, by writing 0x0F to the pointer byte and 0x0D and 0xAC to MSB and LSB. The software reset function performs the same as the RESET pin.

Temperature Indicator

The TPAFE0808 contains an integrated temperature to monitor the die temperature. The temperature can be calculated as follows:

$$\text{Temp} = \frac{\text{ADC Code} - 1024}{16} \tag{3}$$

The range of codes returned by the ADC when reading from the temperature indicator is approximately 384 to 3024.

Serial Interface

The TPAFE0808 has a 2-wire, I^2C-compatible serial interface. It supports standard mode (100 kHz) and fast mode (400 kHz). The six MSBs of the 7-bit slave address is 001000, and the LSB is set by the state of the A0 pin.

The 2-wire serial bus protocol operates as follows:

I^2C Write

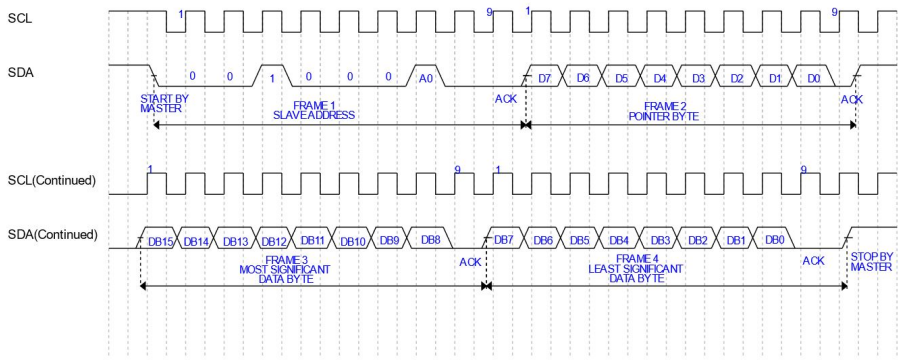


Figure 7. I2C Write

I^2C Read

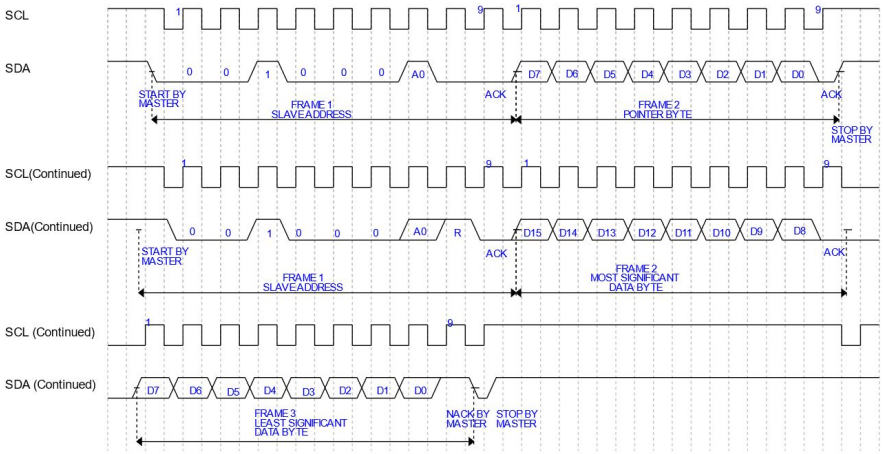


Figure 8. Read One 16-bit Word

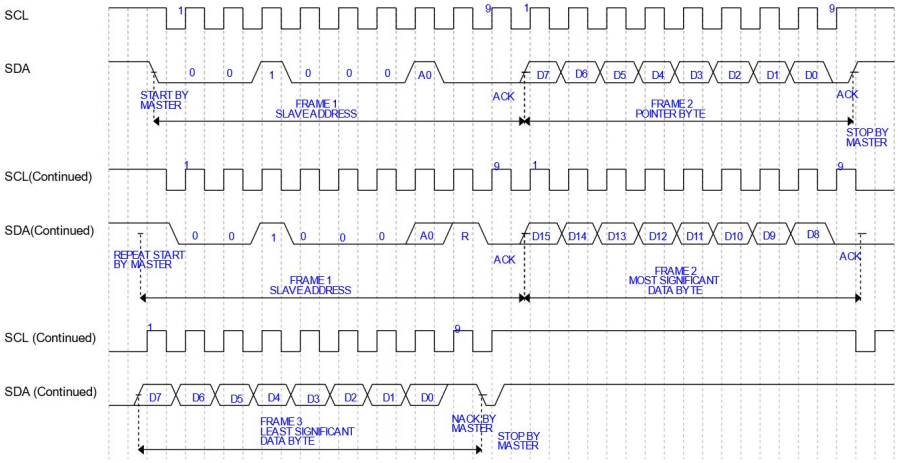


Figure 9. Read One 16-bit Word, Maintain Control of the Bus

I^2C Block Read

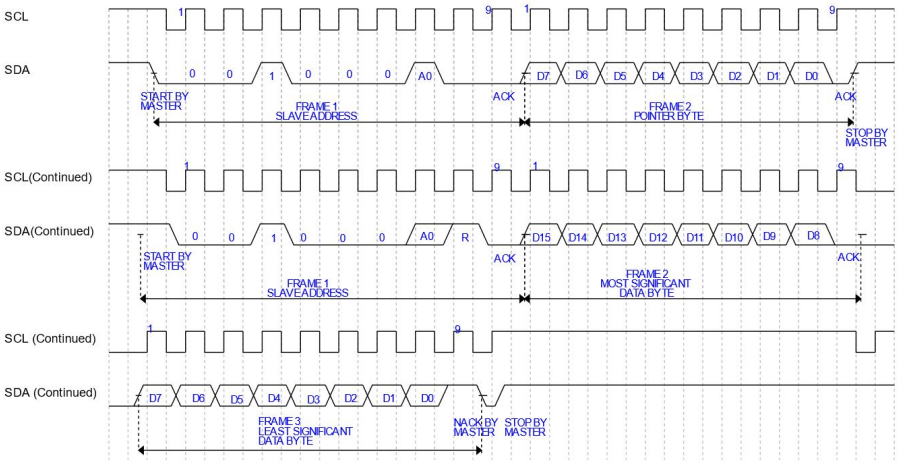


Figure 10. I^2C Block Read

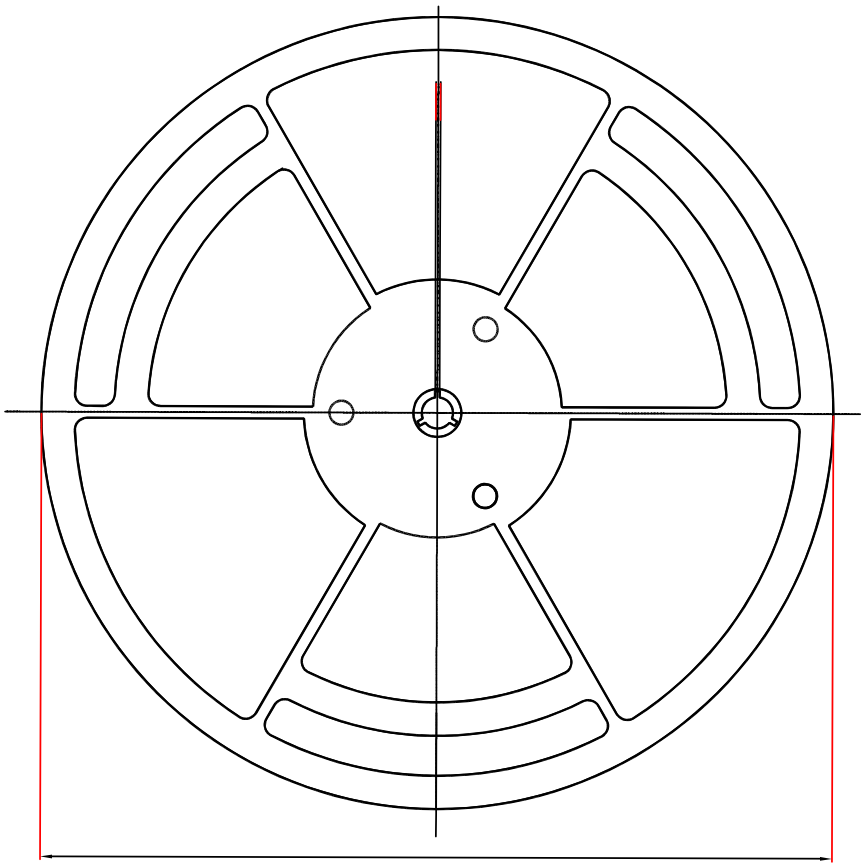
10 Application and Implementation

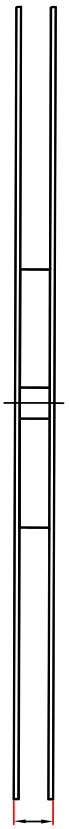
> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

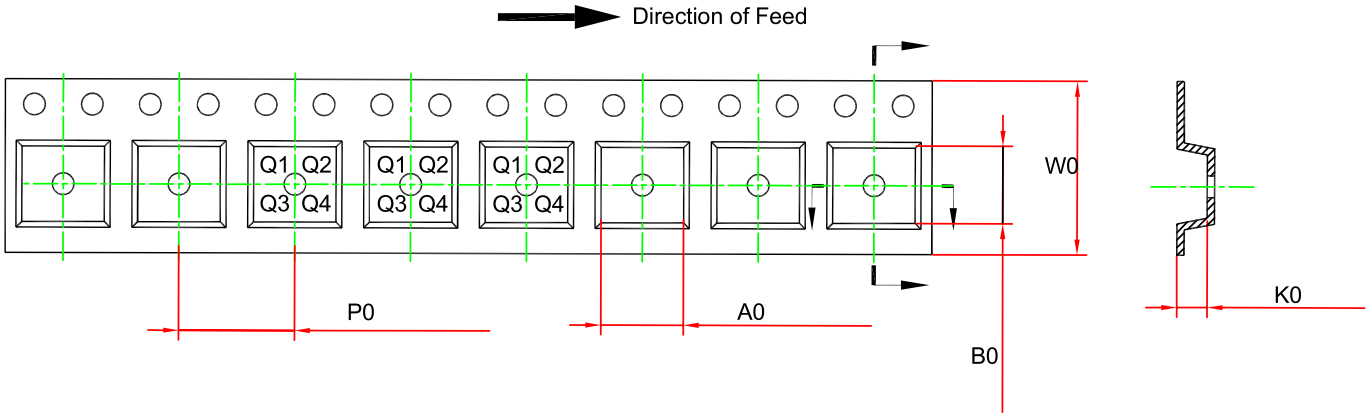
10.1 Application Information

1. When internal reference is used, at least 100 nf capacitors should be added as a filter cap. Resistive loading should not be connected to the reference pin.
2. If one input/output pin is used as a DAC function, don't toggle it between DAC mode and GPIO mode.
3. No special power-up sequence is required.

11 Tape and Reel Information





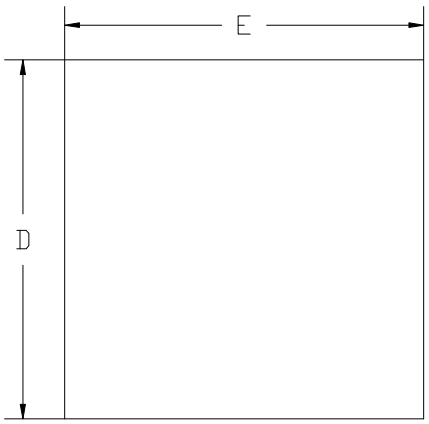


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPAFEA008-WLPR	WLCSP	178	12.5	2.24	2.24	0.75	4	8	Q2
TPAFE0808-LFPR-S	MIS3X3-16L	330	17.6	3.3	3.3	1	8	12	Q2

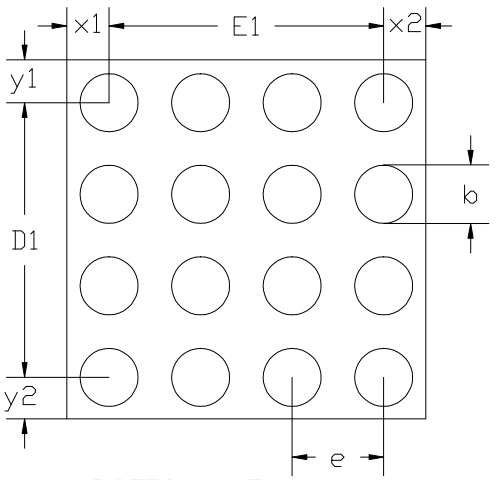
12 Package Outline Dimensions

12.1 WLCSP

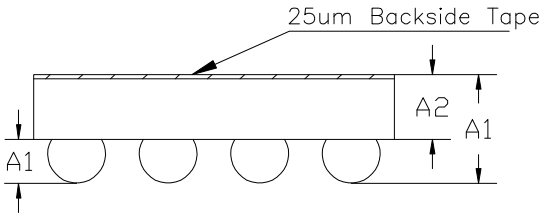
Package Outline Dimensions WLP(WLCSP-A)



TOP VIEW
(MARK SIDE)



BOTTOM VIEW
(BALL SIDE)



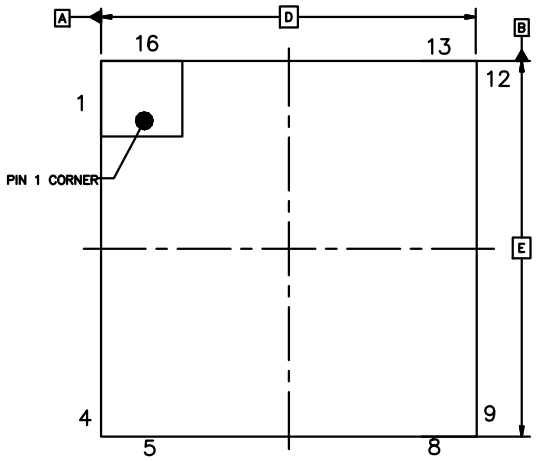
SIDE VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.550	0.640	0.022	0.025
A1	0.220	0.260	0.009	0.010
A2	0.330	0.380	0.013	0.015
D	1.930	1.990	0.076	0.078
E	1.930	1.990	0.076	0.078
D1	1.500 BSC		0.059 BSC	
E1	1.500 BSC		0.059 BSC	
b	0.300	0.340	0.012	0.013
e	0.500 BSC		0.020 BSC	
x1	0.22875 REF		0.009 REF	
x2	0.23125 REF		0.009 REF	
y1	0.2325 REF		0.009 REF	
y2	02275 REF		0.009 REF	

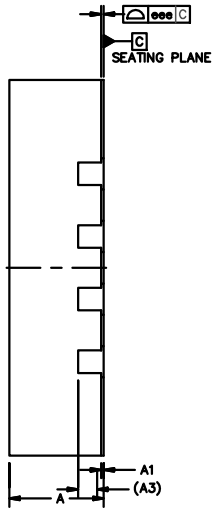
NOTES
1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

12.2 QFN3X3-16

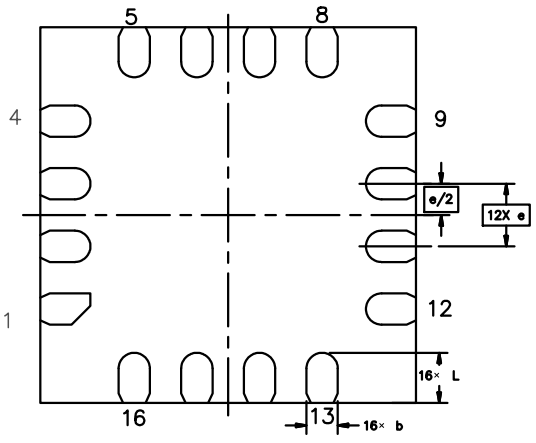
Package Outline Dimensions — QFN(QFN3X3-16-E)



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
b	0.200	0.300	0.008	0.012
A3	0.203 REF		0.008 REF	
D	3.000 BSC		0.118 REF	
E	3.000 BSC		0.118 REF	
e	0.500 BSC		0.020 BSC	
L	0.300	0.500	0.012	0.020

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

13 Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPAFE0808-LFPR-S	−40 to 125°C	MIS3X3-16L	0808	3	Tape and Reel, 4000	Green
TPAFE0808-WS2R	−40 to 125°C	WLCSP 2x2-16L	0808	1	Tape and Reel, 3000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

14 IMPORTANT NOTICE AND DISCLAIMER

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