PE42442

Document category: Product Specification

UltraCMOS® SP4T RF Switch, 30 MHz–6 GHz

Features

- Four symmetric, absorptive RF ports
- High isolation:
  - 61 dB @ 900 MHz
  - 55 dB @ 2100 MHz
  - 52 dB @ 2700 MHz
  - 43 dB @ 4000 MHz
  - 32 dB @ 6000 MHz
- High linearity:
  - IIP2 of 97 dBm
  - IIP3 of 58 dBm
- 1.8V control logic compatible
- Operating temperature range: -40 °C to 125 °C
- Fast switching time: 255 ns
- Two- or three-pin CMOS logic control
- External negative supply option
- ESD performance:
  - 4 kV HBM on RF pins to GND
  - 2 kV HBM on all pins
- Packaging: 24-lead 4 × 4 mm QFN

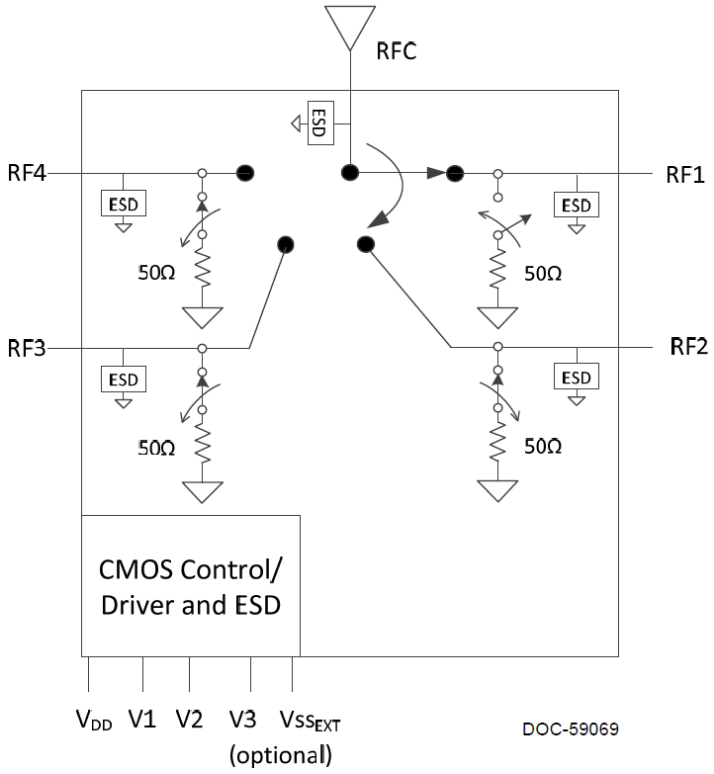

Figure 1. PE42442 functional diagram

Product description

The PE42442 is a HaRP™ technology-enhanced absorptive SP4T RF switch designed for use in 3G/4G wireless infrastructure and other high performance RF applications.

This switch is a pin-compatible four-throw version of the PE42451 with a wider frequency and power supply range. It consists of four symmetric RF ports with very high isolation up to 6 GHz. An integrated CMOS decoder facilitates a two- or three-pin 1.8V CMOS control interface. In addition, no external blocking capacitors are required if 0 VDC is present on the RF ports.

The PE42442 is manufactured on pSemi's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate.

pSemi's HaRP technology enhancements deliver high linearity and excellent harmonics performance. It is an innovative feature of the UltraCMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

Headquarters: 9369 Carroll Park Dr, San Diego, CA 92121

Absolute maximum ratings

Exceeding the absolute maximum ratings listed in Table 1 could cause permanent damage. Restrict operation to the limits in Table 2. Operation between the operating range maximum and the absolute maximum for extended periods could reduce reliability.

ESD precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, do not exceed the rating listed in Table 1.

Latch-up immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1. PE42442 absolute maximum ratings

Parameter or condition	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	-0.3	5.5	V
Voltage on any DC input	V_I	-0.3	3.6	V
Maximum input power at +105 °C	$P_{MAX,ABS}$	–	34	dBm
Maximum input power at +125 °C	$P_{MAX,ABS}$	–	28	dBm
Storage temperature range	T_{ST}	-65	+150	°C
ESD voltage HBM:(1) - All pins - RF pins to ground	$V_{ESD,HBM}$	–	 2000 4000	V
ESD voltage MM, all pins(2)	$V_{ESD,MM}$	–	150	V
ESD voltage CDM, all pins(3)	$V_{ESD,CDM}$	–	250	V

1. Human Body Model (MIL_STD 883 Method 3015).
2. Machine Model (JEDEC JESD22-A115).
3. Charged Device Model (JEDEC JESD22-C101D).

Recommended operating conditions

Table 2 lists the PE42442 recommended operating conditions. Do not operate devices outside the operating conditions listed below.

Table 2. PE42442 operating conditions

Parameter	Symbol	Min	Typ	Max	Unit
Normal mode(1)					
Supply voltage	V_{DD}	2.3	–	5.5	V
Supply current	I_{DD}	–	110	–	µA
Bypass mode(2)					
Supply voltage	V_{DD}	2.7	–	5.5	V
Supply current	I_{DD}	–	50	–	µA
Negative supply voltage	V_{SS_EXT}	-3.6	–	-3.2	V
Normal or bypass mode					
Digital input high, V1, V2, and V3	V_{IH}	1.17	–	3.6	V
Digital input low, V1, V2, and V3	V_{IL}	-0.3	–	0.6	V
Digital input current	I_{CTRL}	–	–	1	µA
RF input power, CW, at +105 °C	$P_{MAX,CW}$	–	–	33	dBm
RF input power, CW, at +125 °C	$P_{MAX,CW}$	–	–	28	dBm
RF input power into terminated ports, CW, at +105 °C	$P_{MAX,TERM}$	–	–	24	dBm
RF input power into terminated ports, CW, at +125 °C	$P_{MAX,TERM}$	–	–	20	dBm
Operating temperature range	T_{OP}	-40	–	+125	°C

1. Normal mode: To enable the internal negative voltage generator, connect V_{SS_EXT} (pin 20) to GND.
2. Bypass mode: To bypass and disable the internal negative voltage generator, apply a negative voltage to V_{SS_EXT} (pin 20).
3. The pull-down resistor in the EVK schematic (Figure 16) can increase the control current.

Electrical specifications

Table 3 lists the PE42442 key electrical specifications at +25 °C and V_{DD} = 5V (Z_S = Z_L = 50Ω), unless otherwise specified.

- Normal mode: V_{DD} = 3.3V, V_{SS_EXT} = 0V (single external positive supply used)
- Bypass mode: V_{DD} = 3.3V, V_{SS_EXT} = –3.3V (both an external positive supply and an external negative supply used)

Table 3. PE42442 electrical specifications at +25 °C

Parameter	Path	Condition	Min	Typ	Max	Unit
Operating frequency	–	–	30	–	6000	MHz
Insertion loss	RFC–RFx	450 MHz 900 MHz 2100 MHz 2700 MHz 4000 MHz 6000 MHz	–	0.85 0.90 1.10 1.15 1.25 1.90	1.00 1.05 1.35 1.40 1.50 2.35	dB
Isolation	RFC–RFx	450 MHz 900 MHz 2100 MHz 2700 MHz 4000 MHz 6000 MHz	62 55 52 50 42 27	67 61 55 52 43 32	–	dB
Isolation	RFx–RFx	450 MHz 900 MHz 2100 MHz 2700 MHz 4000 MHz 6000 MHz	61 56 51 50 41 29	65 61 54 52 44 32	–	dB
Return loss, active port	RFx	30–4000 MHz 4000–6000 MHz	–	17 12	–	dB
Return loss, terminated port	RFx	30–4000 MHz 4000–6000 MHz	–	22 19	–	dB
Input 0.1-dB compression point[1]	RFC–RFx	900 MHz	–	35	–	dBm
Input IP2	RFC–RFx	1900 MHz	–	97	–	dBm
Input IP3	RFC–RFx	1900 MHz	–	58	–	dBm
Switching time[2]	–	50% control to 90% or 10% RF	–	255	330	ns

1. The input 0.1-dB compression point is a linearity figure of merit. For the operating RF input power (50Ω), see Table 2.
2. The PE42442 has a maximum 25 kHz switching rate in normal mode (pin 20 = GND). A faster switching rate is available in bypass mode (pin 20 = V_{SS_EXT}). The rate at which the PE42442 can be switched is then limited to the switching time as specified above. The switching frequency describes the time duration between switching events. The switching time is the time duration between the point that the control signal reaches 50% of the final value and the point that the output signal reaches within 10% or 90% of its target value.

Table 4 lists the PE42442 key electrical specifications at +125 °C and V_{DD} = 5V (Z_S = Z_L = 50Ω), unless otherwise specified.

- Normal mode: V_{DD} = 3.3V, V_{SS_EXT} = 0V (single external positive supply used)
- Bypass mode: V_{DD} = 3.3V, V_{SS_EXT} = –3.3V (both an external positive supply and an external negative supply used)

Table 4. PE42442 electrical specifications at +125 °C

Parameter	Path	Condition	Min	Typ	Max	Unit
Operating frequency	–	–	30	–	6000	MHz
Insertion loss	RFC–RFx	450 MHz 900 MHz 2100 MHz 2700 MHz 4000 MHz 6000 MHz	–	1.11 1.18 1.43 1.50 1.59 2.28	1.38 1.45 1.79 1.95 2.04 2.91	dB
Isolation	RFC–RFx	450 MHz 900 MHz 2100 MHz 2700 MHz 4000 MHz 6000 MHz	56 54 49 46 33 23	66 60 55 52 43 32	–	dB
Isolation	RFx–RFx	450 MHz 900 MHz 2100 MHz 2700 MHz 4000 MHz 6000 MHz	59 54 50 49 39 26	65 61 53 52 43 32	–	dB
Return loss, active port	RFx	30–4000 MHz 4000–6000 MHz	–	16 13	–	dB
Return loss, terminated port	RFx	30–4000 MHz 4000–6000 MHz	–	17 15	–	dB
Input 0.1-dB compression point[1]	RFC–RFx	900 MHz	–	35	–	dBm
Input IP2	RFC–RFx	1900 MHz	–	91	–	dBm
Input IP3	RFC–RFx	1900 MHz	–	56	–	dBm
Switching time[2]	–	50% control to 90% or 10% RF	–	355	439	ns

1. The input 0.1-dB compression point is a linearity figure of merit. For the operating RF input power (50Ω), see Table 2.
2. The PE42442 has a maximum 25 kHz switching rate in normal mode (pin 20 = GND). A faster switching rate is available in bypass mode (pin 20 = V_{SS_EXT}). The rate at which the PE42442 can be switched is then limited to the switching time as specified above. The switching frequency describes the time duration between switching events. The switching time is the time duration between the point that the control signal reaches 50% of the final value and the point that the output signal reaches within 10% or 90% of its target value.

Spurious performance

The PE42442 typical spurious performance is –120 dBm (pin 20 = GND). If you prefer spurious-free performance, disable the internal negative voltage generator by applying a negative voltage to V_{SS_EXT} (pin 20).

Optional external V_{SS} control (V_{SS_EXT})

If your application requires a faster switching rate or spurious-free performance, you can operate this part in bypass mode. Bypass mode requires an external negative voltage in addition to an external V_{DD} supply voltage.

As listed in Table 2, applying the external negative voltage (V_{SS_EXT}) to pin 20 disables and bypasses the internal negative voltage generator.

SP4T control logic

Table 5. PE42442 truth table for 3-pin control

Mode	V3	V2	V1
RF1 on	0	0	1
RF2 on	0	1	0
RF3 on	0	1	1
RF4 on(1)	X	0	0
All off(2)	1	0	1
All off(2)	1	1	0
All off	1	1	1

1. X can be 0 or 1.
2. For legacy PE42450 and PE42451 products, only use logic states 101 or 110 for all off mode.

Table 6. PE42442 truth table for 2-pin control(1)(2)

Mode	V2	V1
RF1 on	0	1
RF2 on	1	0
RF3 on	1	1
RF4 on	0	0

1. V3 (Pin 19) must be grounded.
2. pSemi recommends 2-pin control for new product designs if all off mode is not required.

Typical performance data

Figure 2–Figure 14 show the typical performance data at +25 °C and V_{DD} = 3.3V, unless otherwise specified.

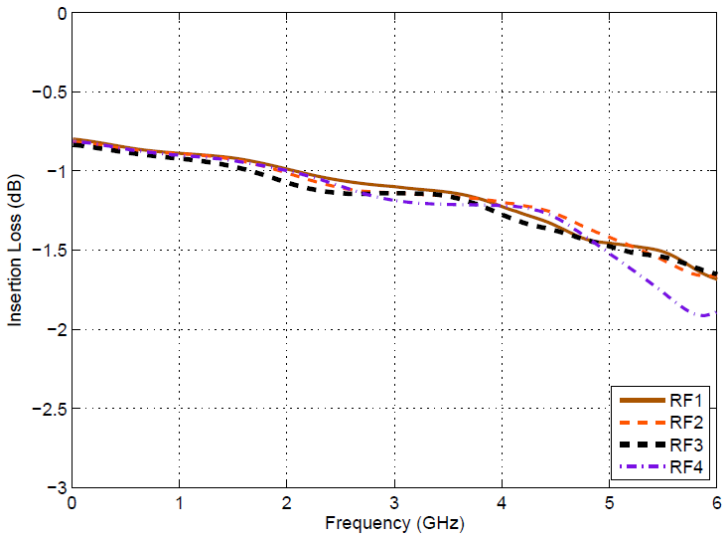

Figure 2. Insertion loss (all paths)

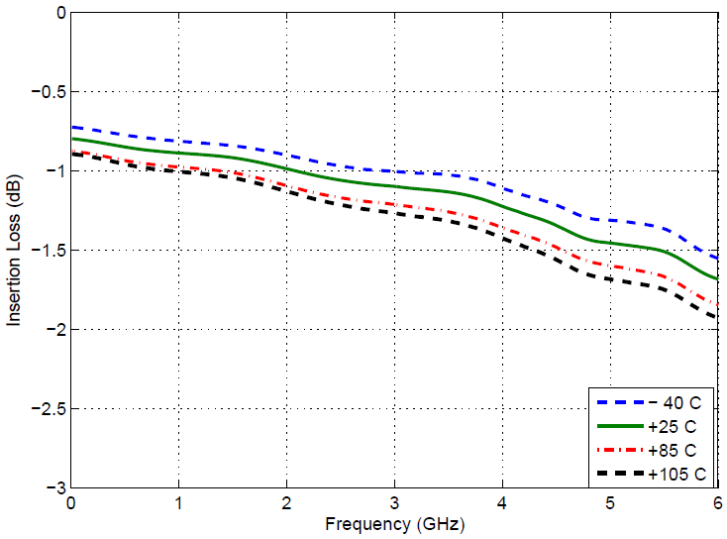

Figure 3. Insertion loss vs. temperature (RFC–RFx)

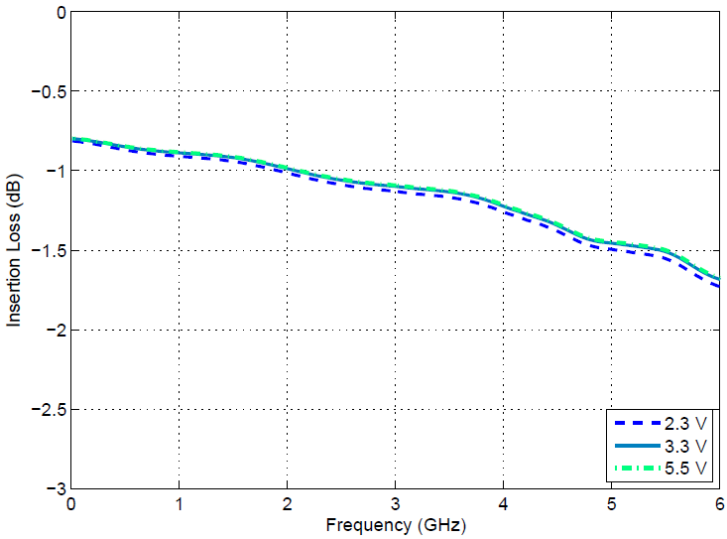

Figure 4. Insertion loss vs. V_{DD} (RFC–RFx)

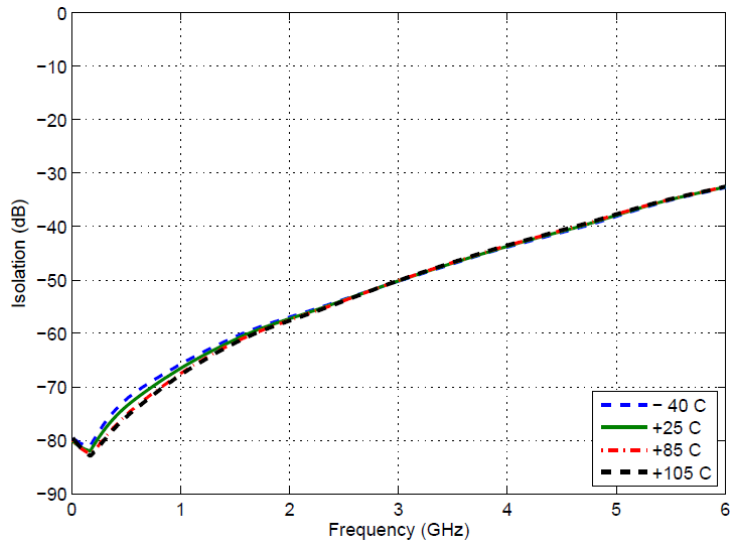

Figure 5. Isolation vs. temperature (RFC–RFx)

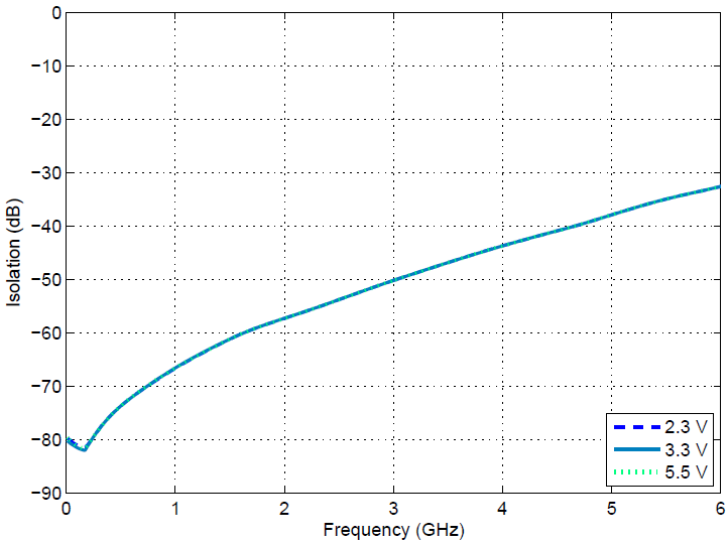

Figure 6. Isolation vs. V_{DD} (RFC–RFx)

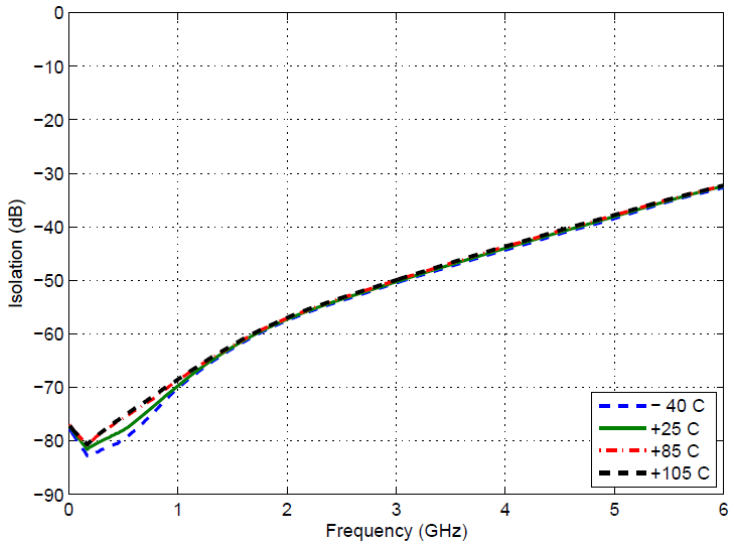

Figure 7. Isolation vs. temperature (RFx–RFx)

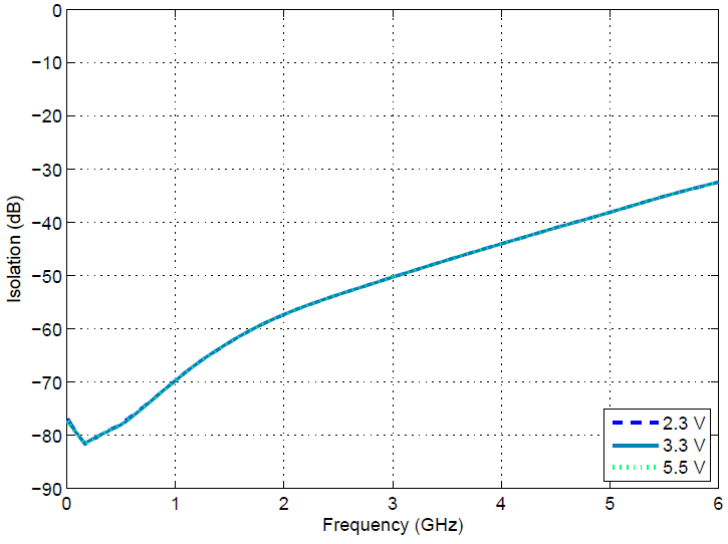

Figure 8. Isolation vs. V_{DD} (RFx–RFx)

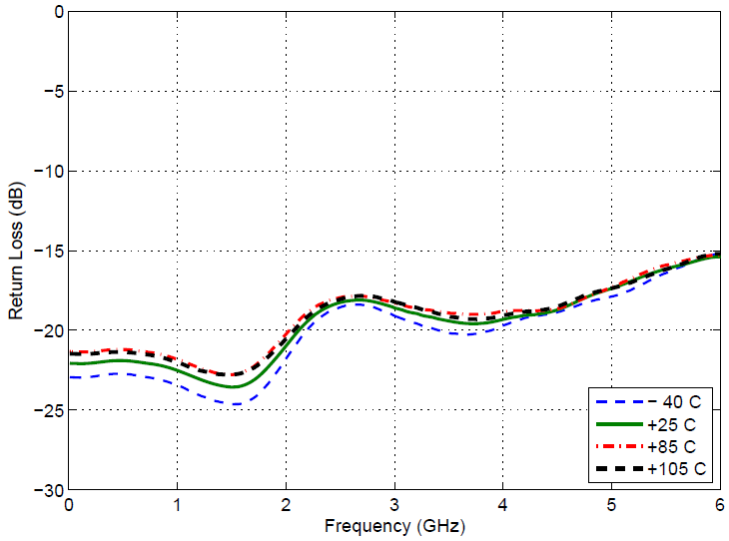

Figure 9. Active port return loss vs. temperature

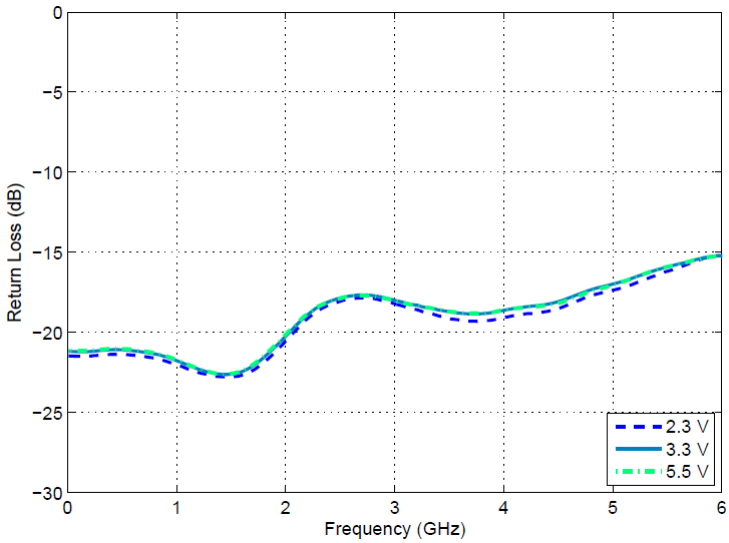

Figure 10. Active port return loss vs. V_{DD}

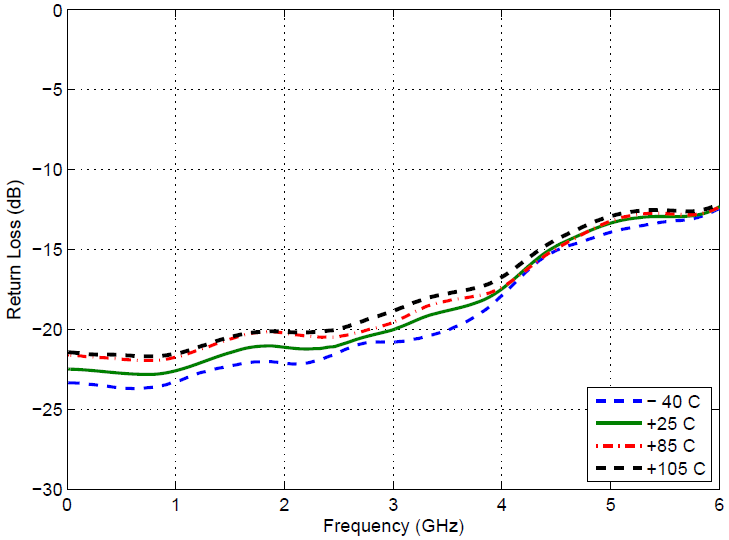

Figure 11. RFC port return loss vs. temperature

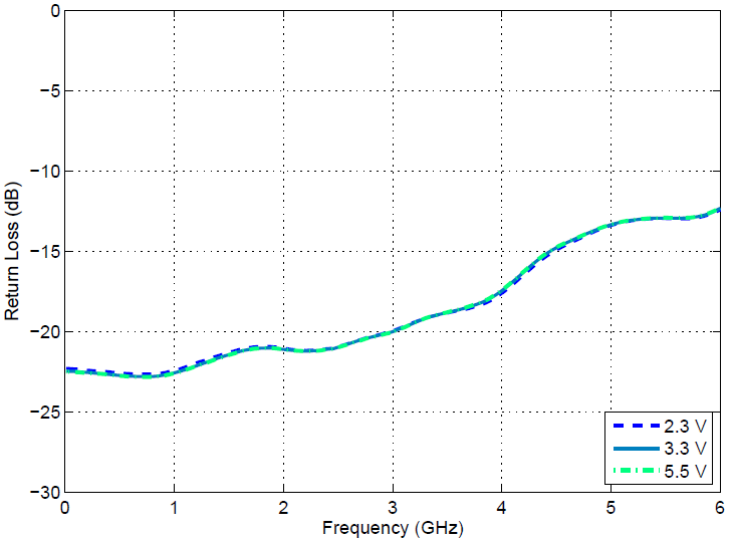

Figure 12. RFC port return loss vs. V_{DD}

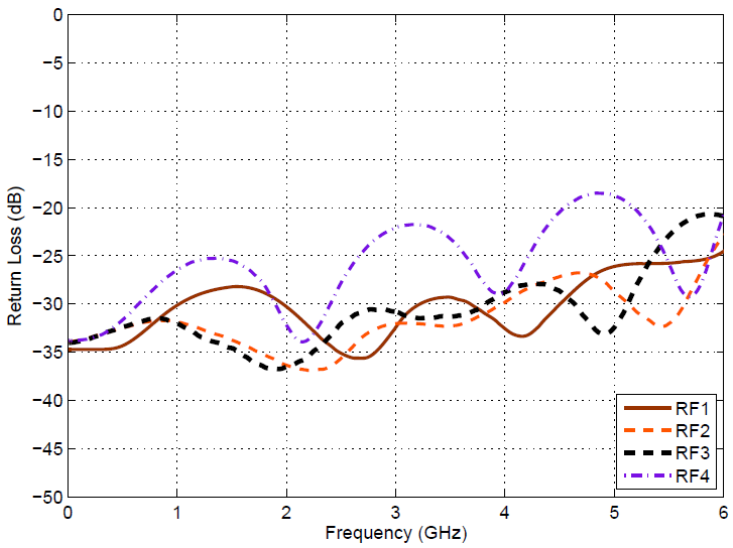

Figure 13. Return loss (all ports terminated)

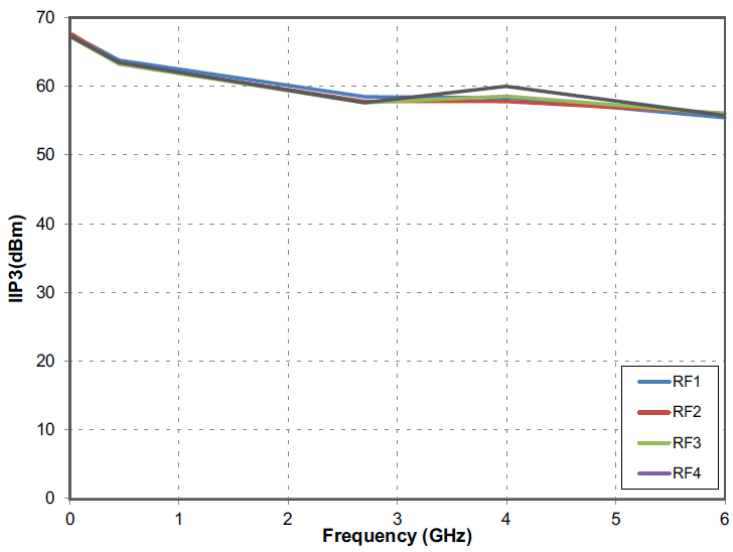

Figure 14. IIP3 vs. frequency

Evaluation kit

pSemi designed the SP4T switch evaluation board to ease your evaluation of the pSemi PE42442. The RF common port connects through a 50Ω transmission line via the top SMA connector. RF1, RF2, RF3, and RF4 connect through 50Ω transmission lines via side SMA connectors. A through 50Ω transmission is available via SMA connectors RFCAL1 and RFCAL2. Use this transmission line to estimate the loss of the PCB over the environmental conditions being evaluated.

The EVK board is constructed with four metal layers on dielectric materials of Rogers 4003C and 4450 with a total thickness of 32 mils. Layer 1 and layer 3 provide ground for the 50Ω transmission lines. The 50Ω transmission lines are designed in layer 2 for high isolation purposes and use a stripline waveguide design with a trace width of 9.4 mils and trace metal thickness of 1.8 mils. The board stack up for 50Ω transmission lines has 8 mil thickness of Rogers 4003C between layer 1 and layer 2, and 10 mil thickness of Rogers 4450 between layer 2 and layer 3.

For the proper board material properties in your application, consult the manufacturer's guidelines. Design the PCB so that the RF transmission lines and sensitive DC I/O traces—such as V_{SS_EXT}—are heavily isolated from each another, otherwise the PE42442 true performance might not be realized.

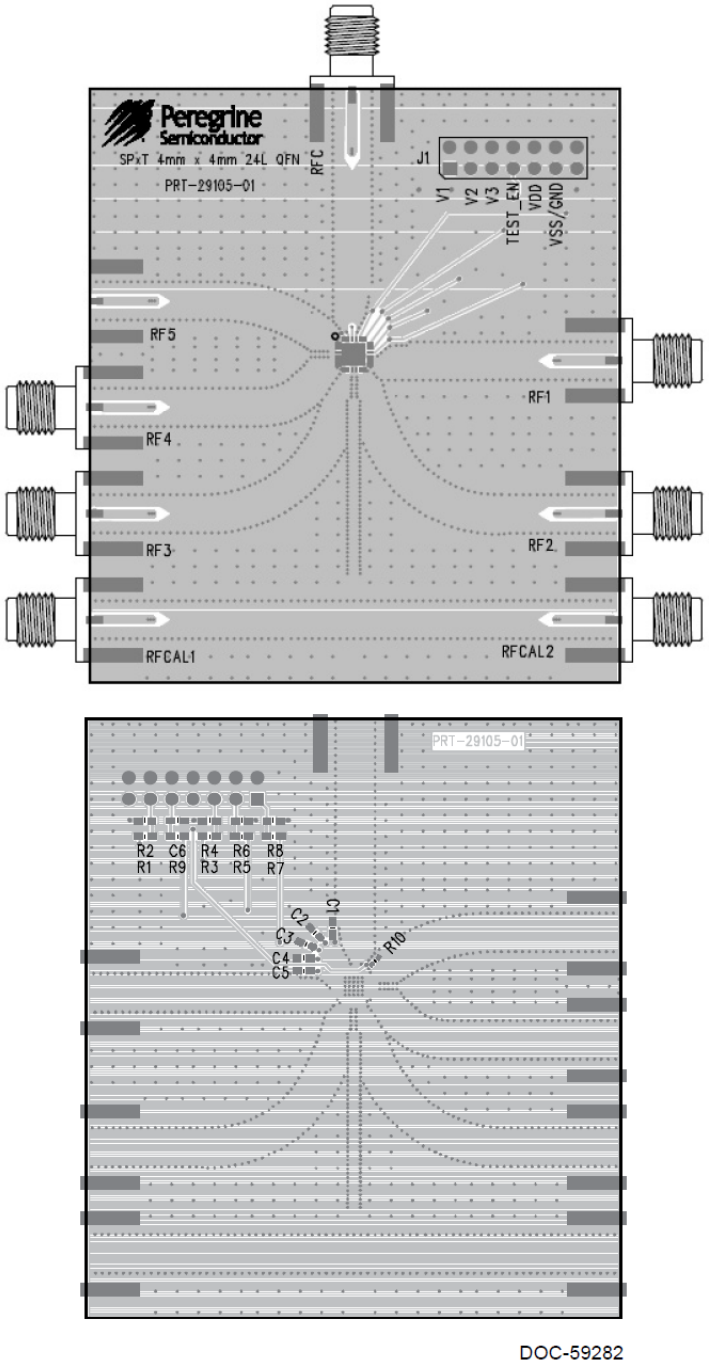

Figure 15. Evaluation board layout

Evaluation board schematic

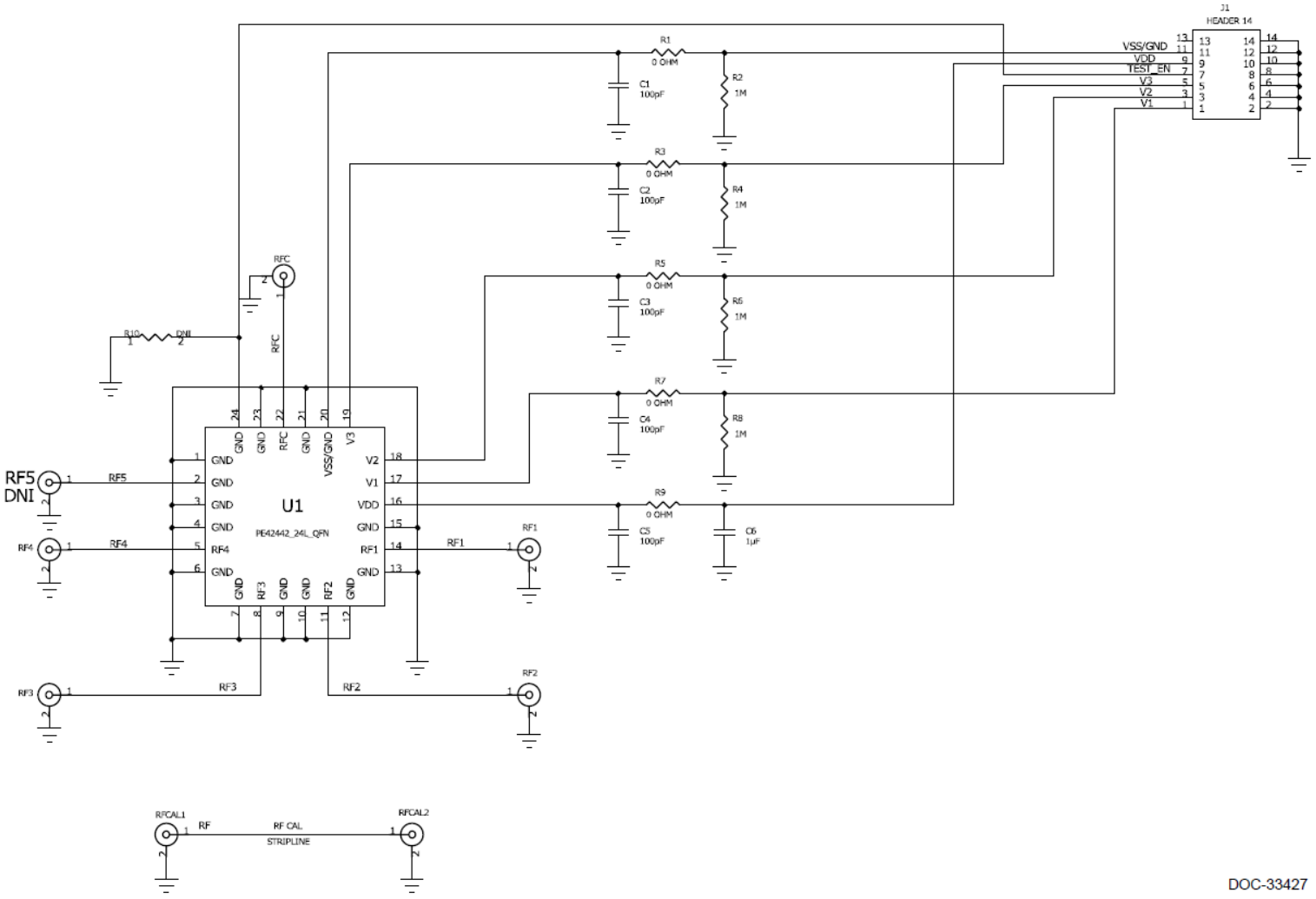

Figure 16. Evaluation board schematic

Pin information

Figure 17 shows the PE42442 pin map for the 24-lead 4 × 4 mm QFN package, and Table 7 lists the description for each pin.

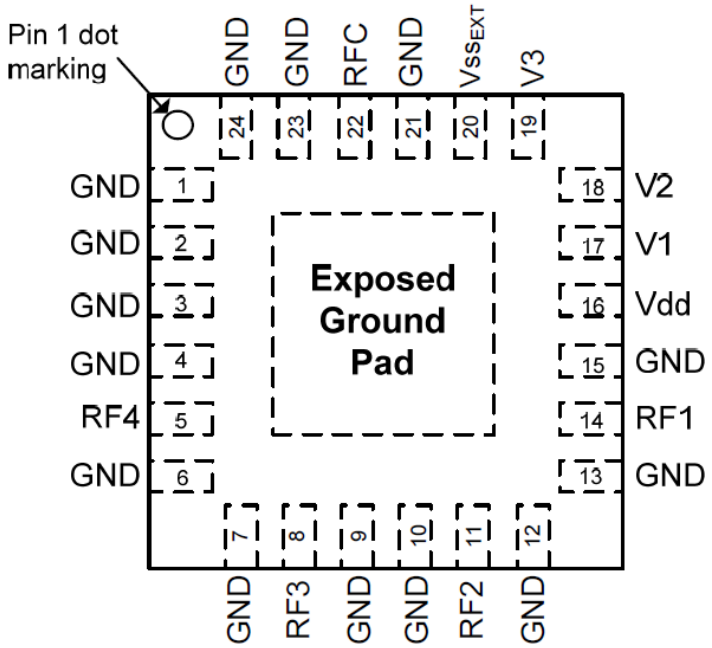

Figure 17. Pin configuration (top view)

Table 7. PE42442 pin descriptions

Pin no.	Pin name	Description
1–3, 4, 6, 7, 9, 10, 12, 13, 15, 21, 23, 24	GND	Ground
5[1]	RF4	RF port 4
8[1]	RF3	RF port 3
11[1]	RF2	RF port 2
14[1]	RF1	RF port 1
16	V_{DD}	Supply voltage
17	V1	Digital control logic input 1
18	V2	Digital control logic input 2
19[2]	V3	Digital control logic input 3
20[3]	V_{SS_EXT}	External V_{SS} negative voltage control or ground
22[1]	RFC	RF common
Pad	GND	Exposed pad. Ground for proper operation.

1. RF pins 5, 8, 11, 14, and 22 must be at 0 VDC. These RF pins do not require DC blocking capacitors for proper operation if the 0 VDC requirement is met.
2. For 2-pin control, ground V3 (Pin 19). See Table 6.
3. To bypass and disable the internal negative voltage generator, use V_{SS_EXT} (pin 20, see Table 2). To enable the internal negative voltage generator, connect V_{SS_EXT} (pin 20) to GND.

Packaging information

This section provides the following packaging data:

- Moisture sensitivity level
- Package drawing
- Package marking
- Tape-and-reel information

Moisture sensitivity level

The PE42442 moisture sensitivity level rating for the 24-lead 4 × 4 mm QFN package is MSL1.

Package drawing

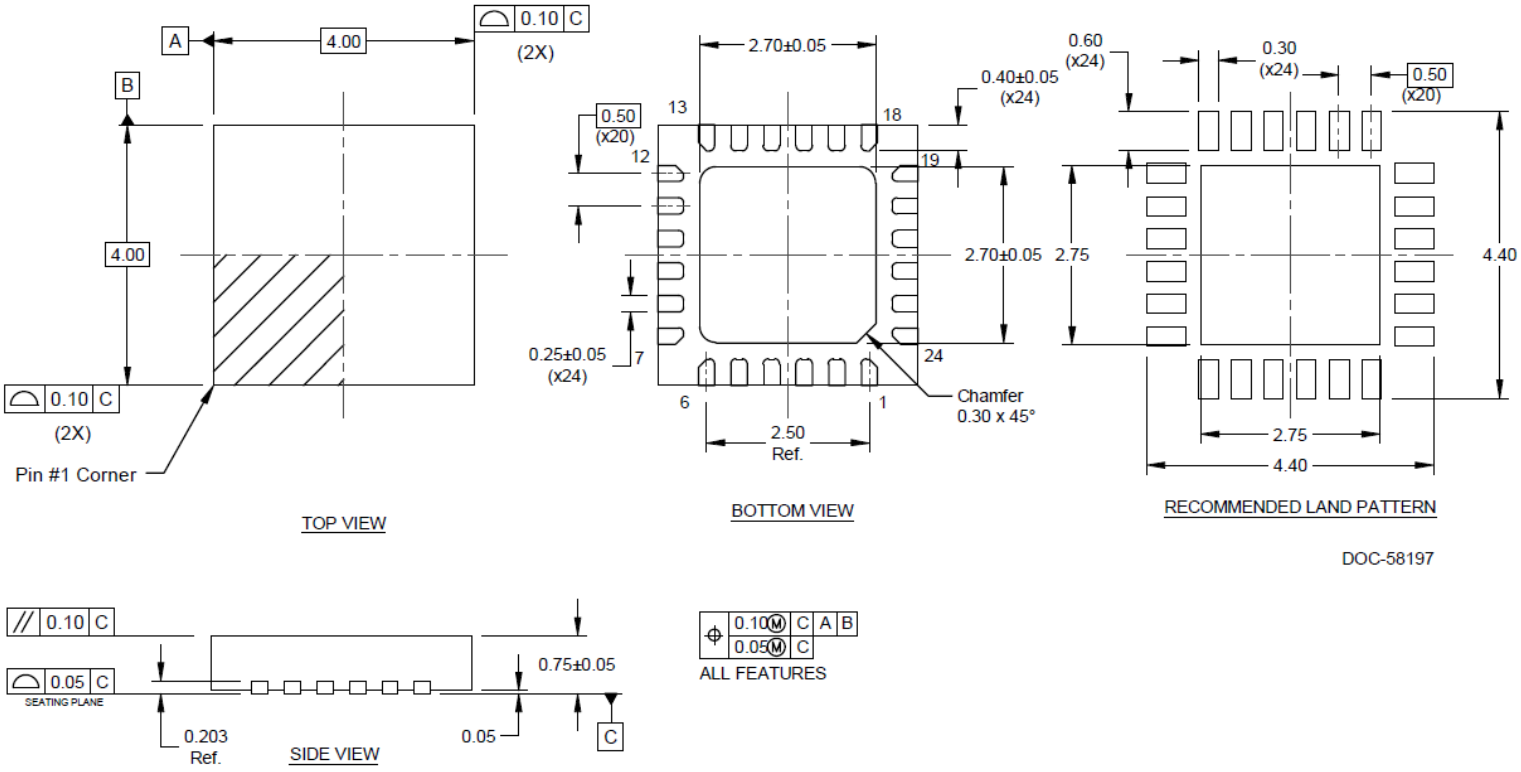

Figure 18. Package mechanical drawing for the 24-lead 4 × 4 mm QFN package

Top-marking specification

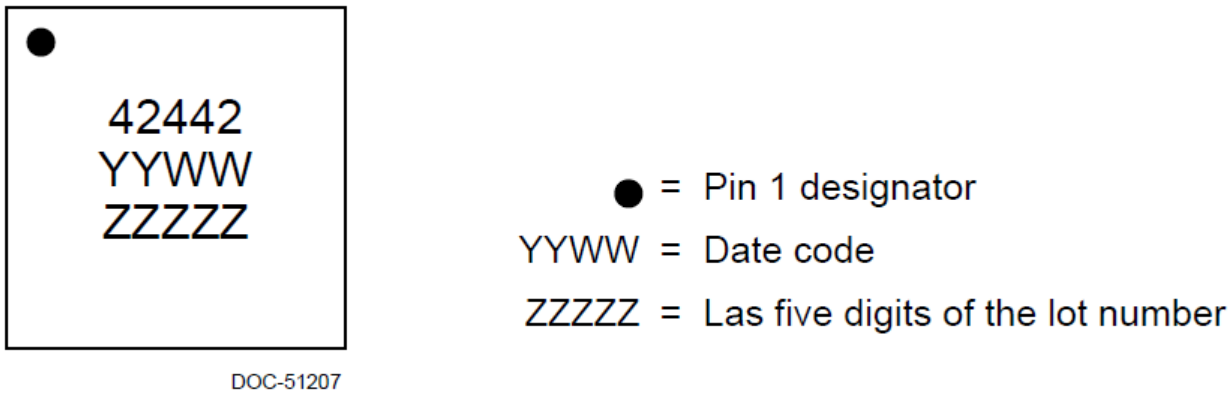

Figure 19. PE42442 package marking specification

Tape and reel specification

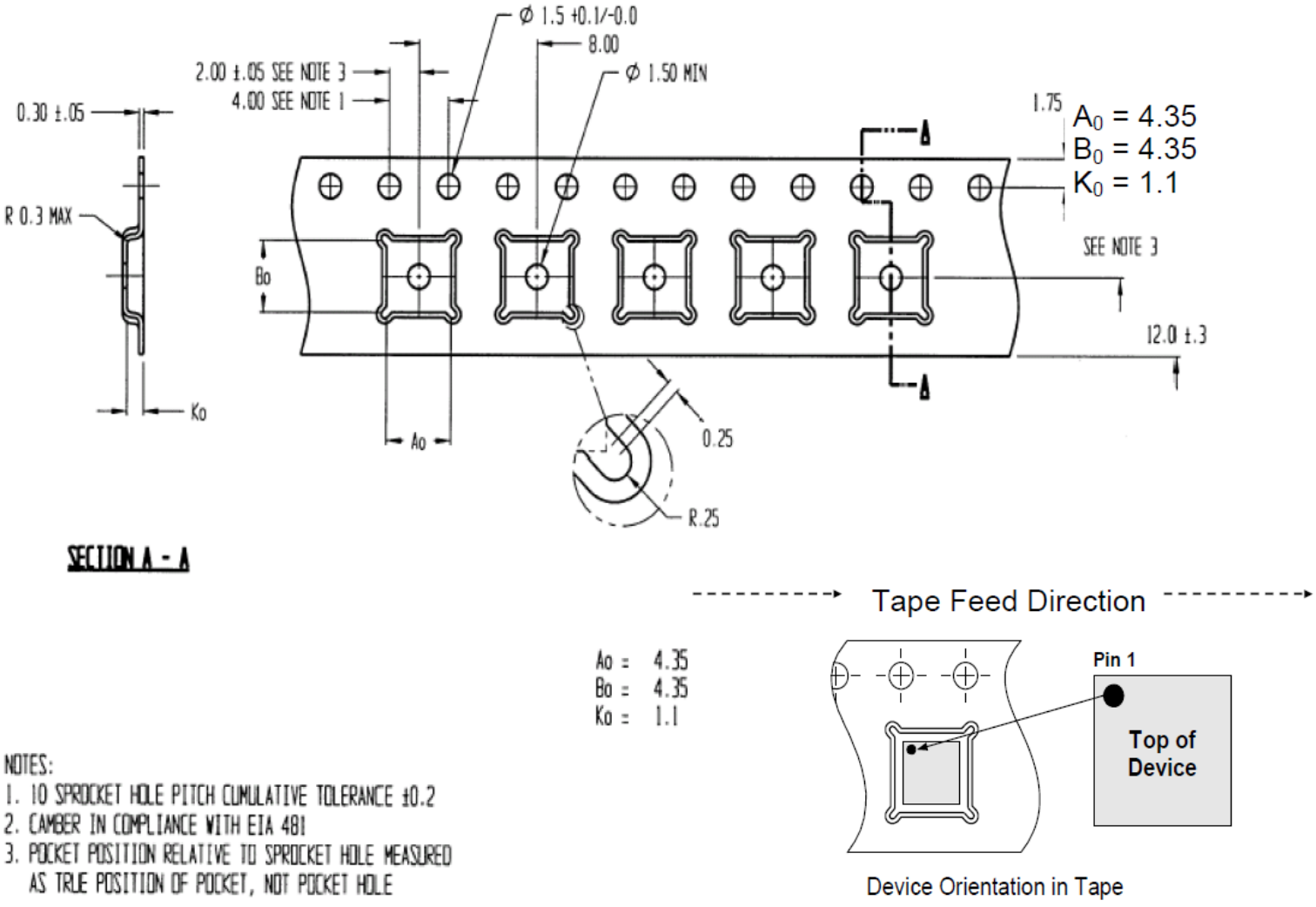

Figure 20. Tape and reel specification for the 24-lead 4 × 4 mm QFN package

Ordering information

Order code	Description	Packaging	Shipping method
PE42442A-Z	PE42442 SP4T RF switch	Green 24-lead 4 × 4 mm QFN	3000 units/T&R
EK42442-01	PE42442 evaluation kit	Evaluation kit	1/box

Document categories

Advance Information	The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.
Preliminary Specification	The data sheet contains preliminary data. Additional data may be added at a later date. pSemi reserves the right to change specifications at any time without notice to supply the best possible product.
Product Specification	The data sheet contains final data. In the event that pSemi decides to change the specifications, pSemi will notify customers of the intended changes by issuing a Customer Notification Form (CNF).
Product Brief	This document contains a shortened version of the data sheet. For the full data sheet, contact sales@psemi.com.

Contact and legal information

Sales contact	For additional information, contact Sales at sales@psemi.com.
Disclaimers	The information in this document is believed to be reliable. However, pSemi assumes no liability for the use of this information. Use shall be entirely at the user's own risk. No patent rights or licenses to any circuits described in this document are implied or granted to any third party. pSemi's products are not designed or intended for use in devices or systems intended for surgical implant, or in other applications intended to support or sustain life, or in any application in which the failure of the pSemi product could create a situation in which personal injury or death might occur. pSemi assumes no liability for damages, including consequential or incidental damages, arising out of the use of its products in such applications.
Patent statement	pSemi products are protected under one or more of the following U.S. patents: http://patents.psemi.com

Copyright and trademarks