PAC1811

Single-Channel Power Monitor with Accumulator, 42V Full Scale Range

Features

- 140 µA Active Current when Sampling at 1,024 sps
- High-Side Current Monitor with a Single Channel:
  - 100 mV Full Scale Range (FSR) for Sense Input Voltage (V_{SENSE}) with 16-bit Resolution
  - Selectable Bipolar Current Sense Capability:
    - -100 mV to + 100 mV FSR
    - -50 mV to +50 mV Programmable FSR/2
  - Very Low Input Current Simplifies Routing
- Voltage Monitor with Wide Bus Voltage Range:
  - 42V FSR for V_{BUS} with 16-bit Resolution
  - Selectable Bipolar Bus Voltage (V_{BUS}) Capability:
    - -42V to +42V FSR
    - -21V to +21V Programmable FSR/2
- Real Time Auto-calibration of Offset Error for Voltage and Current; No User Adjustment
- 1% Power Measurement Accuracy over a Wide Dynamic Range
- On-Chip Accumulation of 24-bit Results for Power Measurement:
  - 56-bit Power Accumulator Register for Recording Accumulated Power Data
  - 32-bit Accumulator Count Register
- User Programmable Sample Rates (f_S) of 8, 64, 256, 1024, 4096 and 8192 sps
  - User Programmable f_S = 16,384 sps for V_{BUS} or V_{SENSE} (only one option at a time)
  - Single-Shot Modes using Refresh Commands or General Purpose Input/Output (GPIO)
- SLOW Pin for Improved Low Power Mode
- 2.7V to 5.5V Supply Operation:
  - 1.62V to 5.5V Capable I^2C/SMBus and Digital I/O
  - SMBus 3.1 and I^2C Fast-mode Plus (1 MHz)
  - I^2C High-speed Mode (3.4 MHz)
- SMBus Address – 16 Options
- A0/A1 Pins can Function as $\overline{\text{ALERT}}$ Pins for Specific Addresses
- No Input Filters Required
- Step Limit for Average Variation Detection
- Patent Pending Addressing Alert Scheme
- Alerts Can Be Enabled for Accumulator Overflow, Conversion Cycle Complete and Limit Excursions, such as Under/Overvoltage or Current
- AEC-Q100 Qualified (Automotive Applications)
- Available Packages:
  - 3x3 mm 8-Lead VDFN with Multiple Exposed Pads and Stepped Wettable Flanks
  - 3x3 mm 10-Lead VDFN
- **10-Lead VDFN Only Features:**
  - Hardware Controlled Power-down Mode
  - Low-Side Power Monitor

Applications

- Low Current General Purpose Applications
- Battery Powered Applications
- Portable and Embedded Computing
- Smart Home and Smart City Applications
- USB Type-A, Type-B and Type-C Connectivity
- Networking
- Automotive
- Internet of Things (IoT)

Description

PAC1811 is a single-channel power monitor with a bus voltage monitor and current sense amplifier that feed into a 16-bit resolution Analog-to-Digital Converter (ADC). Designed for high-side current sensing, its digital circuitry performs power calculations and energy accumulation. This enables the device to monitor power with integration periods up to one year or longer.

The device stores bus voltage (V_{BUS}), shunt resistor voltage (V_{SENSE}) and accumulated proportional power (V_{POWER}) data. The embedded controller or system host can read the PAC1811 registers and retrieve the stored data.

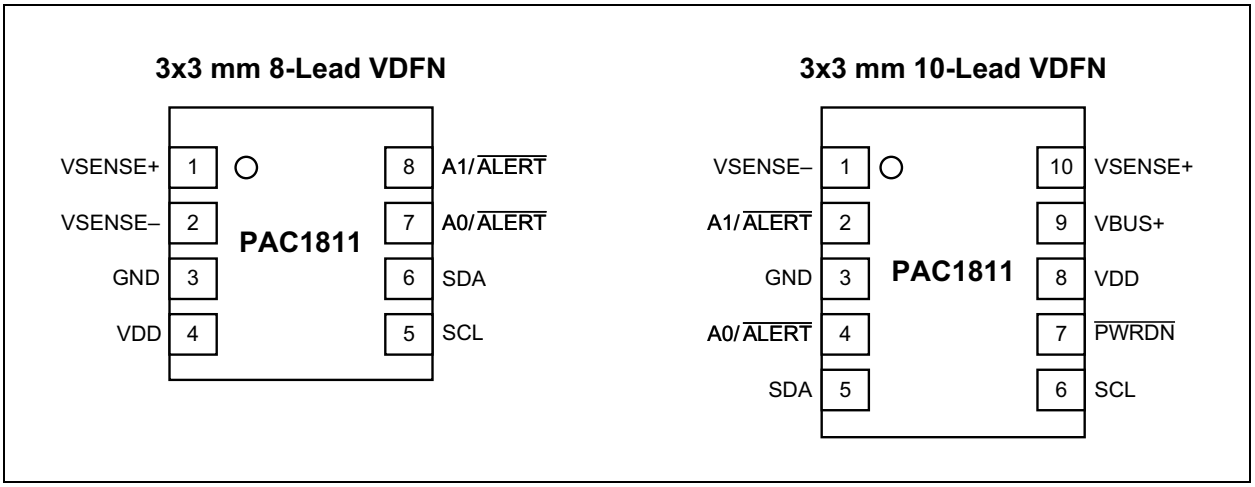
PAC1811 includes a configurable alert system that can trigger alerts when the device detects voltage, current or power excursions.

Configure the sample rate, power integration period, one-shot measurement settings and other controls using SMBus or I^2C communication.

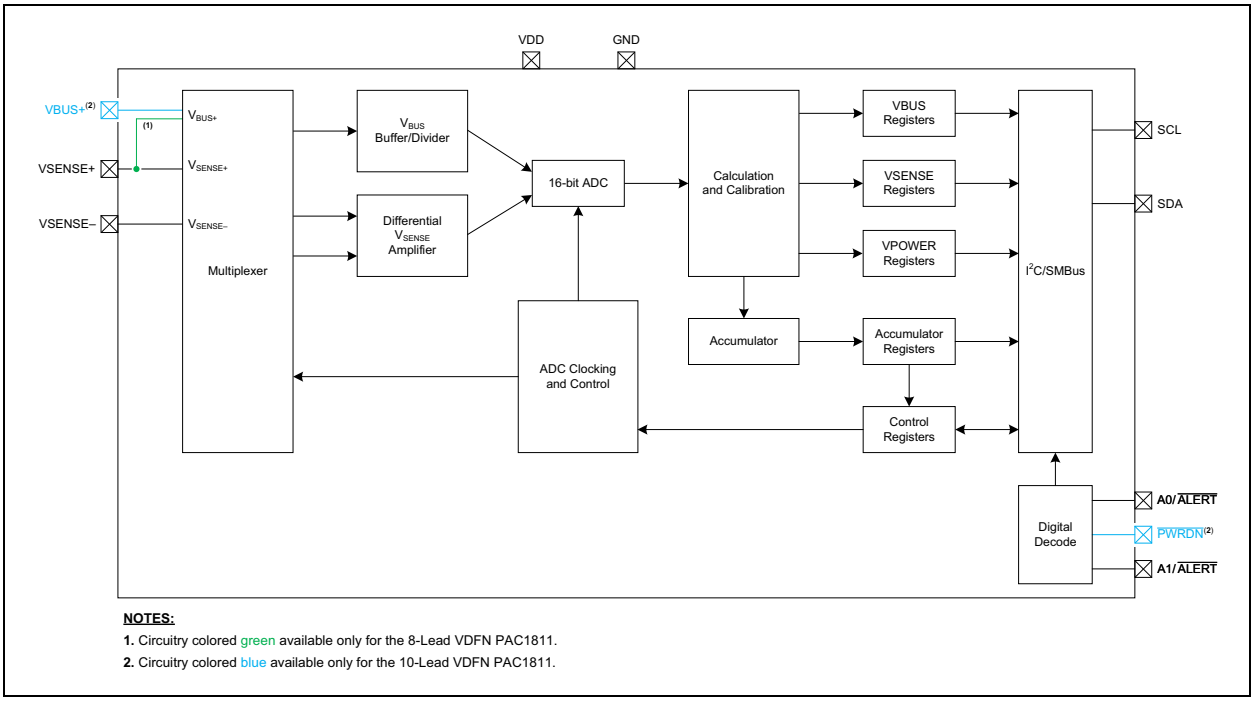
PAC1811 uses real-time calibration to minimize offset error. No input filters are required for this device. The built-in adjustable averaging function produces very low noise, high resolution measurement results.

The 10-Lead VDFN PAC1811 package has a VBUS+ pin that enables low-side power monitoring. This allows additional power savings using a Power-down feature not available for the 8-Lead VDFN package.

Package Types



Functional Block Diagram



NOTES:

1. Circuitry colored green available only for the 8-Lead VDFN PAC1811.

2. Circuitry colored blue available only for the 10-Lead VDFN PAC1811.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Absolute Maximum Ratings (†)

Supply Voltage (V_{DD}) . . . . . -0.3V to +6V
Voltage on VBUS+ pin . . . . . -0.3V to +75V
Voltage on VSENSE+ and VSENSE– pins . . . . . -0.3V to +75V
Voltage on $\overline{\text{PWRDN}}$ pin to GND . . . . . -0.3V to V_{DD}
Voltage on any other pin to GND . . . . . -0.3V to +6V
Voltage between VSENSE pins ($|V_{SENSE+} - V_{SENSE-}|$) 1V
Input Current to any pin except V_{DD} . . . . . ±100 mA
Output Short Circuit Current . . . . . continuous
Operating Temperature (T_A) . . . . . -40°C to +125°C
Storage Temperature (T_{STG}) . . . . . -55°C to +150°C
ESD Rating – All Pins – Human Body Model (V_{HBM}) . . . . . 4 kV
ESD Rating – All Pins – Charge Device Model (V_{CDM}) . . . . . 2 kV

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Figure 1-1 shows the electrostatic discharge (ESD) protection circuitry found on PAC1811. The voltage on the sense pins (VSENSE+ and VSENSE–) can be at 42V (75V absolute maximum) if V_{DD} = 0V.

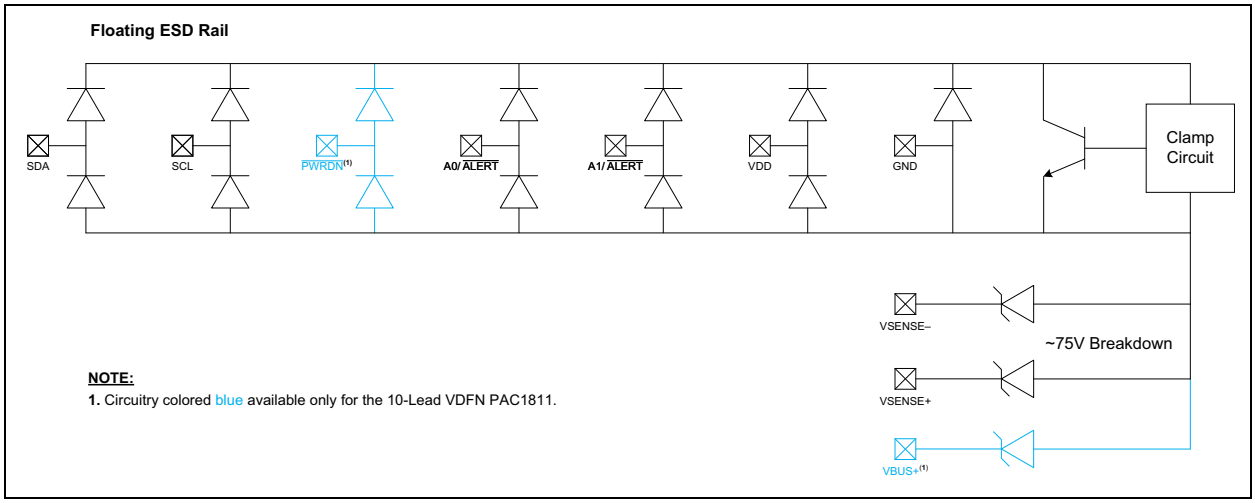


FIGURE 1-1: *PAC1811 ESD Protection Circuitry.*

1.2 DC Electrical Specifications

DC Electrical Characteristics: Unless otherwise indicated, all parameters apply at T_A = -40°C to +125°C, V_{DD} = 2.7V to 5.5V and V_{BUS} = 0V to 42V. Typical values are at T_A = 25°C, V_{DD} = 3.3V and $V_{SENSE} = V_{SENSE+} - V_{SENSE-}$ = 0V.

Parameters	Symbol	Min.	Typical	Max.	Units	Conditions
Power Supply						
Supply Voltage	V_{DD}	2.7	—	5.5	V	
Supply Active Current	I_{DD}	—	300	—	µA	Sample Rate: f_S = 8,192 sps
		—	140	275	µA	Sample Rate: f_S = 1,024 sps
		—	6	—	µA	Sample Rate: f_S = 8 sps
Supply Sleep Current	I_{SLEEP}	—	5	125	µA	
Supply Power-Down Current	I_{PWRDN}	—	0.1	20	µA	
Minimum Supply Voltage Rise Rate	$V_{DD\_RISE\_MIN}$	—	0.05	—	V/ms	0V to 5V in 100 ms, **Note 1**
Maximum Supply Voltage Rise Rate	$V_{DD\_RISE\_MAX}$	—	1000	—	V/ms	0V to 5V in 5 µs, **Note 1**
Power-on Reset (POR) Level (Rising)	V_{POR_RISING}	—	1.4	—	V	**Note 1**
POR Rearm Delay	t_{PORR}	—	20	—	ms	**Note 1**
Analog Input						
Bus Voltage	V_{BUS}	–0.2	—	42	V	Common mode voltage on SENSE pins, Referenced to GND
Sense Differential Input Voltage	V_{SENSE_DIF}	–1	—	1	V	
Sense Pins Input Current	I_{SENSE+} I_{SENSE-}	—	—	1	µA	$V_{SENSE+} = V_{SENSE-}$ = Full Scale, f_S = 1,024 sps, **Note 2**
		—	—	1	µA	V_{SENSE+} = 6V, V_{SENSE-} = 5.9V, f_S = 1,024 sps, **Note 2**
VBUS+ Pin Input Current	I_{BUS+}	—	—	1	µA	**10-Lead VDFN only**, V_{BUS} = Full Scale
		—	—	2	µA	**8-Lead VDFN only**, V_{BUS} = Full Scale, VBUS+ pin internally connected to VSENSE+ pin
Measurement Accuracy						
Sense Voltage ADC Data Resolution	V_{SENSE_RES}	—	—	16	bits	16-bit resolution in unipolar mode, 15 bits of resolution and one sign bit in bipolar modes
Sense Voltage LSB Step Size	V_{SENSE_LSB}	—	1.53	—	µV	FSR = 100 mV, 16-bit resolution
Bus Voltage LSB ADC Data Resolution	$V_{BUS\_RES\_LSB}$	—	—	16	bits	16-bit resolution in unipolar mode, 15 bits of resolution and one sign bit in bipolar modes
Bus Voltage LSB Step Size	V_{BUS_LSB}	—	0.641	—	mV	FSR = 42V, 16-bit resolution
Sense Voltage Gain Accuracy	$V_{SENSE\_GAIN\_ERR}$	—	±0.2	±0.4	%	T_A = 25°C typical
		—	±1	—	%	T_A = -40°C to +125°C
Sense Voltage Offset Accuracy	$V_{SENSE\_OFFSET\_ERR}$	—	±16	±100	µV	16-bit resolution, Referenced to input
Bus Voltage Gain Accuracy	$V_{BUS\_GAIN\_ERR}$	—	±0.02	±0.3	%	T_A = 25°C typical
		—	±0.2	—	%	T_A = 0°C to +125°C
Bus Voltage Offset Accuracy	$V_{BUS\_OFFSET\_ERR}$	—	±6	—	mV	16-bit resolution, Referenced to input

Note 1: No production testing. Characterization only.

2: All states, including leakage current and average value of capacitively coupled switching current.

1.2 DC Electrical Specifications (Continued)

DC Electrical Characteristics: Unless otherwise indicated, all parameters apply at T_A = -40°C to +125°C, V_{DD} = 2.7V to 5.5V and V_{BUS} = 0V to 42V. Typical values are at T_A = 25°C, V_{DD} = 3.3V and $V_{SENSE} = V_{SENSE+} - V_{SENSE-}$ = 0V.

Parameters	Symbol	Min.	Typical	Max.	Units	Conditions
Power Accumulator Accuracy (1σ error range with more than 1,000 accumulations)						
Accumulator Error	ACC_Err	—	0.8	—	%	V_{SENSE} = 97 mV
		—	1	—	%	V_{SENSE} = 10 mV
		—	1.5	—	%	V_{SENSE} = 1 mV
		—	8	—	%	V_{SENSE} = 100 µV
		—	15	—	%	V_{SENSE} = 50 µV
Active Mode Timing						
Time to First Communications	t_{INT_T}	—	12	20	ms	Time after V_{DD} is applied and PAC1811 is ready to initiate communications and sampling. **Note 1**
Transition Time from Sleep State to Start of Conversion Cycle	$t_{SLEEP\_TO\_ACTIVE}$	—	—	5	ms	Time from when a register write initiates a Sleep state exit to the start of a conversion cycle for Single-shot modes. A conversion cycle lasts 1 ms by default and varies depending on f_S. **Note 1**
Digital I/O Pins (SLOW/$\overline{\text{ALERT}}$, $\overline{\text{PWRDN}}$, SMBCLK, SMBDAT)						
Input High Voltage	V_{IH}	1.35	—	—	V	A0, A1, SDA and SCL pins
Input Low Voltage	V_{IL}	—	—	0.8	V	A0, A1, SDA and SCL pins
Input High Voltage ($\overline{\text{PWRDN}}$)	V_{IH_PWRDN}	1.35	—	—	V	$\overline{\text{PWRDN}}$ pin
Input Low Voltage ($\overline{\text{PWRDN}}$)	V_{IL_PWRDN}	—	—	0.4	V	$\overline{\text{PWRDN}}$ pin
Input Hysteresis	V_{HYS}	—	30	—	mV	Only when A0 and A1 pins set as inputs
Output Low Voltage	V_{OL}	—	—	0.4	V	Sinking current: • 8 mA for the A0 and A1 pins • 20 mA for SDA pin
Leakage Current	I_{LEAK}	-7	—	7	µA	Powered

Note 1: No production testing. Characterization only.

2: All states, including leakage current and average value of capacitively coupled switching current.

1.3 AC Electrical Specifications

AC Electrical Characteristics: Unless otherwise indicated, maximum values apply at T_A = -40°C to +125°C, V_{DD} = 2.7V to 5.5V, $V_{I/O}$ = 1.62V to 5.5V and V_{BUS} = 0V to 42V. Typical values are at T_A = 25°C, V_{DD} = 3.3V, $V_{I/O}$ = 3.3V, V_{BUS} = 42V and $V_{SENSE} = V_{SENSE+} - V_{SENSE-}$ = 0V.

Parameters	Symbol	Min.	Typical	Max.	Units	Conditions
I²C/SMBus Timing						
Clock Frequency	f_{CLK}	0.01	—	1	MHz	Fast-mode Plus. No minimum f_{CLK} if timeout is disabled.
		0.01	—	3.4	MHz	High-speed Mode. No minimum f_{CLK} if timeout is disabled.
Spike Suppression	t_{SP}	0	—	50	ns	Fast-mode Plus
		0	—	10	ns	High-speed Mode
Bus Free Time: Stop to Start	t_{BUF}	0.5	—	—	µs	**Note 1**
Hold Time after Repeated Start Condition	$t_{HD:STA}$	0.26	—	—	µs	Fast-mode Plus, **Note 1**
		0.16	—	—	µs	High-speed Mode, **Note 1**
Repeated Start Condition Setup Time	$t_{SU:STA}$	0.26	—	—	µs	Fast-mode Plus, **Note 1**
		0.16	—	—	µs	High-speed Mode, **Note 1**

Note 1: In compliance with the SMBus 3.1 standard.

2: No production testing. Characterization only.

1.3 AC Electrical Specifications (Continued)

AC Electrical Characteristics: Unless otherwise indicated, maximum values apply at T_A = -40°C to +125°C, V_{DD} = 2.7V to 5.5V, $V_{I/O}$ = 1.62V to 5.5V and V_{BUS} = 0V to 42V. Typical values are at T_A = 25°C, V_{DD} = 3.3V, $V_{I/O}$ = 3.3V, V_{BUS} = 42V and $V_{SENSE} = V_{SENSE+} - V_{SENSE-}$ = 0V.

Parameters	Symbol	Min.	Typical	Max.	Units	Conditions
I²C/SMBus Timing (continued)						
Setup Time: Stop	$t_{SU:STO}$	0.26	—	—	µs	Fast-mode Plus, **Note 1**
		0.16	—	—	µs	High-speed Mode, **Note 1**
Setup Time: Start	$t_{SU:STA}$	0.26	—	—	µs	Fast-mode Plus, **Note 1**
		0.16	—	—	µs	High-speed Mode, **Note 1**
Data Hold Time	$t_{HD:DAT}$	0	—	—	ns	Fast-mode Plus, **Note 1**
		0	—	70	ns	High-speed Mode, **Note 1**
Data Setup Time	$t_{SU:DAT}$	50	—	—	ns	Fast-mode Plus, **Note 1**
		10	—	—	ns	High-speed Mode, **Note 1**
Clock Low Period	t_{LOW}	0.5	—	—	µs	Fast-mode Plus, **Note 1**
		0.16	—	—	µs	High-speed Mode, **Note 1**
Clock High Period	t_{HIGH}	0.26	—	50	ns	Fast-mode Plus, **Note 2**
		0.06	—	50	ns	High-speed Mode, **Note 2**
Clock/Data Fall Time	t_{FALL}	12	—	120	ns	Fast-mode Plus, **Note 2**
Clock/Data Rise Time	t_{RISE}	—	—	120	ns	Fast-mode Plus, **Note 2**
Clock Fall Time	t_{FCL}	10	—	40	ns	High-speed Mode, **Note 2**
Clock Rise Time	t_{RCL}	10	—	40	ns	High-speed Mode, **Note 2**
Data Fall Time	t_{FDA}	10	—	80	ns	High-speed Mode, **Note 2**
Data Rise Time	t_{RDA}	10	—	80	ns	High-speed Mode, **Note 2**
Capacitive Load	C_{LOAD}	—	—	550	pF	Per Bus line, Fast-mode Plus
		—	—	100	pF	Per Bus line, High-speed Mode
Pin SLOW Pulse Width	t_{SLOW_PW}	100	—	—	µs	Pulses shorter than 100 µs can remain undetected

Note 1: In compliance with the SMBus 3.1 standard.
2: No production testing. Characterization only.

1.4 Temperature Specifications

Electrical Characteristics: Unless otherwise indicated, all limits are specified for V_{DD} = 2.7V to 5.5V, $V_{I/O}$ = 1.62V to 5.5V, V_{BUS} = 0V to 42V and $V_{SENSE} = V_{SENSE+} - V_{SENSE-}$ = 0V. Typical values are at V_{DD} = 3.3V, $V_{I/O}$ = 3.3V and V_{BUS} = 42V.

Parameters	Symbol	Min.	Typical	Max.	Units	Conditions
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	
Storage Temperature Range	T_{STG}	-55	—	+150	°C	
Thermal Package Resistances						
Junction to Ambient, 8-Lead VDFN	θ_{JA}	—	97.934	—	°C/W	
Junction to Ambient, 8-Lead VDFN	θ_{JB}	—	40.891	—	°C/W	
Junction to Ambient, 8-Lead VDFN	θ_{JC}	—	67.561	—	°C/W	
Junction to Ambient, 10-Lead VDFN	θ_{JA}	—	73.312	—	°C/W	
Junction to Ambient, 10-Lead VDFN	θ_{JB}	—	21.221	—	°C/W	
Junction to Ambient, 10-Lead VDFN	θ_{JC}	—	68.284	—	°C/W	

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = -40°C to +125°C, V_{DD} = 2.7V to 5.5V, V_{BUS} = 0V to 42V, $V_{SENSE} = V_{SENSE+} - V_{SENSE-}$ = 0V.

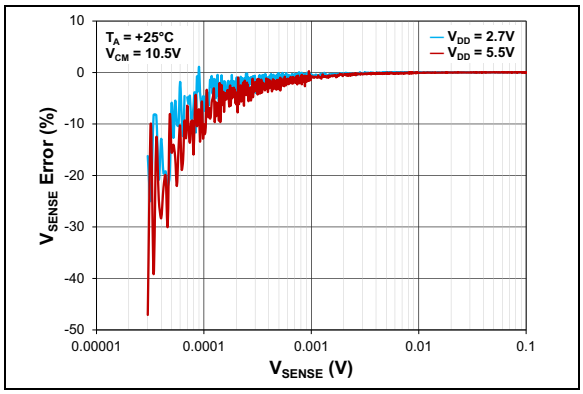


FIGURE 2-1: *V_{SENSE} Error vs. V_{SENSE}, T_A = 25°C, Multiple V_{DD}, Unipolar Mode.*

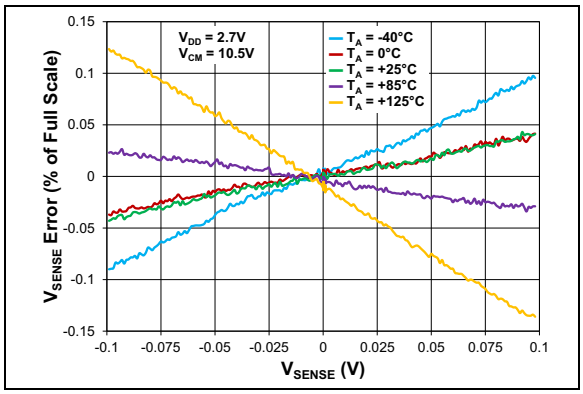


FIGURE 2-4: *V_{SENSE} Error vs. V_{SENSE}, V_{DD} = 2.7V, Multiple T_A, Bipolar FSR Mode.*

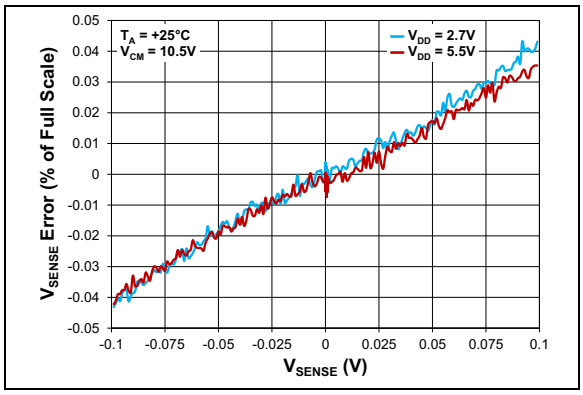


FIGURE 2-2: *V_{SENSE} Error vs. V_{SENSE}, T_A = 25°C, Multiple V_{DD}, Bipolar FSR Mode.*

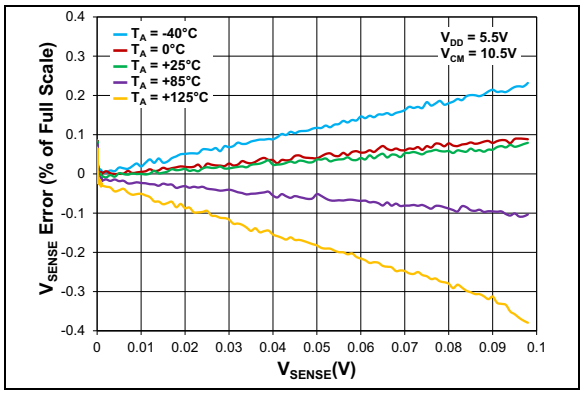


FIGURE 2-5: *V_{SENSE} Error vs. V_{SENSE}, V_{DD} = 5.5V, Multiple T_A, Unipolar Mode.*

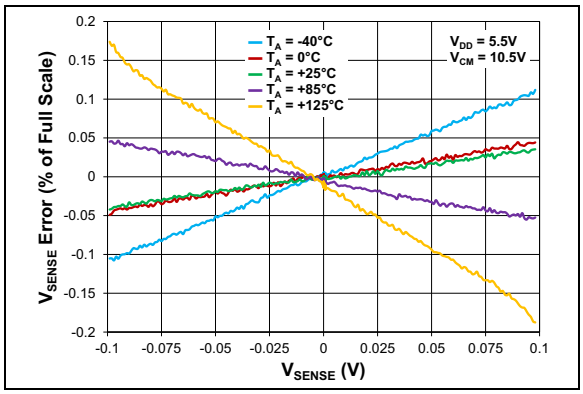


FIGURE 2-3: *V_{SENSE} Error vs. V_{SENSE}, V_{DD} = 5.5V, Multiple T_A, Bipolar FSR Mode.*

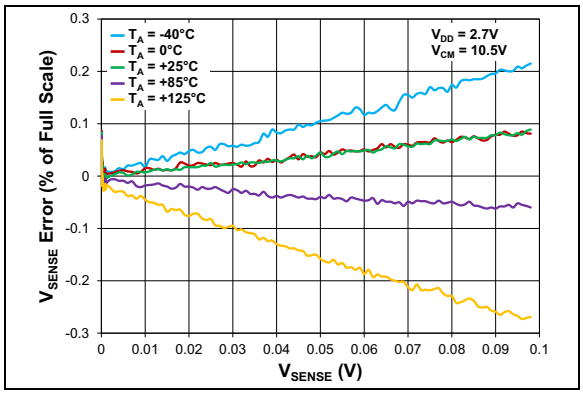


FIGURE 2-6: *V_{SENSE} Error vs. V_{SENSE}, V_{DD} = 2.7V, Multiple T_A, Unipolar Mode.*

Note: Unless otherwise indicated, T_A = -40°C to +125°C, V_{DD} = 2.7V to 5.5V, V_{BUS} = 0V to 42V, V_{SENSE} = V_{SENSE+} – $V_{SENSE–}$ = 0V.

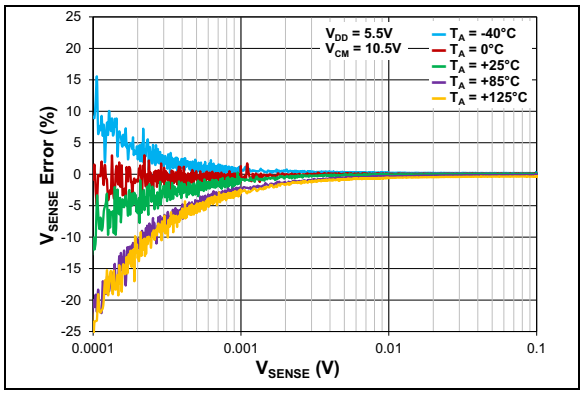


FIGURE 2-7: *V_{SENSE} Error vs. V_{SENSE}, V_{DD} = 5.5V, Multiple T_A, Unipolar Mode, Logarithmic Scale.*

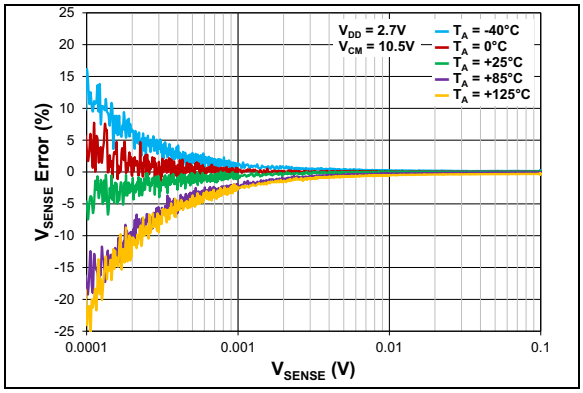


FIGURE 2-8: *V_{SENSE} Error vs. V_{SENSE}, V_{DD} = 2.7V, Multiple T_A, Unipolar Mode, Logarithmic Scale.*

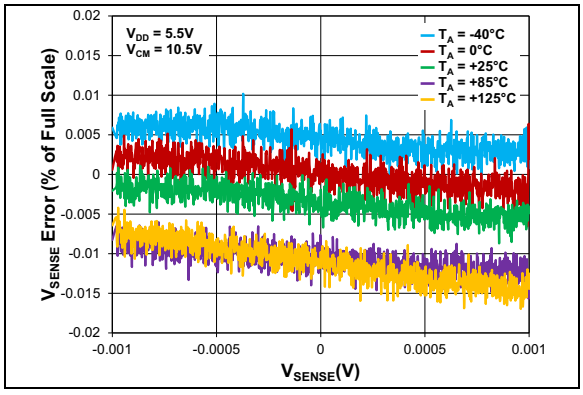


FIGURE 2-9: *V_{SENSE} Error vs. V_{SENSE}, V_{DD} = 5.5V, Multiple T_A, Bipolar FSR Mode, Zoom View.*

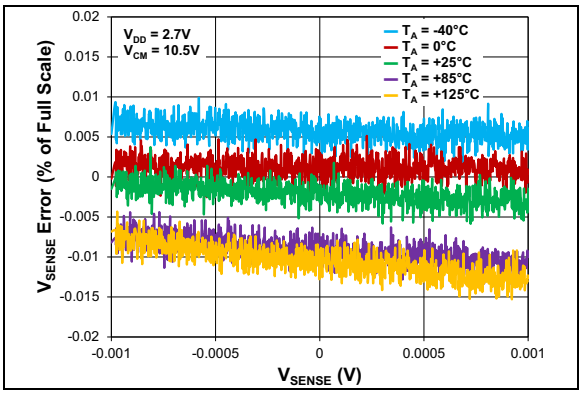


FIGURE 2-10: *V_{SENSE} Error vs. V_{SENSE}, V_{DD} = 2.7V, Multiple T_A, Bipolar FSR Mode, Zoom View.*

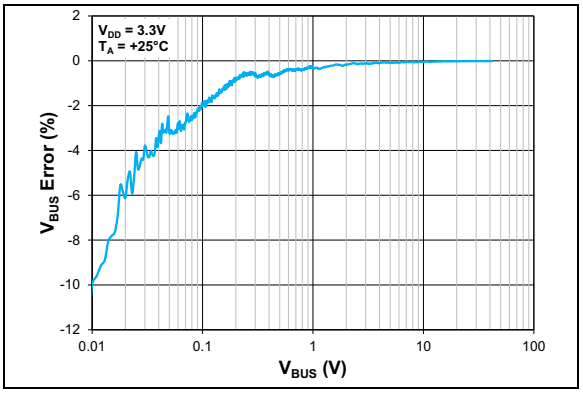


FIGURE 2-11: *V_{BUS} Error vs. V_{BUS}, V_{DD} = 3.3V, T_A = 25°C, Unipolar Mode, Logarithmic Scale.*

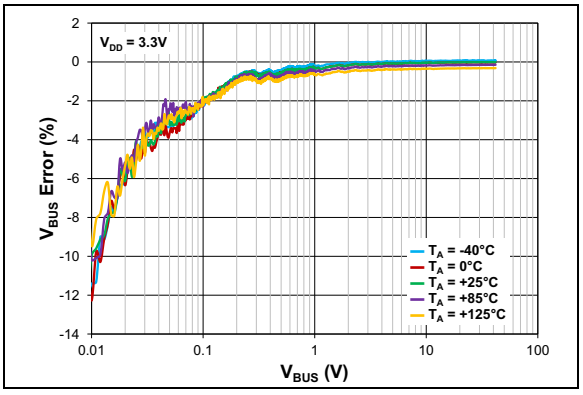


FIGURE 2-12: *V_{BUS} Error vs. V_{BUS}, V_{DD} = 3.3V, Multiple T_A, Unipolar Mode, Logarithmic Scale.*

Note: Unless otherwise indicated, T_A = -40°C to +125°C, V_{DD} = 2.7V to 5.5V, V_{BUS} = 0V to 42V, V_{SENSE} = V_{SENSE+} – $V_{SENSE–}$ = 0V.

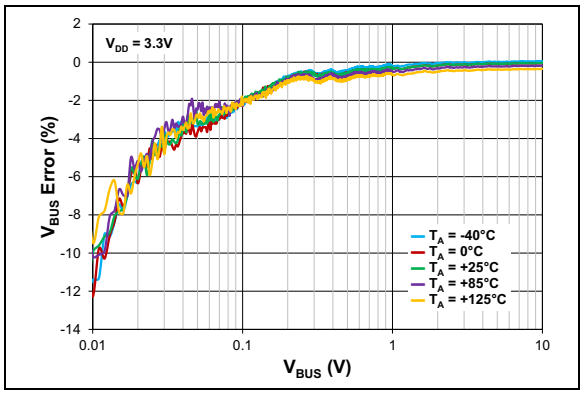


FIGURE 2-13: *V_{BUS} Error vs. V_{BUS}, V_{DD} = 3.3V, Multiple T_A, Unipolar Mode, Logarithmic Scale, Zoom View.*

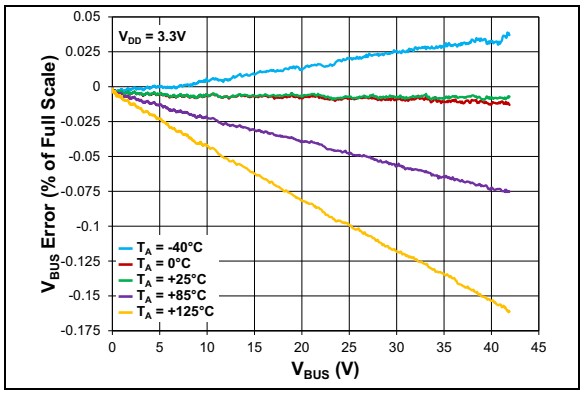


FIGURE 2-16: *V_{BUS} Error vs. V_{BUS}, V_{DD} = 3.3V, Multiple T_A, Bipolar FSR Mode.*

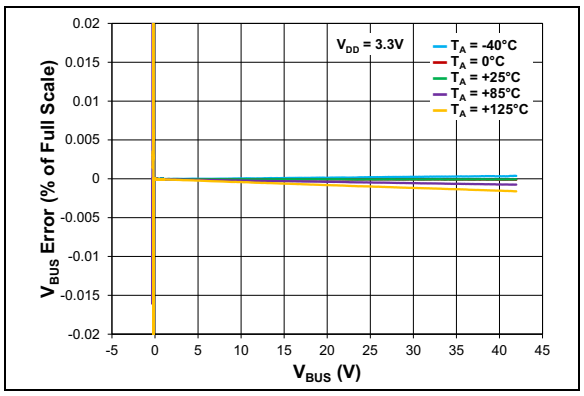


FIGURE 2-14: *V_{BUS} Error vs. V_{BUS}, V_{DD} = 3.3V, Multiple T_A, Bipolar FSR Mode.*

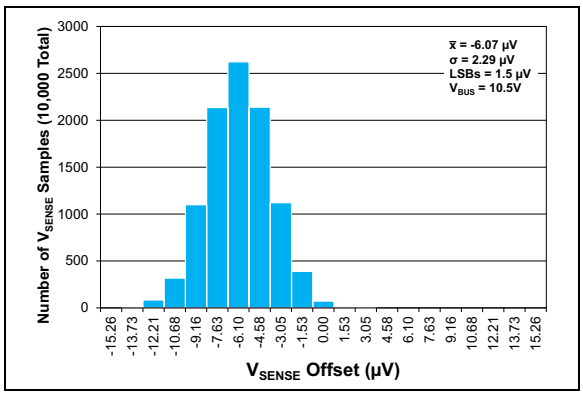


FIGURE 2-17: *V_{SENSE} Offset Histogram, Bipolar FSR/2 Mode, n = 10,000 Total Samples, 8x Average.*

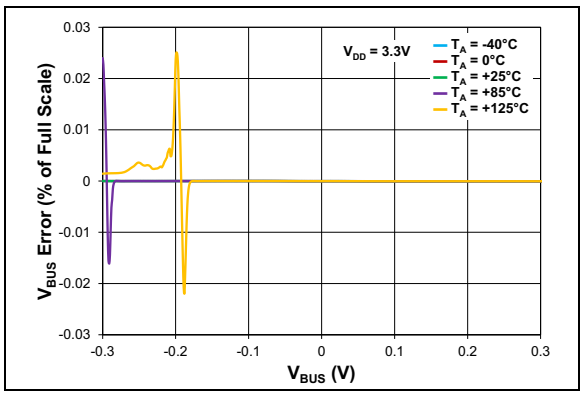


FIGURE 2-15: *V_{BUS} Error vs. V_{BUS}, V_{DD} = 3.3V, Multiple T_A, Bipolar FSR Mode, Zoom View.*

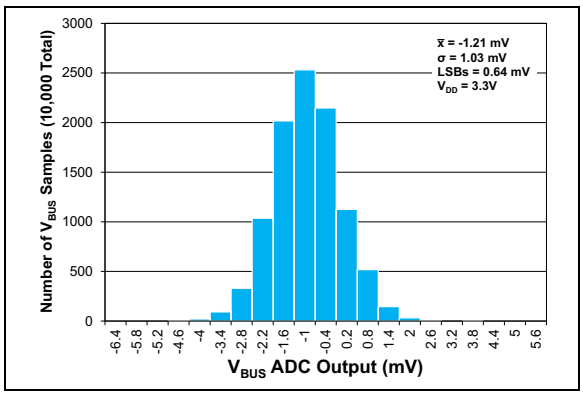


FIGURE 2-18: *V_{BUS} Offset Histogram, Bipolar FSR/2 Mode, n = 10,000 Total Samples, 8x Average.*

Note: Unless otherwise indicated, T_A = -40°C to +125°C, V_{DD} = 2.7V to 5.5V, V_{BUS} = 0V to 42V, V_{SENSE} = V_{SENSE+} – $V_{SENSE–}$ = 0V.

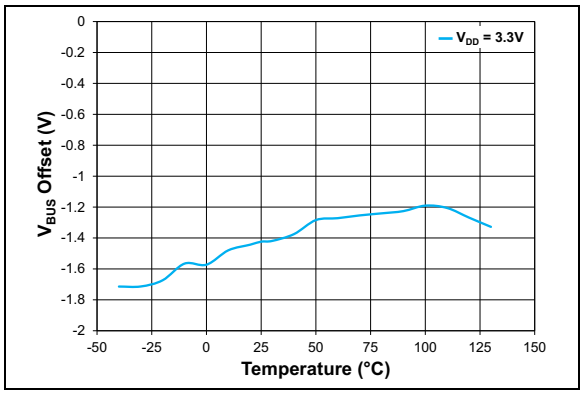


FIGURE 2-19: *V_{BUS} Offset vs. T_A, V_{DD} = 3.3V, Bipolar FSR Mode.*

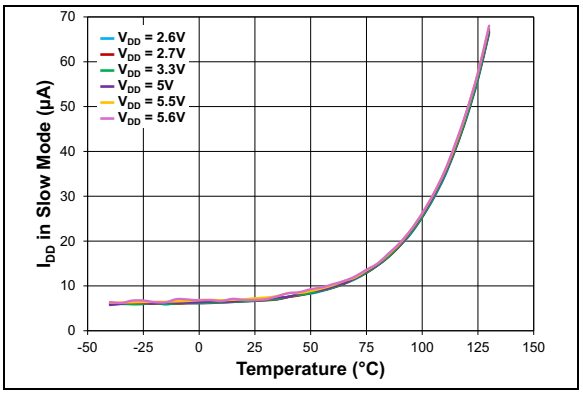


FIGURE 2-22: *I_{DD} in Slow Mode vs. T_A, Multiple V_{DD}.*

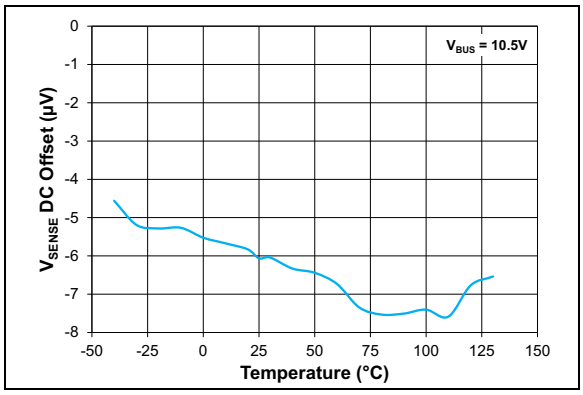


FIGURE 2-20: *V_{SENSE} DC Offset vs. T_A, V_{BUS} = 10.5V, Bipolar FSR Mode.*

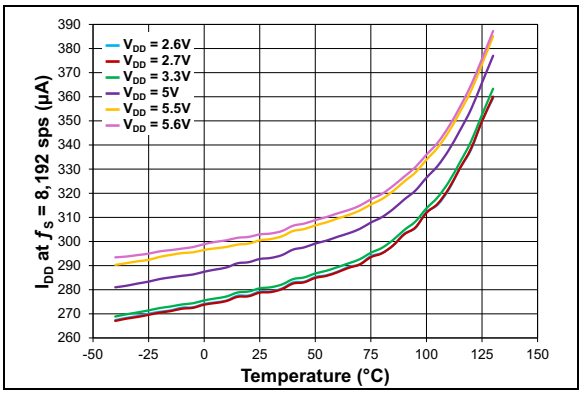


FIGURE 2-23: *I_{DD} at f_S = 8,192 sps vs. T_A, Multiple V_{DD}.*

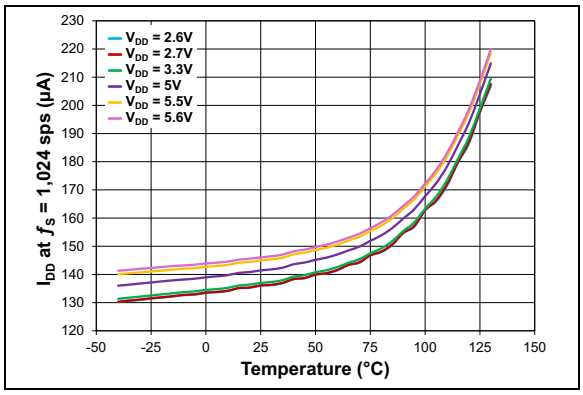


FIGURE 2-21: *I_{DD} at f_S = 1,024 sps vs. T_A, Multiple V_{DD}.*

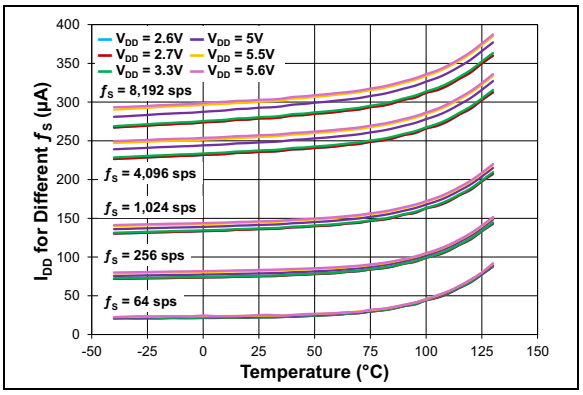


FIGURE 2-24: *I_{DD} vs. T_A, Multiple V_{DD}, Multiple f_S.*

Note: Unless otherwise indicated, T_A = -40°C to +125°C, V_{DD} = 2.7V to 5.5V, V_{BUS} = 0V to 42V, V_{SENSE} = V_{SENSE+} – $V_{SENSE–}$ = 0V.

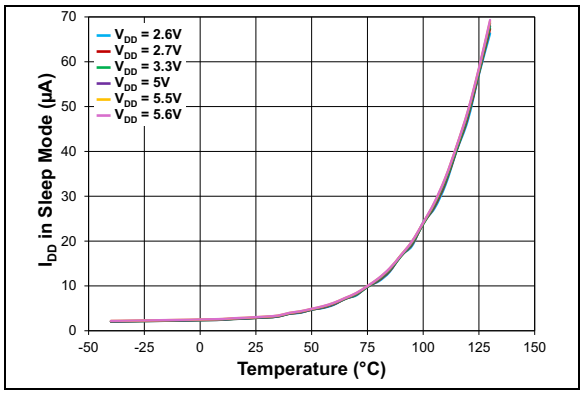


FIGURE 2-25: *I_{DD} in Sleep Mode vs. T_A, Multiple V_{DD}.*

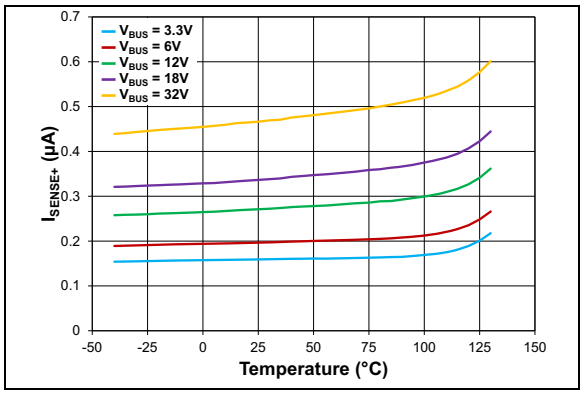


FIGURE 2-28: *I_{SENSE+} vs. T_A, Common Mode, Multiple V_{BUS}.*

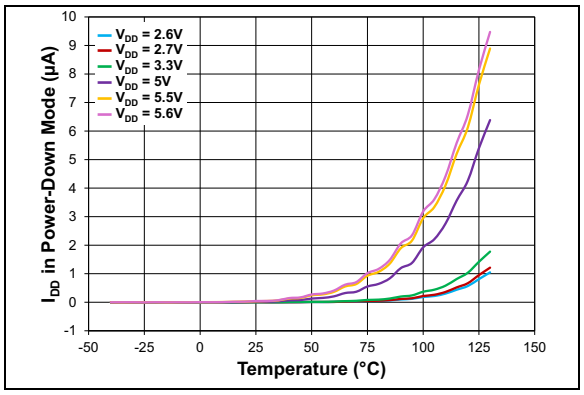


FIGURE 2-26: *I_{DD} in Power-down Mode vs. T_A, Multiple V_{DD}.*

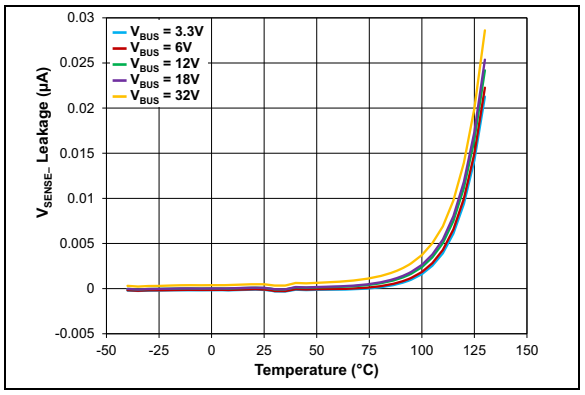


FIGURE 2-29: *V_{SENSE-} Leakage vs. T_A, Common Mode, Multiple V_{BUS}.*

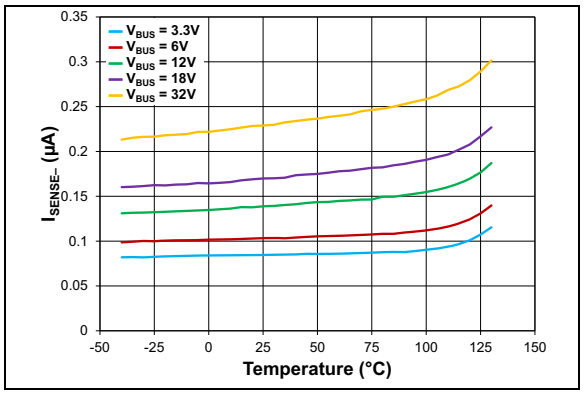


FIGURE 2-27: *I_{SENSE-} vs. T_A, Common Mode, Multiple V_{BUS}.*

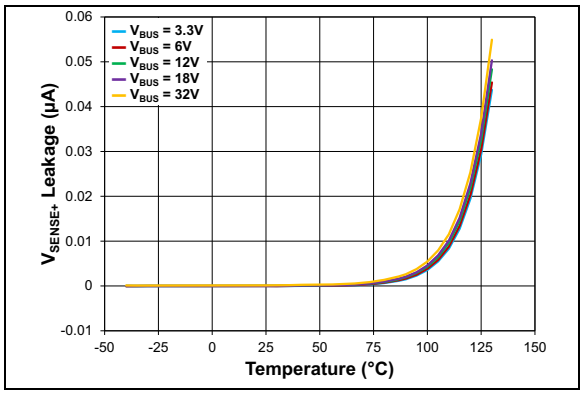


FIGURE 2-30: *V_{SENSE+} Leakage vs. T_A, Common Mode, Multiple V_{BUS}.*

Note: Unless otherwise indicated, T_A = -40°C to +125°C, V_{DD} = 2.7V to 5.5V, V_{BUS} = 0V to 42V, V_{SENSE} = V_{SENSE+} – $V_{SENSE–}$ = 0V.

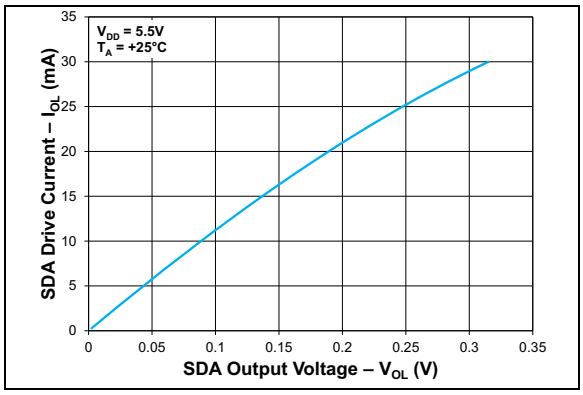


FIGURE 2-31: *I_{OL} vs. V_{OL}, T_A = 25°C, V_{DD} = 5.5V.*

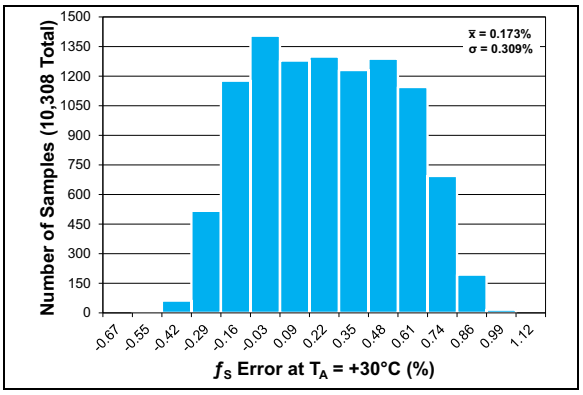


FIGURE 2-33: *f_S Error across T_A = 30°C, n = 10,308 Total Samples.*

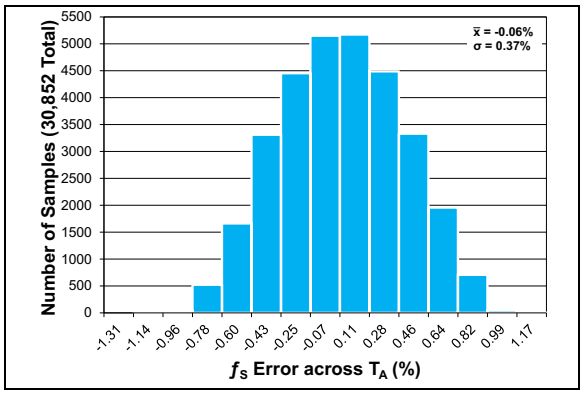


FIGURE 2-32: *f_S Error across T_A = -40°C to +125°C, n = 30,852 Total Samples.*

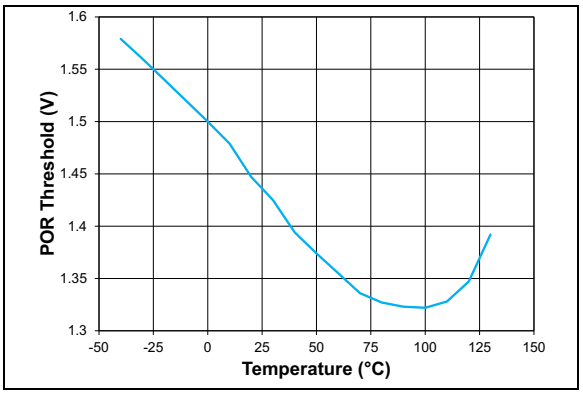


FIGURE 2-34: *POR Threshold vs. T_A.*

3.0 PIN DESCRIPTIONS

Table 3-1 describes the pins of PAC1811.

TABLE 3-1: PAC1811 PIN DESCRIPTIONS

Pin Number		Pin Symbol	Description
8-Lead VDFN	10-Lead VDFN		
1	10	VSENSE+	Analog input pin. 0 to FSR. Connect to source side of the shunt resistor (R_{SHUNT}).
2	1	VSENSE–	Analog input pin. 0 to FSR. Connect to load side of R_{SHUNT}.
3	3	GND	Ground pin for the integrated circuit (IC).
4	8	VDD	IC power pin.
5	6	SCL	SMBus clock input pin.
6	5	SDA	SMBus data I/O pin.
7	4	A0	Multifunction pin. Digital I/O. Address 0, $\overline{\text{ALERT}}$, SLOW and GPIO pin.
8	2	A1	Multifunction pin. Digital I/O. Address 1, $\overline{\text{ALERT}}$, SLOW and GPIO pin.
—	7	$\overline{\text{PWRDN}}$	When this pin becomes active low, PAC1811 enters power-down state. Hardware triggered POR.
—	9	VBUS+	Analog input pin. Connect to V_{BUS}. Configurable for high-side or low-side power monitoring.

3.1 Sense Voltage Pins (VSENSE+ and VSENSE–)

Pins VSENSE+ and VSENSE– form the differential input for measuring voltage across R_{SHUNT} in the circuit application.

Note: **8-Lead VDFN only:** Pin VSENSE+ also acts as the input pin for V_{BUS}

3.2 Ground Pin (GND)

This pin is the system ground.

3.3 Positive Power Supply Voltage Pin (VDD)

This is the power supply input pin for PAC1811. It has a voltage range of 2.7V to 5.5V. Bypass it with a 100 nF ceramic capacitor connected to GND near the IC.

3.4 SMBus Data (SMBDAT) Pin (SDA)

This is the bidirectional SMBus data pin. This pin is open-drain and requires a pull-up resistor connected to the external communication voltage rail.

3.5 SMBus Clock (SMBCLK) Pin (SCL)

This is the SMBus clock input pin and requires an external pull-up resistor, except if used in High-speed mode, which requires a CMOS driver from the host.

3.6 A0 and A1 Multi-functional Pins

These pins are used to define the I^2C/SMBus address. When pulled high through a resistor to V_{DD}, the A0 or A1 pin can be used as an $\overline{\text{ALERT}}$, SLOW or GPIO pin.

These pins are an open-drain configuration.

3.7 Power-down Pin ($\overline{\text{PWRDN}}$)

When this pin is pulled low, PAC1811 enters the Power-down state. In this state, all the circuitry powers down, including the SMBus pins.

Note 1: **10-Lead VDFN only**

2: Maximum voltage on this pin is V_{DD}. Do not pull this pin up to voltages that exceed V_{DD}

3.8 Positive Bus Voltage Pin (VBUS+)

This pin is the input pin for V_{BUS}. It can be used as either a high-side or a low-side power monitor.

Note: This pin is available only for the **10-Lead VDFN**.

4.0 DEVICE DESCRIPTION

This section describes the functional requirements of PAC1811 presented in the Functional Block Diagram.

4.1 Definitions

I. V_{BUS} is the system bus voltage measured across:

- For **8-Lead VDFN:** VSENSE+ pin to GND
- For **10-Lead VDFN:** VBUS+ pin to GND

For more details, see **Section 4.3**.

II. V_{SENSE} is the sense input voltage measured across an external current shunt resistor, R_{SHUNT}. The differential voltage is measured between the VSENSE+ and VSENSE– pins. For more details, see **Section 4.4**.

III. V_{POWER} is the result of multiplying V_{BUS} and V_{SENSE} samples together: $V_{POWER} = V_{BUS} \times V_{SENSE}$. Use V_{POWER} to calculate the actual electrical power. For details, see **Section 4.8**.

IV. A **conversion cycle** is the time period during which PAC1811 performs the following operations in order:

1. Sample V_{BUS} and V_{SENSE}
2. Convert V_{BUS} and V_{SENSE} results from analog to digital values
3. Calculate V_{POWER}
4. Accumulate V_{POWER} results

Note: The duration of a conversion cycle, t_{CC}, varies with the selected sample rate, f_S:

$$t_{CC} = 1/f_S$$

- f_S = 8 sps → t_{CC} = 125 ms
- f_S = 1,024 sps → t_{CC} = 977 µs
- f_S = 8,192 sps → t_{CC} = 122 µs

V. PAC1811 supports the following three commands: Refresh, Refresh_G and Refresh_V. Throughout the document, the term "**Refresh (any)**" refers to situations when any of the three refresh commands can be used.

4.2 Detailed Description

The input pins to V_{BUS} and V_{SENSE} connect directly to their own amplifiers. The outputs of these amplifiers are sampled serially for both V_{BUS} and V_{SENSE}. Offset is removed using a modified correlated double sampling method, while the gain error is calibrated in production. After every completed conversion, V_{BUS} and V_{SENSE} are multiplied together to produce V_{POWER}.

PAC1811 has a single 16-bit ADC that is managed by its own internal oscillator and digital logic.

When a Refresh (any) command is issued, measurements update 1 µs after the current conversion cycle completes. The timing depends on the selected sample rate and the moment the Refresh (any) command was issued.

4.2.1 INITIAL OPERATION

After POR and the start-up sequence, PAC1811 enters Active state and begins sequentially sampling device inputs. PAC1811 first samples voltage and current, then calculates the instantaneous electrical power and sums the result in the power accumulator.

PAC1811 has a default sample rate of 1,024 sps. It can be programmed over I^2C or SMBus. Pin A0 or A1 can operate as the SLOW pin (see **Section 4.2.8**). Holding the SLOW pin high overrides the programmed sample rate, gathering 8 sps (Slow mode). When sampling at rates lower than the maximum of 8,192 sps, PAC1811 enters a low-power state (no sampling) for a portion of the conversion cycle, resulting in minimum power dissipation.

A Refresh command updates the data registers (see **Section 6.2**) and resets the accumulator (VACC) and the accumulator count (ACC_COUNT) registers. To update data registers without resetting the VACC or ACC_COUNT registers, issue a Refresh_V command.

Issue a Refresh or Refresh_V command to activate changes to the CONTROL register. When writing to this register, the new settings take effect after the current conversion cycle (active sampling) or before the next conversion cycle that follows a Refresh or Refresh_V command.

Note: When enabled, Auto-refresh changes this operation. For details, see **Section 4.2.5**.

4.2.2 REFRESH COMMAND

The host sends a Refresh command after changing the CONTROL register and/or before reading accumulator data from PAC1811. This is used by the host to control the accumulation period.

Note: Various registers require a Refresh (any) command to activate new settings.

Data registers for V_{BUS}, V_{SENSE}, V_{POWER}, accumulator and accumulator count update with every Refresh command and their values become static until the next Refresh command. These data registers become ready-to-read within one conversion cycle after issuing a Refresh command. The registers can be read by the host at any time up until the next Refresh command issues. For more details, see Register 6-1.

Note 1: Refresh commands reset the accumulator and accumulator count. However, they do not reset input sampling, data conversion and power integration. These continue as set by the CONTROL register.

2: Changes to control and configuration registers take effect one conversion cycle after issuing a Refresh command.

Internal values continue to update according to the sample rate selected in the CONTROL register.

Note: Issue a Refresh command to save the results of the most recently completed conversion cycle to the VBUS, VSENSE and VPOWER registers. Otherwise, the results of the conversion are discarded. For more details, see Register 6-1.

4.2.3 REFRESH_G COMMAND

The Refresh_G command is identical in all aspects to the Refresh command, with added compatibility for the I^2C General Call address (**0000 000b**).

Using Refresh_G, the host issues a single Refresh command to all PAC1811 devices in the system. The data from this Refresh_G command is read device by device to capture a snapshot of system power and energy for all PAC1811 units.

Besides the General Call address, Refresh_G can also be issued with a valid target address. In this scenario, only the PAC1811 device with the specified target address receives the command. For more details, see Register 6-21.

4.2.4 REFRESH_V COMMAND

To read V_{SENSE} and V_{BUS} measurements, as well as the most recent power calculation and/or accumulator values and accumulator count without resetting the accumulators, issue a Refresh_V command.

To ensure data registers are ready-to-read by the host, wait for one conversion cycle to complete after issuing a Refresh_V command. Input sampling, data conversion and power integration are not interrupted and continue as set by the CONTROL register. Data registers remain available to read until the next Refresh or Refresh_V command is issued.

Note: The accumulator and accumulator count are not reset when issuing a Refresh_V.

Refresh_V can activate changes to the CONTROL register, just like the Refresh command. However, the Refresh_V command activates these changes without resetting the accumulators or the accumulator count. For more details, see Register 6-22.

4.2.5 AUTO-REFRESH

The Auto-refresh function speeds up the transition time from the Conversion-complete state to Ready-to-read state.

To enable Auto-refresh, set the AUTO_REFRESH[1:0] bits in the CONTROL register. When these bits are set, PAC1811 performs a Limited Refresh: only the values stored in the data registers migrate to the I^2C domain (populate I^2C registers). For details, see Register 6-2.

The following registers required a manual Refresh (any) command to update their values. They cannot be updated while the Auto-refresh function is enabled.

- CONTROL
- NEG_PWR_FSR
- SLOW
- SLOW_ALERT0
- GPIO_ALERT1
- ACC_FULL_LIMIT
- ALERT_ENABLE
- ACC_COUNT_PRESET
- VACC_PRESET

When Auto-refresh is enabled, all manual Refresh (any) commands are ignored, except when setting the AUTO_REFRESH[1:0] bits in the CONTROL register.

To activate register changes that require a Refresh (any) command, first set the AUTO_REFRESH[1:0] bits to **00b**. This disables Auto-refresh and allows to change registers. Next, issue a manual Refresh (any) command to activate these changes.

Auto-refresh does not trigger when communicating to PAC1811 or another device on the I^2C bus. To ensure that the conversion cycle has completed and there is new data available to read, set up the Conversion Complete alert:

1. In the CONTROL register, set pin A0 or A1 to function as ALERT pin:

   A0 → SLOW_ALERT0[1:0] = **00b**

   A1 → GPIO_ALERT1[1:0] = **00b**
2. Enable the Conversion Complete alert:

   ALERT_ENABLE register → ALERT_CC = **1b**
3. Assign the alert to the A0 or A1 pin:

   A0: SLOW_ALERT0 register → ALERT_CC0 = **1b**

   A1: GPIO_ALERT1 register → ALERT_CC1 = **1b**

The next conversion cycle overwrites the data if not read by the time the new cycle completes.

Note 1: While enabled, Auto-refresh overrules all other refresh commands (Refresh, Refresh_G and Refresh_V).

2: Do not enable Auto-refresh when using Single-shot sample modes.

3: If the CONTROL register no longer corresponds to the CONTROL_ACT register, Auto-refresh halts. It resumes only if both registers match.

4.2.6 SLEEP STATE

The Sleep state is a lower power state than the Active state, during which PAC1811 draws a supply current, I_{SLEEP}, (5 µA, typical) from pin VDD. During this state, registers retain their values and do not reset.

PAC1811 enters the Sleep state when a Refresh or Refresh_V command follows a write to the CONTROL register. PAC1811 exists the Sleep state and resumes sampling only after selecting a new sample mode. To force PAC1811 out of the Sleep state:

1. Select a new sample mode/rate by setting the SAMPLE_MODE[3:0] bits in the CONTROL register. For more details, see Register 6-2.
2. Issue a Refresh or Refresh_V command to apply the new sample mode.

PAC1811 does not enter the Sleep state based on any other parameters, such as static conditions on the SMBus pins. If the SMBus Timeout feature is enabled, it functions in both Sleep and Active states.

To enter Sleep state, set the SAMPLE_MODE[3:0] bits in the CONTROL register to **1110b** or **1111b**.

4.2.7 POWER-DOWN STATE

Note 1: The Power-down state is available only on the **10-Lead VDFN** package.

2: Maximum voltage on this pin is V_{DD}. Do not pull this pin up to voltages that exceed V_{DD}.

The only way to enter the Power-down state is to pull down the $\overline{\text{PWRDN}}$ pin. In this state, all PAC1811 circuits, including the SMBus pins, are inactive and the device is in a state of minimum power dissipation.

In the Power-down state, PAC1811 does not retain any data, be it register configuration or measurement data. When the $\overline{\text{PWRDN}}$ pin is pulled high, sampling, power integration and accumulation resume using the default register settings as described in **Section 4.2.1**.

The initial request for measurement data must be done t_{INT_T} (time to first communications; 20 ms, maximum) after POR with a Refresh or Refresh_V command. POR occurs when V_{DD} exceeds V_{POR} (1.2 V, typical) or when the $\overline{\text{PWRDN}}$ pin is pulled high.

The POR bit in the SMBUS_SETTINGS register is set to **1b** on POR events. To determine that a POR event occurred using this bit, follow these steps:

1. After the initial POR event, clear the POR bit.

2. Poll the SMBUS_SETTINGS register to check if the POR bit is indeed cleared.

3. If the POR bit is set to **1b** when polling the register, then a POR event occurred and PAC1811 requires reprogramming, unless the objective is to operate the device using the default configuration for all registers.

4.2.8 SLOW SAMPLE MODE

Pins A0 and A1 are multifunction pins when pulled to V_{DD} through a resistor. When programming pin A0 or A1 for the Slow sample mode, the selected pin is now considered the SLOW pin. If the SLOW pin is pulled high, PAC1811 samples at 8 sps. Regardless of the configured sample rate, this new Slow sample rate takes effect on the next conversion cycle. If a conversion cycle is in progress when pulling the SLOW pin high, the Slow sample rate takes effect after the current conversion cycle completes.

To configure pin A0 or A1 as the SLOW pin, set the following bit in the CONTROL register:

- A0 → SLOW_ALERT0[1:0] = **11b**
- A1 → GPIO_ALERT1[1:0] = **11b**

Note: While both A0 and A1 pins can be set as SLOW pins, A0 precedes A1. If A0 is set as SLOW pin and pulled high, PAC1811 enters Slow sample mode, regardless how pin A1 is configured or controlled.

4.2.8.1 Interaction with $\overline{\text{ALERT0/1}}$

Pin A0 can function as the $\overline{\text{ALERT0}}$ pin, while pin A1 can operate as the $\overline{\text{ALERT1}}$ pin. If the Alert function is enabled for pin A0 or A1, that pin can no longer control the active conversion.

Alert conditions include overvoltage, undervoltage, overcurrent, undercurrent, overpower, step limit, accumulator overflow and accumulator count overflow. If an alert condition is assigned to the A0 or A1 pin, sampling proceeds at the programmed rate (or the default rate of 1,024 sps if not changed). For more details, see **Section 4.10**.

Note: The same pin (A0 or A1) cannot be set to operate as both SLOW and $\overline{\text{ALERT}}$ pin simultaneously.

To configure pin A0 or A1 as an $\overline{\text{ALERT}}$ pin, set the following bit in the CONTROL register:

- A0 → SLOW_ALERT0[1:0] = **00b**
- A1 → GPIO_ALERT1[1:0] = **00b**

If pin A0 or A1 is set to operate as $\overline{\text{ALERT}}$ pin and not as SLOW pin, the Slow sample rate of 8 sps can be selected by setting the SAMPLE_MODE[3:0] bits in the CONTROL register to **0101b**. Other sample rates are available. For more details, see Register 6-2.

If PAC1811 operates in one of the Single-shot sample modes and the SLOW pin is pulled high, sampling starts one band gap start-up cycle after the SLOW pin is pulled high. This lasts for approximately 5 ms.

If PAC1811 is in the Sleep state, pulling the SLOW pin high does not trigger the device to initiate sampling.

Whenever the SLOW pin is pulled high, PAC1811 itself can execute a Limited Refresh or Refresh_V command; default is Refresh. The Limited Refresh or Refresh_V command behaves like its counterpart, except that programmed changes to the configuration or status registers do not take effect. Data registers are updated and are ready-to-read within one conversion cycle after the SLOW pin transition.

The SLOW register allows to:

- Select between issuing a Limited Refresh or Refresh_V command on SLOW pin transitions.
- Enable or disable Limited Refresh or Refresh_V commands for either signal edge of the SLOW pin.
- Track the state of the SLOW pin and its transitions. For details, see Register 6-23.

Note: If the Adaptive Accumulator function is enabled while PAC1811 is sampling, the bits in the SLOW register that control Limited Refresh/Refresh_V commands are set to **0b** by default. These bits can be set so that Limited Refresh/Refresh_V commands still occur. For details, see **Section 4.8.1** and Register 6-23.

4.2.9 OPERATION OF SAMPLE MODES 1010B AND 1011B

PAC1811 has multiple sample modes available for selection. Among them, there are two sample modes that lock the ADC to a specific input:

- Sample mode **1010b** only samples input V_{BUS} at 16,384 sps
- Sample mode **1011b** only samples input V_{SENSE} at 16,384 sps

4.2.9.1 Sample Mode 1010b

While operating in sample mode **1010b**, PAC1811 only measures V_{BUS} and not V_{SENSE}. However, the device uses the last available V_{SENSE} value to approximate V_{POWER}. The newly measured V_{BUS} value and the last available V_{SENSE} value are multiplied together to produce a quasi-V_{POWER} result. This result can be used as an estimate of the actual V_{POWER} value. PAC1811 also uses this result to update V_{POWER} registers, including VPOWER, VPOWER_MIN and VPOWER_MAX.

Registers associated with V_{SENSE}, including VSENSE, VSENSE_AVG, VSENSE_MIN and VSENSE_MAX, keep their most recent valid results even after a Refresh (any) command occurs.

The accumulator operates as normal. No registers are skipped over during auto-incrementing.

4.2.9.2 Sample Mode 1011b

While operating in sample mode **1011b**, PAC1811 only measures V_{SENSE} and not V_{BUS}. However, the device uses the last available V_{BUS} value to approximate V_{POWER}. The newly measured V_{SENSE} value and the last available V_{BUS} value are multiplied together to produce a quasi-V_{POWER} result. This result can be used as an estimate of the actual V_{POWER} value. PAC1811 also uses this result to update V_{POWER} registers, including VPOWER, VPOWER_MIN and VPOWER_MAX.

Registers associated with V_{BUS}, including VBUS, VBUS_AVG, VBUS_MIN and VBUS_MAX, keep their most recent valid result even after a Refresh (any) command occurs.

The accumulator operates as normal. No registers are skipped over during auto-incrementing.

4.2.10 USING THE A0/A1 PINS AS I/O PINS

Pins A0 and A1 can be used as General Purpose Input/Output (GPIO) pins. Enable this functionality in the CONTROL register:

- Pin A0:
  - GPIO digital input → SLOW_ALERT0[1:0] = **01b**
  - GPIO digital output → SLOW_ALERT0[1:0] = **10b**
- Pin A1:
  - GPIO digital input → GPIO_ALERT1[1:0] = **01b**
  - GPIO digital output → GPIO_ALERT1[1:0] = **10b**

The SMBUS_SETTINGS register holds input data to read and output data to write when A0/A1 is GPIO pin:

- GPIO_DATA0 bit for pin A0
- GPIO_DATA1 bit for pin A1

Note: GPIO_DATA0 and GPIO_DATA1 are read when A0/A1 function as GPIO inputs and written when A0/A1 are as GPIO outputs.

4.3 Voltage Measurement

PAC1811 measures the following voltages:

- V_{BUS}:
  - 8-Lead VDFN: across pin VSENSE+ to GND
  - 10-Lead VDFN: across pin VBUS+ to GND
- V_{SENSE} between the VSENSE+ and VSENSE– pins

Measurements can be unsigned full range, signed full range or signed half range 16-bit values, depending on NEG_PWR_FSR register settings. ADC internal values for V_{BUS} and V_{SENSE} are multiplied together and result in V_{POWER}. This V_{POWER} result is then summed into the accumulator. VACC is the Accumulator register and it can be programmed to accumulate different results depending on the settings of the CONTROL register:

- Accumulate V_{BUS} results → CONFIG[1:0] = **10b**
- Accumulate V_{SENSE} results → CONFIG[1:0] = **01b**
- Accumulate V_{POWER} results → CONFIG[1:0] = **00b**

By default, the VACC register accumulates V_{POWER} results. For details, see Register 6-2 and Register 6-4.

The default Full Scale Range (FSR) for PAC1811 is 0V to 42V. The device can be programmed for bipolar V_{BUS} measurements. In this bipolar mode, the mathematical range for V_{BUS} results is ±42V, while the actual range is limited to approximately -200 mV to +42V due to physical factors. Bipolar mode enables accurate V_{BUS} offset measurements. While PAC1811 operates in bipolar mode, 16-bit V_{BUS} measurements are 2's complement signed numbers.

Calculate the actual value of V_{BUS} using Equation 4-1.

EQUATION 4-1

$$LSB(V_{BUS}) = \frac{FSV_{BUS}}{2^{16}}$$

$$V_{BUS} = LSB(V_{BUS}) \times CONV(VBUS)$$

Where:

- V_{BUS} = Bus Voltage (V)
- $LSB(V_{BUS})$ = LSBs of the V_{BUS} measurement
- FSV_{BUS} = Full Scale Voltage for V_{BUS} (V):
  - 42V for Unipolar mode
  - 84V for Bipolar mode
  - 42V for Bipolar FSR/2 mode
- 2^{16} = 16-bit ADC Resolution
- $CONV(VBUS)$ = Converted analog-to-digital value, from hexadecimal to decimal, read from the VBUS register

Note: FSR/2 mode can be used to reduce FSR. For more details, see **Section 4.6**.

4.4 Current Measurement

PAC1811 includes a high-side current sensing circuit that measures the voltage (V_{SENSE}) induced across a fixed external current shunt resistor (R_{SHUNT}). It then stores the measured value as a 16-bit number in the VSENSE register.

By default, PAC1811 operates in unipolar current mode with a FSR of 0 to 100 mV. When sensing unipolar currents, ADC results are in unsigned binary format.

For bipolar current mode, FSR changes to ±50mV or ±100 mV. When sensing bipolar currents, ADC results are in 2's complement signed format.

Note: For best accuracy when sampling current values near zero, Microchip recommends using bipolar mode and 8x average current results. For more details, see Register 6-2.

4.5 Selecting R_{SHUNT} Values

R_{SHUNT} can be calculated only when the maximum current to sense, I_{MAX}, is known. First determine I_{MAX} and then use Equation 4-2 to calculate R_{SHUNT}.

Note: Consider that the value selected for I_{MAX} needs to include current peaks beyond nominal current.

EQUATION 4-2

$$R_{SHUNT} = \frac{|FSV_{SENSE}|}{I_{MAX}}$$

Where:

- R_{SHUNT} = External Shunt Resistor (Ω)
- $|FSV_{SENSE}|$ = Full Scale Voltage for V_{SENSE} (V), absolute value:
  - 100 mV for Unipolar mode
  - 100 mV for Bipolar mode
  - 50 mV for Bipolar FSR/2 mode
- I_{MAX} = Maximum Current to Measure (A)

Determine the value of I_{SENSE} using Equation 4-3.

EQUATION 4-3

$$I_{SENSE} = \frac{V_{SENSE}}{R_{SHUNT}}$$

Where:

- I_{SENSE} = Sense Current (mA)
- V_{SENSE} = Sense Voltage (mV)
- R_{SHUNT} = External Shunt Resistor (Ω)

Use Equation 4-4 to calculate the real value of V_{SENSE}.

EQUATION 4-4

$$LSB(V_{SENSE}) = \frac{FSV_{SENSE}}{2^{16}}$$

$$V_{SENSE} = LSB(V_{SENSE}) \times CONV(VSENSE)$$

Where:

- V_{SENSE} = Sense Voltage (V)
- $LSB(V_{SENSE})$ = LSBs of the V_{SENSE} measurement
- FSV_{SENSE} = Full Scale Voltage for V_{SENSE} (V):
  - 100 mV for Unipolar mode
  - 200 mV for Bipolar mode
  - 100 mV for Bipolar FSR/2 mode
- 2^{16} = 16-bit ADC Resolution
- $CONV(VSENSE)$ = Converted analog-to-digital value, from hexadecimal to decimal, read from the VSENSE register

4.6 FSR/2 Modes

FSR/2 mode allows the use of a reduced FSR. This can be divided by a factor of two for V_{SENSE} and/or V_{BUS} and it can be selected for both voltages by configuring the NEG_PWR_FSR register:

- V_{BUS} → CFG_VB[1:0] = **10b**
- V_{SENSE} → CFG_VS[1:0] = **10b**

TABLE 4-1: FSR/2 – V_{BUS}

V_{BUS} Range	FSR = 42V, FSR/2 = 21V
Unipolar 0-FSR	0.641 mV/LSB
Bipolar ± FSR	1.28 mV/LSB
Bipolar ± FSR/2	0.641 mV/LSB

TABLE 4-2: FSR/2 – V_{SENSE}

V_{SENSE} Range	FSR = 100 mV, FSR/2 = 50 mV
Unipolar 0-FSR	1.53 µV/LSB
Bipolar ± FSR	3.05 µV/LSB
Bipolar ± FSR/2	1.53 µV/LSB

4.7 ADC Measurements, Offset and Averaging

PAC1811 is primarily used for energy measurements where many power calculations are accumulated. This is inherently an averaging process. Individual voltage and current measurements can also benefit from averaging to reduce noise. The averaged values are internally calculated for V_{BUS} and V_{SENSE}.

Rolling averages of the most recent samples are stored in the VBUS_AVG and VSENSE_AVG registers. The rolling averages update internally after every complete conversion cycle, while readable registers are updated using Refresh (any) commands. Use these averaged results to obtain the most accurate, lowest noise measurements.

Results from both V_{BUS} and V_{SENSE} ADCs are 16-bit 2's complement signed numbers. Conversion results are stored as unipolar or bipolar numbers based on NEG_PWR_FSR register settings. Besides measuring bipolar currents (charging/discharging) and voltages that can drop below ground level, bipolar numbers can give more accurate results for very small values that may actually be negative for some readings. For more details, see Register 6-20.

Note: Using the full resolution of the device can impact NEG_PWR_FSR register settings. For example, if conversion results are stored as unipolar numbers and a negative value is converted, the average result includes the signed negative value and produces a different value than just averaging the VBUS or VSENSE register.

PAC1811 calculates the mean value for both V_{BUS} and V_{SENSE} by averaging the most recent voltage samples. The number of samples (measurements) included in the rolling average is determined by the AVERAGE[2:0] bits in the CONTROL register. By default, these bits are set to **001b**, equivalent to using the most recent eight measurements to determine rolling averages.

PAC1811 stores the rolling averages of the most recent V_{BUS} and V_{SENSE} samples in the VBUS_AVG and VSENSE_AVG registers. After POR, these registers start representing accurate voltage averages only after the minimum required number of samples/completed conversion cycles is reached. Set the AVERAGE[2:0] bits in the CONTROL register so that PAC1811 uses the most recent 4, 8, 16, 32, 64 or 128 samples when calculating the rolling V_{BUS} and V_{SENSE} averages. For more details, see Register 6-2.

The VBUS_AVG and VSENSE_AVG registers update after every completed conversion cycle. Refresh (any) commands update these registers like any readable register. For details, see Register 6-7 and Register 6-8.

The AVERAGE[2:0] bits in the CONTROL register determine how many samples are included in a rolling average. When this setting changes, PAC1811 resets the averaging registers. This results in the VBUS_AVG and VSENSE_AVG registers to be incorrect until the new set number of samples is performed. For example, if the average is set to require 64 samples, PAC1811 reports the correct value only after 64 new samples are taken. PAC1811 negatively acknowledges (NACK) all register reads of VBUS_AVG and VSENSE_AVG until the set number of samples is reached.

Note: During a Bulk Read action, the incorrect value is read without an opportunity to NACK.

4.8 Power and Energy

Power calculations (V_{POWER}) result in 32-bit numbers obtained by multiplying together 16-bit voltage values and 16-bit current values:

$$V_{POWER} = V_{BUS} \times V_{SENSE}$$

The Full Scale Range for Power (FSR_P) depends on the value of R_{SHUNT}, as Equation 4-5 shows.

EQUATION 4-5

$$FSR_P = \frac{FSV_{BUS} \times FSV_{SENSE}}{R_{SHUNT}}$$

Where:

- FSR_P = Full Scale Range for Power (V)
- FSV_{BUS} = Full Scale Voltage for V_{BUS} (V):
  - 42V for Unipolar mode
  - 84V for Bipolar mode
  - 42V for Bipolar FSR/2 mode
- FSV_{SENSE} = Full Scale Voltage for V_{SENSE} (V):
  - 100 mV for Unipolar mode
  - 200 mV for Bipolar mode
  - 100 mV for Bipolar FSR/2 mode
- R_{SHUNT} = External Shunt Resistor (Ω)

V_{POWER} results are digitally accumulated in the VACC register. For more details, see Register 6-4.

Bipolar mode for energy applies when bipolar mode is used for V_{BUS} and/or V_{SENSE}.

PAC1811 implements power measurements through $V_{POWER} = V_{BUS} \times V_{SENSE}$. The actual power is the power measured in one sample and is calculated as shown in Equation 4-6.

EQUATION 4-6

$$P_{Actual} = FSR_P \times \frac{CONV(VPOWER)}{2^{32}}$$

Where:

- P_{Actual} = Actual Power (W)
- FSR_P = Full Scale Range for Power (V)
- $CONV(VPOWER)$ = Converted digital value, from hexadecimal to decimal, read from the VPOWER register
- 2^{32} = VPOWER Register Size (bits)

Equation 4-7 shows how to calculate energy using the accumulator results, the accumulator count and the accumulation period (t_{ACC}).

Note: PAC1811 internal oscillator variations can introduce an additional error source of up to 1%. To remove the error source, use a host clock to determine timing.

EQUATION 4-7

$$E = \frac{CONV(VACC)}{2^{32}} \times FSR_P \times \frac{t_{ACC}}{AccCount}$$

Where:

- E = Energy (J)
- $CONV(VACC)$ = Converted digital value, from hexadecimal to decimal, read from the VACC register
- 2^{32} = VPOWER Register Size (bits)
- FSR_P = Full Scale Range for Power (W)
- t_{ACC} * = Accumulation Period (s)
  - * must be generated by host clock
- $AccCount$ = Accumulator Count

Equation 4-8 shows how to calculate energy using the accumulated power and the sample rate (sampling frequency), f_S. For this calculation, consider f_S as measured in Hz instead of sps.

EQUATION 4-8

$$E = \frac{CONV(VACC)}{2^{32}} \times \frac{FSR_P}{f_S}$$

Where:

E	=	Energy (J)
$CONV(VACC)$	=	Converted digital value, from hexadecimal to decimal, read from the VACC register
2^{32}	=	VPOWER Register Size (bits)
FSR_P	=	Full Scale Range for Power (W)
f_S	=	Sample Rate (Hz)

4.8.1 ADAPTIVE ACCUMULATOR

In Adaptive Accumulator (AA) mode, regardless of the selected f_S, PAC1811 accumulates samples at the equivalent rate of 8,192 sps. For example, after the SLOW pin is pulled high, if PAC1811 begins sampling at a programmed rate of 8 sps (Slow mode), the samples taken are shifted to the left by an appropriate amount and accumulated. This is done to simulate sampling as if f_S is set to the maximum of 8,192 sps. To achieve the simulated sample rate in AA mode, the accumulator count is also incremented by the appropriate amount for each sample taken while PAC1811 operates in Slow mode.

AA mode provides a big reduction in host overhead and bus traffic for applications that require to:

1. Use the SLOW pin for low power operation during specific times
2. Have continuous accurate energy monitoring for both the maximum and Slow sample rates

As shown in Equation 4-7 and Equation 4-8, it is necessary to know the sample rate (f_S) and sampling period (t_S) for each interval during which energy is accumulated. If the SLOW pin is pulled high and t_S changes, the host must read accumulator data and determine the accumulator value and accumulator count every time f_S changes. While operating in AA mode, the host needs to read accumulator data only once, just before the accumulator and/or accumulator count overflows. Using AA mode, PAC1811 accurately calculates the accumulated energy, independent of how many times the SLOW pin was pulled high and low during t_S.

The SLOW register offers a variety of options to monitor when the SLOW pin transitions or when the Slow function is active. This includes issuing Refresh (any) and Limited Refresh commands. This behavior is controlled by setting the appropriate bits in the SLOW register. For more details, see Register 6-23.

While AA mode is enabled, if f_S is configured to any other value than 8,192 sps, registers VACC and ACC_COUNT shift the accumulator data and count to mimic sample accumulation at the maximum sampling rate of 8,192 sps. Adaptive Accumulator mode is enabled by setting the AA bit in the CONTROL register to **1b**. For more details, see Register 6-2.

4.8.2 ADDITIONAL ACCUMULATOR INFORMATION

Power calculation and accumulation inside PAC1811 are always done using 2's complement, regardless of what the output registers are set to show. Internally, V_{BUS} and V_{SENSE} are 16-bit 2's complement signed numbers. V_{POWER} is calculated by multiplying V_{SENSE} and V_{BUS}, resulting in a 32-bit 2's complement signed number. In some cases, while the 32-bit V_{POWER} result is not identical to the product of the VBUS register multiplied by the VSENSE register, the V_{POWER} result is more accurate.

The FSR for V_{BUS} or V_{SENSE} measurements is set in the NEG_PWR_FSR register using the CFG_VB[1:0] and CFG_VS[1:0] bits. For details, see Register 6-20.

If FSR for both V_{SENSE} and V_{BUS} measurements is set to unipolar mode, these measurements are stored in the VBUS and VSENSE registers as 16-bit unsigned numbers.

If FSR for V_{BUS} and V_{SENSE} sampling is set to bipolar mode, the measurement results are stored in the VBUS and the VSENSE registers as 16-bit 2's complement signed numbers.

However, V_{POWER} calculations use 16-bit 2's complement signed values. Therefore, a mismatch is possible between an externally calculated power value (where $V_{POWER} = V_{BUS} \times V_{SENSE}$) and the actual power value determined by PAC1811. This internal value is more accurate than the externally calculated power. This also applies to FSR/2 modes that use bit shifting to change the FSR. Therefore, accuracy is not lost during power calculations (similar to unipolar mode).

Continuous power integration periods, also called energy accumulation periods, range from ~ 1 ms to several hours, depending on the programmed f_S. The total number of samples is limited by the size of the ACC_COUNT register to 4,294,967,296 or 2^{32}. The count corresponds to about 1,165 hours at 1,024 sps or approximately 17 years at 8 sps.

Note: The VACC and ACC_COUNT registers saturate when reaching their maximum value. They do not roll over and do not reset until cleared. This is called accumulator overflow. The VACC_PRESET register allows to set a base level for the VACC register so it starts at the preset level any time a Refresh or Refresh_G command is sent. For more details, see Register 6-3 and Register 6-4.

To read and/or reset the VACC and ACC_COUNT registers before they overflow, calculate the worst-case time when these registers roll over or set a fullness limit using the ACC_FULL_LIMIT register.

PAC1811 compares the 6 MSBs of the VACC register, while ignoring its LSBs, to the ACC_FULL[5:0] bits in the ACC_FULL_LIMIT register. It triggers an alert if the 6 MSBs of the VACC register exceed the set limit. The ACC_FULL_LIMIT register can also limit accumulator count to 3/4 (75%), 7/8 (~ 87%), 15/16 (~ 93%) or 100% full. For more details, see Register 6-28.

Calculate the worst-case accumulator overflow time assuming that every accumulated measurement is a full scale number. Since the values stored in the VPOWER register are 32 bits and the accumulator uses 56 bits, up to 2^{24} full scale samples can be summed before overflow. For most applications, the samples are not all full scale numbers, especially if V_{BUS} is very small compared to the maximum V_{BUS} for PAC1811. If the maximum V_{BUS} of the system is always lower than the FSR for V_{BUS}, the maximum number of full scale samples that can be accumulated is scaled by FSR/maximum V_{BUS}. If both V_{BUS} and V_{SENSE} values are always near full scale, this can limit the accumulation period (t_{ACC}) before overflow to 1,092 minutes at 8,192 sps or 233 hours at 8 sps.

Note: The Accumulator Count does not limit the number of samples that can be accumulated and counted.

4.8.3 ALTERNATIVE USES FOR THE ACCUMULATOR

The VACC register can be used to accumulate V_{SENSE} or V_{BUS} values instead of V_{POWER} values. This is done by setting the ACC_CONFIG[1:0] bits in the CONTROL register. For more details, see Register 6-2.

Configuring the VACC register to accumulate V_{SENSE} values provides a measure of accumulated current, which is the same thing as charge. This allows the VACC register to be used as a Coulomb Counter.

For either V_{SENSE} or V_{BUS}, many samples can be accumulated on PAC1811. The host first reads the VACC and ACC_COUNT registers. It then divides the accumulator value by the accumulator count to provide an average value with a very long integration time and reduced noise. This feature is also useful for testing, allowing many averages to accumulate for fast and easy averaging/noise reduction. Test time can be further reduced by combining this with higher sample rates.

Note: If a Refresh_V command changes the accumulation type (V_{POWER}, V_{BUS} or V_{SENSE}), the VACC register does not reset and the data it collected up to that moment persists. To avoid this issue, use a Refresh command when changing the accumulation type.

4.9 Conversion Cycles

A conversion cycle for PAC1811 consists of an analog-to-digital conversion for V_{BUS} or V_{SENSE}. The device performs data conversion and processing in sequence:

1. It samples V_{BUS} and V_{SENSE}
2. Converts V_{BUS} and V_{SENSE} results from analog to digital values
3. Calculates $V_{POWER} = V_{BUS} \times V_{SENSE}$
4. And then accumulates V_{POWER} results in the VACC register and increments the ACC_COUNT register

This sequence of operations completes the conversion cycle and the following registers update afterward:

- VBUS_MIN and VBUS_MAX
- VSENSE_MIN and VSENSE_MAX
- VBUS_AVG and VSENSE_AVG
- VPOWER_MIN and VPOWER_MAX
- ALERT_STATUS

Note: Only the internal registers update during conversion cycles. Readable registers update only when issuing a Refresh (any) command or while Auto-refresh is enabled.

A special configuration is available to only sample V_{BUS} or V_{SENSE} (sample modes **1010b** and **1011b**, respectively). This speeds up the conversion cycle by 50%. For more details, see **Section 4.2.9**.

Switching between sample modes during the middle of a conversion results in the ADC continuing the previous sample mode. It changes to the new sample mode only after the current conversion cycle completes.

When switching to Single-shot mode, any triggers are ignored until the conversion cycle is complete. When changing from a continuous sample mode to Single-shot mode, an extra conversion occurs. The extra conversion does not occur when switching between continuous sampling or between various Single-shot operational modes.

4.9.1 SINGLE-SHOT MODE

In Single-shot mode, PAC1811 samples and converts V_{BUS} and V_{SENSE} measurements and then calculates V_{POWER}. These actions are done in a single sequence.

Note 1: First enter Sleep state and then switch to the desired Single-shot mode. This resolves any situations where the current conversion cycle impacts the accumulator count. For details on the Sleep state, see **Section 4.2.6**.

2: If PAC1811 enters Single-shot Awake mode from either the low-power state or from another Single-shot mode, the initial Single-shot Awake conversion adds a wake-up delay that allows the internal digital logic to fully exit the low-power state.

3: After entering Single-shot mode, the first refresh-type command issued must be a Refresh. Do not issue a Refresh_V or Refresh_G instead of a Refresh command.

By default, PAC1811 operates in continuous 1,024 sps sample mode. To switch to Single-shot mode, set the following bits in the CONTROL register:

1. Enter the Sleep state:

   SAMPLE_MODE[3:0] = **1110b** or **1111b**

2. Switch to the Single-shot mode:

   SAMPLE_MODE[3:0] = **0110b**

After completing the single-shot measurements and calculations, PAC1811 enters the Sleep state. Issue a Refresh (any) command to read the most recent data.

Note: After issuing a Refresh (any) command, wait for a conversion cycle to complete before starting the next single-shot conversion.

Generally, single-shot conversion commands are not issued one after the other. Replace single-shot conversions with a continuous sample rate in scenarios where conversions need to occur in short succession.

4.9.1.1 Single-shot Average Mode

In Single-shot Average mode, PAC1811 issues a single Refresh command to collect the programmed number of V_{BUS} or V_{SENSE} samples. The gathered samples are averaged and the result is stored in the VBUS_AVG or VSENSE_AVG register, while the VBUS and VSENSE registers hold the most recent results of the V_{BUS} and V_{SENSE} conversions. Averaging reduces noise and offset in the result. In this mode, all averaged samples are added to the accumulator, while the accumulator count is incremented by the configured amount each time a Refresh command triggers another single-shot average acquisition and conversion.

To enter Single-shot Average mode from the Sleep state, set the following bits in the CONTROL register:

- SAMPLE_MODE[3:0] = **0111b**

4.9.1.2 Single-shot Awake Mode

In Single-shot Awake mode, PAC1811 does not enter Sleep state after the conversion cycle completes. This results in a higher quiescent current, but allows PAC1811 to start converting samples much faster after it receives the command to initiate the conversion.

To enter Single-shot Awake mode from the Sleep state, set the following bits in the CONTROL register:

- SAMPLE_MODE[3:0] = **1000b**

4.9.1.3 Single-shot Awake Average Mode

The Single-shot Awake Average mode works similarly to Single-shot Awake mode, but with PAC1811 taking the programmed amount of samples to average.

See **Section 4.9.1**, **Note 2**.

To enter Single-shot Awake Average mode from the Sleep state, set the following bits in the CONTROL register:

- SAMPLE_MODE[3:0] = **1001b**

4.9.1.4 GPIO Triggered Single-shot Awake Mode

In General Purpose Input/Output (GPIO) Triggered Single-shot Awake mode, PAC1811 can use pin A0 or A1 as a GPIO input to signal the start of a conversion. This mode is similar to the Single-shot Awake mode in that PAC1811 does not enter into any low power state and thus has a fast reaction time when triggered. The time-limiting factor is the internal 16 kHz oscillator that monitors the A0/A1 inputs.

Note: The A0/A1 pin must be configured as GPIO input for the trigger to occur and the signal must be active high. For details, see **Section 4.2.10**.

GPIO Triggered Single-shot Awake mode activates when the GPIO pin is pulled and held low for longer than 250 µs. This triggers the single-shot sample.

I²C Triggered Single-shot mode is also available. It is used with a Refresh (any) command. Accumulator and accumulator count operate the same as for continuous conversion, summing every single-shot power calculation and incrementing the accumulator count. The conversion cycle starts when the GPIO edge is sent or when a Refresh (any) command is issued.

To enter GPIO Triggered Single-shot Awake mode from the Sleep state, set the following bits in the CONTROL register:

- A0 → SAMPLE_MODE[3:0] = **1100b**
- A1 → SAMPLE_MODE[3:0] = **1101b**

4.10 Alert Functionality

If enabled, the Alert functionality notifies when:

- A conversion cycle completes
- The accumulator or accumulator count overflows
- An electrical parameter exceeds the set limit
- The rolling average of the most recent V_{BUS} or V_{SENSE} samples changes by more than expected

Depending on the configuration, alerts trigger either the A0 pin or the A1 pin to be pulled low and latched low. The only exception is the Conversion Complete alert, when a 5 µs pulse of the $\overline{\text{ALERT}}$ pin occurs. Alerts are set at the end of conversion cycles.

4.10.1 $\overline{\text{ALERT}}$ PIN ASSIGNMENTS

Before assigning any alerts, pin A0, pin A1 or both must be set to function as $\overline{\text{ALERT}}$ pins by programming the CONTROL register:

- A0 → SLOW_ALERT0[1:0] = **00b**
- A1 → GPIO_ALERT1[1:0] = **00b**

> **Note:** The Slow function is disabled if the Alert function is programmed on the same pin.

After configuring pin A0/A1 to function as $\overline{\text{ALERT}}$ pin, assign alerts to the pin using the SLOW_ALERT0 register for A0 and the GPIO_ALERT1 register for A1. For details, see Register 6-26 and Register 6-27.

When an active alert triggers, except the Conversion Complete alert, PAC1811 sets the ANY_ALERT bit in the SMBUS_SETTINGS register to **1b**. Monitor this bit over I²C, SMBus or on pin A0/A1 to determine if an alert was triggered. Clearing the alert that set the bit also clears the ANY_ALERT bit.

> **Note:** The SMBUS_SETTINGS register updates without requiring a Refresh (any) command. For more details, see Register 6-19.

4.10.2 CONVERSION COMPLETE ALERT

When the Conversion Complete (CC) alert is enabled, the assigned $\overline{\text{ALERT}}$ pin is pulled and held low for 5 µs after each completed conversion cycle.

To enable the Conversion Complete alert function on the $\overline{\text{ALERT}}$ pin, follow the next steps:

1. Program pin A0/A1 as $\overline{\text{ALERT}}$ pin(s) in the CONTROL register:
   - A0 → SLOW_ALERT0[1:0] = **00b**
   - A1 → GPIO_ALERT1[1:0] = **00b**
2. Enable the Conversion Complete alert:

   ALERT_ENABLE register: ALERT_CC = **1b**
3. Assign the alert to the A0/A1 pin:
   - If A0 is set as $\overline{\text{ALERT}}$ pin → SLOW_ALERT0 register: ALERT_CC0 = **1b**
   - If A1 is set as $\overline{\text{ALERT}}$ pin → GPIO_ALERT1 register: ALERT_CC1 = **1b**

Use the CC alert to read data continuously as soon as each conversion cycle is complete. For more details, see Register 6-26 and Register 6-27.

> **Note 1:** Jitter caused by the low power clocking scheme can be present when viewing the Conversion Complete alert. This does not impact the conversion cycle.
>
> **2:** The Conversion Complete alert does not impact the ALERT_STATUS register. For more details, see Register 6-18.

4.10.3 ALERT FUNCTIONALITY – VOLTAGE, CURRENT AND POWER

The Alert functionality enables the detection of voltage and current events that equal or exceed programmable limits, for one or more samples. To monitor alert status, set pin A0/A1 to correspond to a single specific alert or to multiple alerts by programming the corresponding bits in the SLOW_ALERT0 register for pin A0 and the GPIO_ALERT1 register for pin A1. For more details, see Register 6-26 and Register 6-27.

Alert status can also be monitored over SMBus or I²C by reading the ALERT_STATUS register. For more details, see Register 6-18.

Alerts can be triggered by various events:

- V_{BUS} overvoltage or undervoltage
- V_{SENSE} overcurrent or undercurrent
- Fast rising or falling voltage or current
- Overpower warning or overpower critical
- Conversion cycle complete
- Accumulator or accumulator count hitting a limit for fullness or overflow

> **Note:** Over limits trigger when voltage or current exceeds its set limit, while under limits trigger when voltage or current drops below its set limit.

To enable the following alerts, set the corresponding bits in the ALERT_ENABLE register:

- Overvoltage and undervoltage alerts
- Overcurrent and undercurrent alerts
- Overpower alerts
- Rising and falling voltage and current alerts
- Accumulator and accumulator count alerts

For more details on enabling alerts, see Register 6-37.

Accumulator fullness limits are 2's complement values, regardless if unipolar or bipolar mode is used for V_{BUS} and V_{SENSE} sampling. The ACC_FULL_LIMIT register sets the accumulator and accumulator count fullness and overflow limits. For details, see Register 6-28.

Note 1: Only the alert conditions set in the ALERT_ENABLE register are capable of triggering alerts. For more details, see Register 6-37.

2: The ALERT_STATUS register displays only enabled alerts. For more details, see Register 6-18.

4.10.4 ALERT THRESHOLD LIMITS

Overvoltage, undervoltage, overcurrent, undercurrent, overpower, rising and falling voltage and current events trigger an alert only when the monitored parameter is outside its set limits.

The registers for overcurrent (OC), undercurrent (UC), overvoltage (OV), undervoltage (UV) and step limits use 8 bits. PAC1811 compares the 8-bit limits (2's complement) to the first 8 MSBs of the corresponding data 16-bit register.

The registers for overpower (OP) warning and critical limits use 16 bits. PAC1811 compares the 16-bit limits to the first 16 MSBs of the 32-bit VPOWER register.

Step limits are used to detect large changes in the most recent conversion when compared to the appropriate average register.

The alert thresholds are set in the following registers:

- OC_LIMIT – Register 6-29
- UC_LIMIT – Register 6-30
- OP_WARNING_LIMIT – Register 6-31
- OP_CRITICAL_LIMIT – Register 6-32
- OV_LIMIT – Register 6-33
- UV_LIMIT – Register 6-34
- STEP_LIMIT – Register 6-35

4.10.5 SAMPLES OVER LIMIT TO TRIGGER ALERT

The N-SAMPLES_LIMIT register can be programmed to specify how many consecutive samples must be outside their configured limits before triggering an Alert condition. For more details, see Register 6-36.

For overcurrent, overvoltage and overpower events, exceeding the set threshold implies the measurement is over the programmed limit. For undercurrent and undervoltage, not exceeding the set threshold implies the measurement is under the programmed limit. Both events trigger an Alert condition.

When thresholds are negative, it implies that negative numbers with large magnitudes trigger overcurrent, overvoltage and overpower events, while negative numbers with small magnitudes trigger undercurrent and undervoltage events.

When sampling, PAC1811 detects if a measurement is outside its programmed limits. By default, the number of consecutive over limit detections that is required to trigger the corresponding alert is 1, resulting in an alert that occurs on the first sample that is not within the set threshold. To change the number of consecutive over limit detections required to trigger an alert, set the appropriate bits in the N-SAMPLES_LIMIT register.

4.10.6 ACCUMULATOR-BASED ALERTS

The Alert function can be programmed to trigger when the VACC and/or ACC_COUNT registers are filled to or beyond a specified limit.

By default, the VACC register stores the accumulated sum of V_{POWER} calculations. It can be programmed to accumulate V_{BUS} or V_{SENSE} measurements instead.

PAC1811 compares the ACC_FULL[5:0] bits of the ACC_FULL_LIMIT register with the 6 MSBs of the VACC register. It determines if the accumulator has exceeded its fullness limit and triggers the Accumulator Full alert, if applicable.

Note: The maximum value that can be stored in the ACC_FULL[5:0] bits is **111111b**. Do not use this value as the Accumulator Full limit. Since this is the maximum value, it cannot be exceeded and thus, no alert is triggered. Use **111110b** as the maximum Accumulator Full limit.

The ACC_COUNT register stores the total number of results accumulated in the VACC register. The Accumulator Count Full limit determines the threshold beyond which the ACC_COUNT register is considered full and an alert condition triggers.

The Accumulator Count Full limit can be programmed for the ACC_COUNT register to one of the following options by configuring the ACC_FULL_LIMIT register:

- 3/4 (75%) full → ACC_COUNT_FULL[1:0] = **11b**
- 7/8 (~87%) full → ACC_COUNT_FULL[1:0] = **10b**
- 15/16 (~93%) full → ACC_COUNT_FULL[1:0] = **01b**
- 100% full → ACC_COUNT_FULL[1:0] = **00b**

This allows maximizing the accumulation period, t_{ACC}. The Accumulator and Accumulator Count Full limits are specified in the ACC_FULL_LIMIT register. For more details, see Register 6-28.

Whenever an alert occurs, read the ALERT_STATUS register to determine the cause: a conditional threshold or the accumulator or accumulator count fullness limit. Alert conditions are cleared when the register is read, specifically when the bit that caused the specific alert event is read.

The ALERT_STATUS register is updated immediately upon detecting an alert event, as it does not require a Refresh (any) command.

When accumulator overflow occurs and triggers the Alert function, the alert condition is cleared and the Alert function resets only after issuing a Refresh or Refresh_G command.

Note:	Refresh_V commands do not clear the alert condition or reset the Alert function.

4.10.7 ALERT CLEARING AND PERSISTENT FAULT CONDITIONS

When an alert event occurs and the alert triggers, this is recorded in the ALERT_STATUS register. PAC1811 sets the bit corresponding to the alert type to **1b**.

To clear the ALERT_STATUS register after an alert occurred, read the register. If the alert condition is still present after the next conversion cycle completes, the alert condition is reasserted.

If the overvoltage, undervoltage, overcurrent, undercurrent, overpower, accumulator or accumulator count full conditions that triggered an alert persist after the ALERT_STATUS register is read, the Alert function is reasserted if the next converted sample exceeds the set threshold.

5.0 SMBUS AND I²C COMMUNICATIONS PROTOCOLS

PAC1811 communicates over a two-wire bus with a Controller using SMBus or I²C. Figure 5-1 shows a detailed SMBus timing diagram.

Stretching of the SMBus clock signal is supported. However, PAC1811 does not stretch the clock signal.

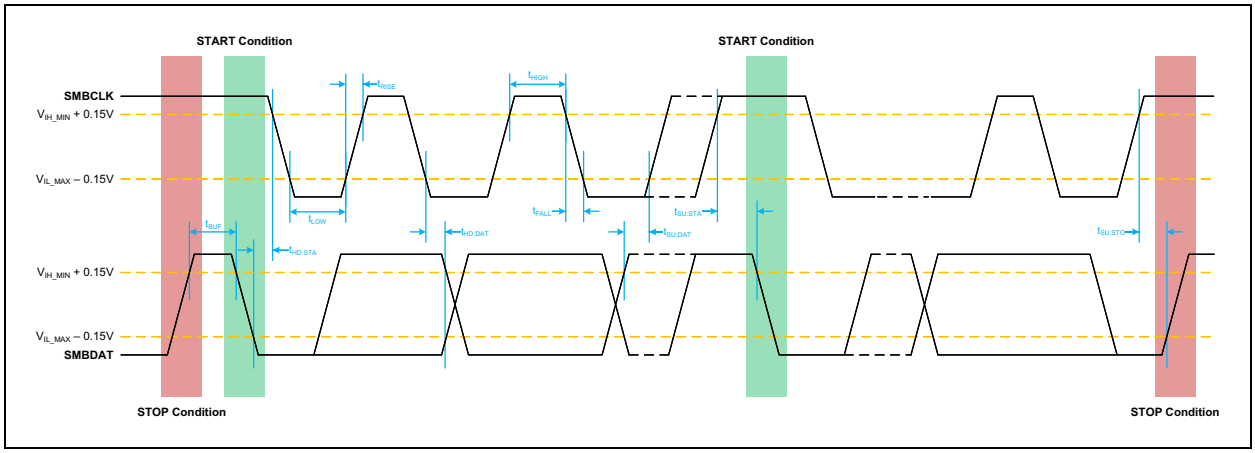


FIGURE 5-1: *SMBus Timing Diagram.*

5.1 Addressing and Control Bits

The following section describes SMBus and I²C addressing and their control bits. The address of PAC1811 is defined by the connections of pins A0 and A1 as shown in Table 5-1. The control bits follow the SMBus and I²C protocol standards.

5.1.1 SMBUS ADDRESS AND RD/WR BIT

The SMBus address byte consists of the 7-bit target address followed by a Read/Write (RD/WR) bit. If this RD/WR bit is at logic '0', the SMBus is writing data to the target device. If this RD/WR bit is at logic '1', the SMBus host is reading data from the target device.

Power-on Reset (POR) Condition:

On power-up, PAC1811 does not have any Alert, GPIO or Slow functionality.

Send an I²C command to set the address. The address is defined by the hardware connections between pins A0 and A1 (see Table 5-1) once the I²C Serial Data (SDA) and Serial Clock (SCL) completes three cycles. I²C SDA acts as START condition. The initial command can be any command that is supported by PAC1811. The device first sets its address and then executes the received commands.

Note: I_{DD} is slightly higher during this initial address selection. This is caused by an internal oscillator that is active while the address is determined.

* Multifunction pin. When pulled up to V_{DD}, pin A0 or A1 can be programmed to operate as SLOW, GPIO or ALERT pin.

Multiple PAC1811 or other devices can share the same I²C bus without any functional differences. If the host command is issued to another IC on the bus, PAC1811 still defines its address based on that command. To detect the SDA condition, the SDA hold time must be longer than the spike suppression period:

$$t_{HD:DAT} > t_{SP}$$

After the initial command, the I²C address is set and cannot be changed until the next POR event (V_{DD} or PWRDN pin) occurs. Afterwards, pins A0/A1 are either high impedance or operate as defined in Table 5-1. The default functions are defined in the CONTROL register.

TABLE 5-1: ADDRESS SELECT

A1 PIN	A0 PIN	SMBUS ADDRESS
GND	GND	1000 000b
GND	V_{DD} Pull-up(*)	1000 001b
GND	SDA	1000 010b
GND	SCL	1000 011b
V_{DD} Pull-up(*)	GND	1000 100b
V_{DD} Pull-up(*)	V_{DD} Pull-up(*)	1000 101b
V_{DD} Pull-up(*)	SDA	1000 110b
V_{DD} Pull-up(*)	SCL	1000 111b
SDA	GND	1001 000b
SDA	V_{DD} Pull-up(*)	1001 001b
SDA	SDA	1001 010b
SDA	SCL	1001 011b
SCL	GND	1001 100b
SCL	V_{DD} Pull-up(*)	1001 101b
SCL	SDA	1001 110b
SCL	SCL	1001 111b

Pins A0/A1 are set as inputs during POR, allowing signal detection to occur during the first I^2C/SMBus command. After the address is defined, pins A0/A1 enter their default state or are high impedance if the defined address disallows multifunction operation.

To avoid blocking the SMBus, the Alert functionality is disabled for addresses that do not include V_{DD} pull-up connections. The Slow function is allowed. However, it remains disabled until the function is configured and the SLOW pin is pulled high.

The following functionality can be changed when the A0/A1 pins are pulled up to V_{DD} through a resistor:

- A0 → SLOW, $\overline{\text{ALERT}}$ or GPIO
- A1 → SLOW, $\overline{\text{ALERT}}$ or GPIO

The correct programming workflow is:

1. Select the pin function
2. Configure pin settings
3. Enable the pin, if required

1. Use Case 1: A0 as SLOW Pin

POR → Set address → Set pin A0 to function as SLOW pin

Note: No setup required and no need to enable the SLOW pin as it becomes active when selecting the Slow function.

2. Use Case 2: A1 as GPIO Output Pin

POR → Set address → Set pin A1 to function as GPIO output pin

Note: No need to enable the GPIO pin as it becomes active when selecting the GPIO function.

3. Use Case 3: A0 as $\overline{\text{ALERT}}$ Pin

POR → Set address → Set pin A0 to function as $\overline{\text{ALERT}}$ pin → Set alerts to be available on the $\overline{\text{ALERT}}$ pin → Set limits → Enable $\overline{\text{ALERT}}$ pin as output

4. External Alert Connections Considerations

Do not externally connect pins A0 and A1. While this is technically feasible, considering the power-up requirements for these pins, any change in voltage during the initial address setup results in an incorrect address definition and incorrect A0/A1 functionality.

Do not enable any alerts until all PAC1811 devices that are part of the system have defined addresses.

A single address, **1000 101b** (R/W), has two alerts available. The alerts cannot be set until the I^2C address is defined after the initial I^2C command.

5.1.2 SMBUS START CONDITION

The SMBus START condition is defined as a high-to-low transition of the SMBus data line while the SMBus clock line is pulled high.

5.1.3 SMBUS STOP CONDITION

The SMBus STOP condition is defined as a low-to-high transition of the SMBus data line while the SMBus clock line is pulled high.

While in communications with the SMBus protocol, if PAC1811 detects an SMBus STOP condition, it resets its target interface and prepares to receive further data.

5.1.4 SMBUS ACK AND NACK BITS

The SMBus target acknowledges (ACK) received data bytes by holding the SMBus data line low after the 8^{th} bit of each transmitted byte.

The SMBus target negatively acknowledges (NACK) received data bytes by holding the SMBus data line high after the 8^{th} bit of each transmitted byte.

5.1.5 SMBUS DATA BYTES

All SMBus DATA bytes are sent MSB first. If a complete set of SMBus clock pulses is not sent (for example, less than 16 pulses for a 2-byte register), the data is written starting from its MSB.

5.2 SMBus Timeout

PAC1811 supports the SMBus Timeout functionality. This feature is disabled by default. To enable it, set the TIMEOUT bit in the SMBUS_SETTINGS register to **1b**.

If SMBus Timeout is enabled and the clock line is held at logic '**0**' for 25 to 35 ms ($t_{TIMEOUT}$), PAC1811 times out and resets the SMBus interface. Communication is restored with a START condition.

5.3 SMBus and I²C Compatibility

PAC1811 is compatible with the SMBus and I²C serial communication protocols:

- SMBus 3.1 1 MHz class
- I²C 1 MHz Fast-mode Plus
- I²C 3.4 MHz High-speed mode

Following are the major differences between SMBus and I²C devices. For more details, refer to the SMBus 3.1 and I²C specifications.

- If SMBus Timeout is enabled, the minimum required frequency for SMBus communications is 10 kHz. If SMBus Timeout is disabled, PAC1811 operates without following the SMBus specifications and there is no minimum frequency for communications.

> **Note 1:** By default, SMBus Timeout is disabled.
>
> **2:** To enable the SMBus Timeout feature, set the TIMEOUT bit to **1b** in the SMBUS_SETTINGS register.
>
> **3:** Disable SMBus Timeout in I²C clock stretching conditions.

- I²C does not have a timeout. This is the default condition. If SMBus Timeout is enabled, the SMBus interface resets after the clock is pulled high for $t_{TIMEOUT}$. For more details, see **Section 5.2**.
- I²C devices do not support the Alert Response Address (ARA) functionality (optional for SMBus). PAC1811 also does not support this feature. Instead, pin A0/A1 configured as $\overline{ALERT}$ pin is an open-drain output that can be monitored by the host or an embedded controller to detect alert conditions. Upon detection, the controller reads the ALERT_STATUS register, determines the alert type and then acts upon it according to its programming.
- I²C devices support Block Read and Block Write differently. The I²C protocol allows the sending of an unlimited number of bytes in either direction.For Block Read and Block Write, the SMBus protocol requires the transmission of an additional data byte indicating the number of bytes to read or write. PAC1811 supports the I²C protocol for Block Read by default (does not send byte count information). If the BYTE_COUNT bit is set to **1b** in register SMBUS_SETTINGS, PAC1811 sends the byte count as the first data byte in response to Block Read, as described by the SMBus protocol.
- SMBus uses fixed logic thresholds for logical high and logic low signals, while I²C uses levels that are proportional to V_{DD}. PAC1811 uses the SMBus method – fixed logic levels relative to the internal 1.8V (regulated) power supply according to the SMBus specifications:
  - Input High Voltage: V_{IH} = 1.35V
  - Input Low Voltage: V_{IL} = 0.8V

5.4 SMBus and I²C Standard Protocol

The following are valid PAC1811 commands:

- Read Byte
- Write Byte
- Block Read
- Block Write (I²C only)
- Send Byte
- Receive Byte

While PAC1811 responds to the I²C General Call Address (**0000 000b**), it does not respond to the SMBus Alert Response Address (**0001 100b**).

All protocol packets present throughout this document, use the convention in Table 5-2.

TABLE 5-2: PROTOCOL PACKET

DATA SENT TO DEVICE	DATA SENT TO THE HOST
Number of bits sent	Number of bits sent

5.5 Auto-incrementing Pointer

PAC1811 has an auto-incrementing address pointer. The pointer has two loops for auto-incrementing: a READ loop and a WRITE loop.

While the READ loop includes all of the data and configuration registers, the WRITE loop includes only the configuration registers.

> **Note:** READ and WRITE loops do not include Refresh (any) commands.

Figure 5-2 shows how the auto-incrementing READ loop works for reading. It also shows how the WRITE loop functions with any refresh command.

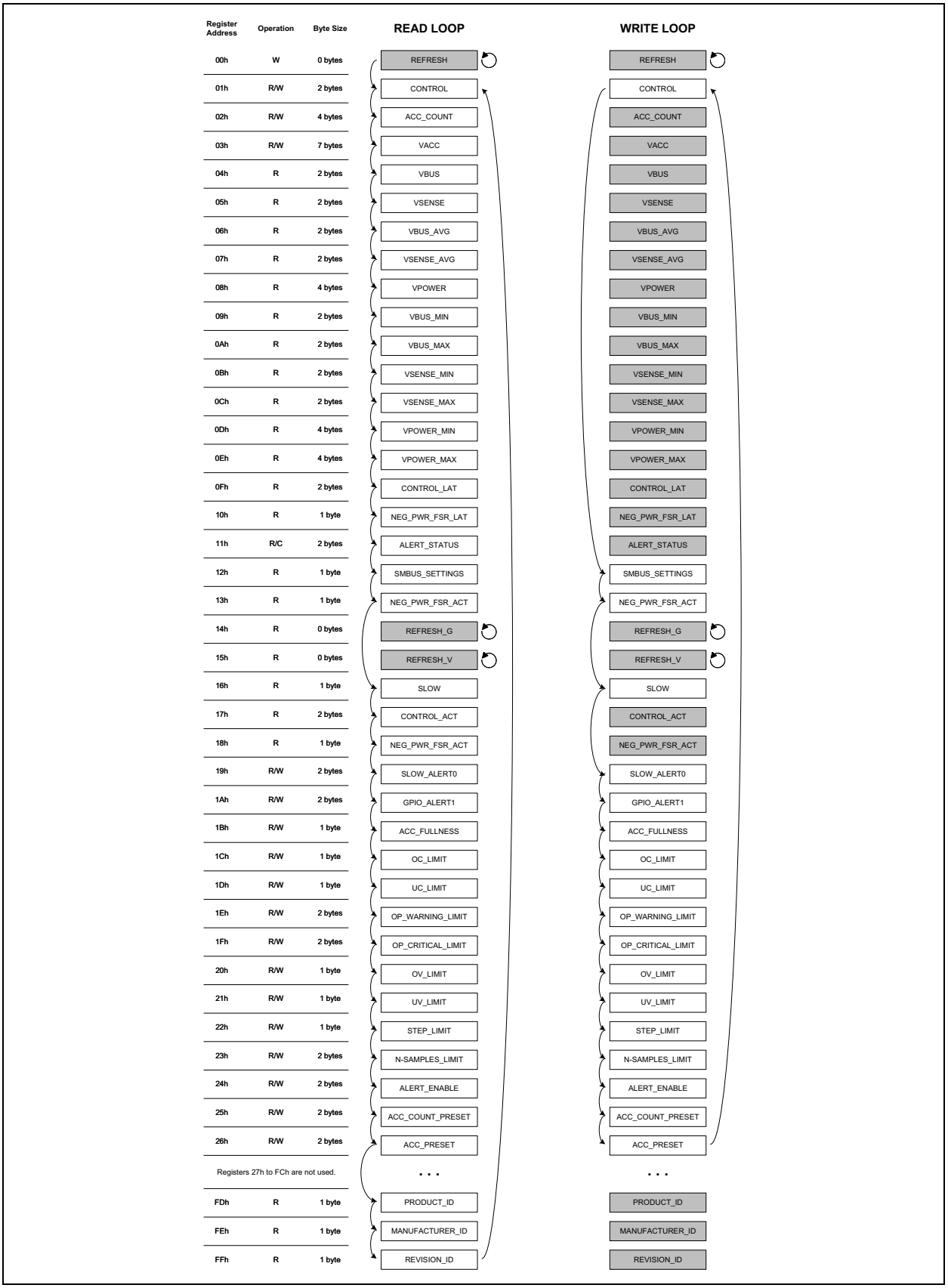


FIGURE 5-2: *READ and WRITE Auto-Incrementing Loops.*

5.6 SMBus/I²C Commands

The following section describes the commands sent to PAC1811 using the SMBus or I²C protocols.

5.6.1 REFRESH AND REFRESH_V

Issue Refresh and Refresh_V commands using the Send Byte. Specify the target address and the selected command data (**00h** for REFRESH or **15h** for REFRESH_V) as shown in Table 5-3.

TABLE 5-3: REFRESH AND REFRESH_V COMMANDS

START Condition	Target Address	WR	ACK	REFRESH or REFRESH_V Register Address	ACK	STOP Condition
1 → 0	**YYYY_YYY**	0	0	**00h or 15h**	0	0 → 1

5.6.2 GENERAL CALL RESPONSE

When the host sends the General Call Address, PAC1811 is able to execute a Refresh_G command. For more details, see **Section 4.2.3**.

Issue the Refresh_G command using the Send Byte. Specify the target address, the General Call Address (**0000 000b**) and the REFRESH_G command register address (**14h**).

Table 5-4 shows the PAC1811 General Call Response to a Refresh_G command.

TABLE 5-4: GENERAL CALL RESPONSE

START Condition	General Call Address	WR	ACK	REFRESH_G Register Address	ACK	STOP Condition
1 → 0	**0000_000**	0	0	**14h**	0	0 → 1

5.6.3 WRITE BYTE

Use the Write Byte to write one byte of data to the specified register address, as shown in Table 5-5.

TABLE 5-5: WRITE BYTE

START Condition	Target Address	WR	ACK	Register Address	ACK	Register Data	ACK	STOP Condition
1 → 0	**YYYY_YYY**	0	0	**XXh**	0	**XXh**	0	0 → 1

5.6.4 READ BYTE

Use the Read Byte to read one byte of data from the specified register address, as shown in Table 5-6.

If an invalid register address is specified, the target ACKs its address, but NACKs the register address.

The host NACKs the data received from the target by holding the SMBus data line high after the 8th data bit is sent.

TABLE 5-6: READ BYTE

START Condition	Target Address	WR	ACK	Register Address	ACK	START Condition
1 → 0	YYYY_YYY	0	0	XXh	0	1 → 0

Target Address	RD	ACK	Register Data	NACK	STOP Condition
YYYY_YYY	1	0	XXh	1	0 → 1

5.6.5 SEND BYTE

Use the Send Byte to set the internal register pointer to the correct address location. No data is transferred during the Send Byte, as shown in Table 5-7.

TABLE 5-7: SEND BYTE

START Condition	Target Address	WR	ACK	Register Address	ACK	STOP Condition
1 → 0	YYYY_YYY	0	0	XXh	0	0 →1

5.6.6 RECEIVE BYTE

Use the Receive Byte to read data from a register when the internal register pointer is known to be at the correct address location. For example, when the address is set via the Send Byte. This is shown in Table 5-8.

Note: If the BYTE_COUNT bit is set to 1b in the SMBUS_SETTINGS register, PAC1811 reports the byte count. This does not comply with SMBus specifications.

After receiving the register data, if an ACK is received, the internal register pointer automatically increments. If instead a NACK is received, then the internal address pointer remains at the same position.

To continue clocking and reading the next register, the host sends an ACK after the register data, instead of sending a NACK followed by a STOP condition.

TABLE 5-8: RECEIVE BYTE

START Condition	Target Address	RD	ACK	Register Data	NACK	STOP Condition
1 → 0	YYYY_YYY	1	0	XXh	1	0 → 1

5.6.7 BLOCK WRITE – I²C VERSION

Use Block Write to write multiple data bytes to a single register that has more than one byte of data or to a group of contiguous registers, as shown in Table 5-9.

If an invalid register address is specified, the target ACKs its address, but NACKs the register address.

The host NACKs the data received from the target by holding the SMBus data line high after the 8th data bit is sent.

TABLE 5-9: BLOCK WRITE – I²C VERSION

START Condition	Target Address	WR	ACK	Register Address	ACK	Register Data	ACK
1 → 0	YYYY_YYY	0	0	XXh	0	XXh	0

Register Data	ACK	Register Data	ACK	Register Data	ACK	STOP Condition
XXh	0	XXh	0	XXh	0	0 → 1

5.6.8 BLOCK WRITE – SMBUS VERSION

PAC1811 does not support the SMBus Block Write functionality. Use the I²C Block Write implementation.

5.6.9 BLOCK READ – I²C VERSION

Use Block Read to read multiple data bytes from a register that has more than one byte of data or from a group of contiguous registers, as shown in Table 5-10.

If an invalid register address is specified, the target ACKs its address, but NACKs the register address.

The host NACKs the data received from the target by holding the SMBus data line high after the 8th data bit is sent.

TABLE 5-10: BLOCK READ – I²C VERSION

START Condition	Target Address	WR	ACK	Register Address	ACK	START	Target Address	RD	ACK	Register Data
1 → 0	YYYY_YYY	0	0	XXh	0	1 → 0	YYYY_YYY	1	0	XXh

ACK	Register Data	ACK	Register Data	ACK	Register Data	ACK	Register Data	NACK	STOP Condition
0	XXh	0	XXh	0	XXh	0	XXh	1	0 → 1

5.6.10 BLOCK READ – SMBUS VERSION

If the BYTE_COUNT bit in the SMBUS_SETTINGS register is set to **1b**, Block Read results in PAC1811 sending the byte count before register data. This means that, during a transaction, the byte count is included each time a new register is read. This is shown in Table 5-11.

TABLE 5-11: BLOCK READ – SMBUS VERSION (MUST SET BYTE COUNT BIT)

START Condition	Target Address	WR	ACK	Register Address	ACK	START Condition	Target Address	RD	ACK
1 → 0	**YYYY_YYY**	0	0	**XXh**	0	1 → 0	**YYYY_YYY**	1	0

Byte Count	ACK	Register Data	ACK	Byte Count	Register Data	ACK	Byte Count	Register Data	NACK	STOP Condition
XXh = N	0	**XXh**	0	**XXh** = N	**XXh**	0	**XXh** = N	**XXh**	1	0 → 1

6.0 REGISTER DESCRIPTION

Table 6-1 presents the PAC1811 registers arranged in hexadecimal order based on their register address.

TABLE 6-1: PAC1811 REGISTERS

Register Name and Address	Description	Type	Bytes	POR Value
REFRESH (Address 00h)	Send Byte for Refresh command	SEND	0	00h
CONTROL (Address 01h)	Configure sample rate, pins A0/A1 and more	R/W	2	2520h
ACC_COUNT (Address 02h)	Accumulator count	R	4	000000h
VACC (Address 03h)	Accumulator	R	7	00000000000000h
VBUS (Address 04h)	V_{BUS} measurement	Block Read	2	0000h
VSENSE (Address 05h)	V_{SENSE} measurement	Block Read	2	0000h
VBUS_AVG (Address 06h)	Rolling average of most recent V_{BUS} measurements	Block Read	2	0000h
VSENSE_AVG (Address 07h)	Rolling average of most recent V_{SENSE} measurements	Block Read	2	0000h
VPOWER (Address 08h)	V_{POWER} calculation: $V_{SENSE} \times V_{BUS}$	Block Read	4	00000000h
VBUS_MIN (Address 09h)	Minimum value measured on V_{BUS}	Block Read	2	0000h
VBUS_MAX (Address 0Ah)	Maximum value measured on V_{BUS}	Block Read	2	0000h
VSENSE_MIN (Address 0Bh)	Minimum value measured on V_{SENSE}	Block Read	2	0000h
VSENSE_MAX (Address 0Ch)	Maximum value measured on V_{SENSE}	Block Read	2	0000h
VPOWER_MIN (Address 0Dh)	Minimum calculated value for V_{POWER}	Block Read	4	00000000h
VPOWER_MAX (Address 0Eh)	Maximum calculated value for V_{POWER}	Block Read	4	00000000h
CONTROL_LAT (Address 0Fh)	Latched active settings for CONTROL register	R	2	2520h
NEG_PWR_FSR_LAT (Address 10h)	Latched active settings for NEG_PWR_FSR register	R	1	00h
ALERT_STATUS (Address 11h)	Read to determine the cause that triggered an alert	RC	2	0000h
SMBUS_SETTINGS (Address 12h)	Activate SMBus functionality, I/O data for R/$\overline{W}$ on I/O pins	R/W	1	10h
NEG_PWR_FSR (Address 13h)	Configuration control for bipolar current and voltage	R/W	1	00h
REFRESH_G (Address 14h)	Refresh response to General Call Address command	SEND	0	00h
REFRESH_V (Address 15h)	Refreshes $V_{BUS\ and}$ V_{SENSE} data only, no accumulator or accumulator count reset	SEND	0	00h
SLOW (Address 16h)	Status and control for SLOW pin functions	R/W	1	00h
CONTROL_ACT (Address 17h)	Currently active settings for CONTROL register	R	2	2520h

Note 1: Unimplemented/reserved bits in registers can be read and written, but they do not impact any internal functionality.

2: If the data written to a register is less than the full register size, the data is written to the register's MSBs.

TABLE 6-1: PAC1811 REGISTERS (CONTINUED)

Register Name and Address	Description	Type	Bytes	POR Value
NEG_PWR_FSR_ACT (Address 18h)	Currently active settings for NEG_PWR_FSR register	R	1	00h
SLOW_ALERT0 (Address 19h)	Assign specific alerts to A0	R/W	2	0000h
GPIO_ALERT1 (Address 1Ah)	Assign specific alerts to A1	R/W	2	0000h
ACC_FULL_LIMIT (Address 1BH)	Set Accumulator and Accumulator Count Fullness limits	R/W	1	01h
OC_LIMIT (Address 1CH)	Set overcurrent limit	R/W	1	00h
UC_LIMIT (Address 1DH)	Set undercurrent limit	R/W	1	00h
OP_WARNING_LIMIT (Address 1EH)	Set overpower warning limit	R/W	2	0000h
OP_CRITICAL_LIMIT (Address 1FH)	Set overpower critical limit	R/W	2	0000h
OV_LIMIT (Address 20H)	Set overvoltage limit	R/W	1	00h
UV_LIMIT (Address 21H)	Set undervoltage limit	R/W	1	00h
STEP_LIMIT (Address 22H)	Set step limit	R/W	1	00h
N-SAMPLES_LIMIT (Address 23h)	Set number of consecutive samples over set threshold to trigger an alert	R/W	2	00h
ALERT_ENABLE (Address 24h)	Enables alerts	R/W	2	0000h
ACC_COUNT_PRESET (Address 25h)	Accumulator Count Preset	R/W	2	0000h
VACC_PRESET (Address 26h)	Accumulator Preset	R/W	2	0000h
. . .				
Registers 27h to FCh are not used, Note 1				
. . .				
PRODUCT_ID (Address FDh)	Stores the Product ID	R	1	84h
MANUFACTURER_ID (Address FEh)	Stores the Manufacturer ID	R	1	54h
REVISION_ID (Address FFh)	Stores the Revision Number	R	1	04h

Note 1: Unimplemented/reserved bits in registers can be read and written, but they do not impact any internal functionality.

2: If the data written to a register is less than the full register size, the data is written to the register's MSBs.

6.1 Reading Data Bytes

Data represented by the data registers becomes readable 1 µs after a conversion cycle completes and a Refresh (any) command is issued.

When new data is written to a configuration register and the host reads it back, the new data is read back even if no Refresh (any) command was issued to trigger the new data to take effect.

Check the following registers to ensure that the active and latched configurations are known:

- CONTROL_ACT
- NEG_PWR_FSR_ACT
- CONTROL_LAT
- NEG_PWR_FSR_LAT

6.2 Register Categories

The PAC1811 registers can be categorized as follows:

- Data Registers:
  - ACC_COUNT
  - VACC
  - VBUS
  - VSENSE
  - VBUS_AVG
  - VSENSE_AVG
  - VPOWER
  - VBUS_MIN
  - VBUS_MAX
  - VSENSE_MIN
  - VSENSE_MAX
  - VPOWER_MIN
  - VPOWER_MAX
- Configuration Registers:
  - CONTROL
  - NEG_PWR_FSR
  - SLOW
  - SLOW_ALERT0
  - GPIO_ALERT1
  - ACC_FULL_LIMIT
  - ALERT_ENABLE
  - ACC_COUNT_PRESET
  - VACC_PRESET

6.3 Detailed Register Information

REGISTER 6-1: REFRESH (ADDRESS 00H)

SEND	SEND	SEND	SEND	SEND	SEND	SEND	SEND
No data in this command, Send Byte only							
bit 7							bit 0

Legend:			
R = Read bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	X = Bit is unknown

bit 7:0 **SEND**[7:0]: This command is a Send Byte and does not contain any data.
When PAC1811 receives the command, it executes a Refresh. The accumulator results, accumulator count, V_{BUS} and V_{SENSE} measurements update and the accumulators reset.
When a Refresh command is issued, data registers become readable after the current conversion cycle completes. The conversion period varies depending on the selected sample rate. Set the ALERT_CC bit in the ALERT_ENABLE register if the fastest timing is required.
The host can read the accumulator results, accumulator count, V_{BUS} and V_{SENSE} data any time before the next Refresh command is issued (see Figure 6-1).
Update the accumulator results, accumulator count, V_{BUS} and V_{SENSE} data without resetting the accumulators using a Refresh_V command. See Section 4.2.2, Refresh Command.

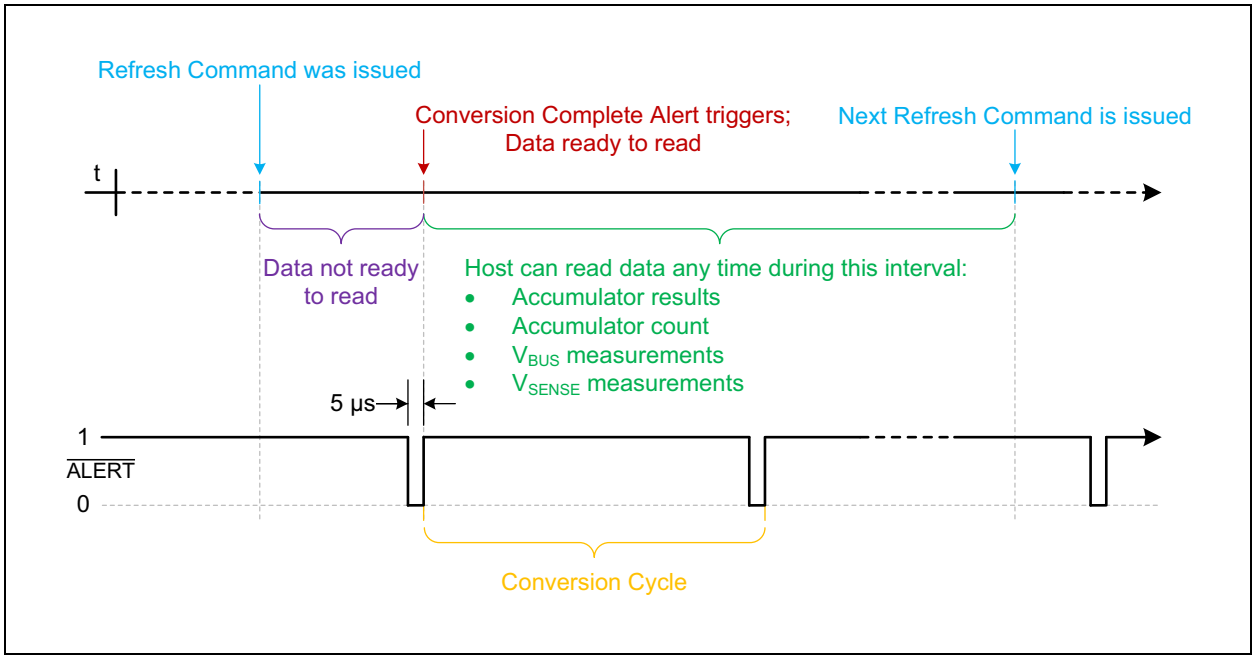


FIGURE 6-1: *Host Read Period After a Refresh Command.*

REGISTER 6-2: CONTROL (ADDRESS 01H)

R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1
SAMPLE_MODE[3:0]				GPIO_ALERT1[1:0]		SLOW_ALERT0[1:0]	
bit 15							bit 8

R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
AVERAGE[2:0]			AA	ACC_CONFIG[1:0]		AUTO_REFRESH [1:0]	
bit 7							bit 0

Legend:			
R = Read bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	X = Bit is unknown

bit 15:12 **SAMPLE_MODE**[3:0]: Selects one of the sample modes listed below. These modes are exclusive – only one mode can be set at any given time.
One of the sample rate options is Sleep state for when no sampling occurs.
When switching sample modes during a conversion cycle, the ADC continues the current sample mode until the conversion completes and then switches to the new sample mode. Registers CONTROL and CONTROL_ACT update.
Switching from a Continuous sample mode to a Single-shot mode triggers an extra conversion cycle.
When using a GPIO Triggered sample mode, first configure the desired pin (A0 or A1) as an input by setting the SLOW_ALERT0[1:0] or GPIO_ALERT1[1:0] bits to **01b**.

0000b = 8,192 sps (see **Section 4.8.1**)
0001b = 4,096 sps
0010b = 1,024 sps (default)
0011b = 256 sps
0100b = 64 sps
0101b = 8 sps (Slow mode) (see **Section 4.2.8**)
0110b = Single-shot mode (see **Section 4.9.1**)
0111b = Single-shot Average mode
1000b = Single-shot Awake mode
1001b = Single-shot Awake Average mode
1010b = V_{BUS} Only at 16,384 sps (see **Section 4.2.9**)
1011b = V_{SENSE} Only at 16,384 sps (see **Section 4.2.9**)
1100b = GPIO (A0) Triggered Single-shot Awake mode, Edge (see **Section 4.9.1.4**)
1101b = GPIO (A1) Triggered Single-shot Awake mode, Edge (see **Section 4.9.1.4**)
1110b = Sleep state (see **Section 4.2.6**)
1111b = Sleep state (see **Section 4.2.6**)

bit 11:10 **GPIO_ALERT1**[1:0]: Selects the signals for the A1 pin, GPIO/$\overline{\text{ALERT}}$ function.
If pin A1 is configured as GPIO pin, the R/W data for the pin is stored in register SMBUS_SETTINGS.
While the A1 pin is multifunction, Microchip recommends using A1 as GPIO/$\overline{\text{ALERT}}$ pin.

00b = $\overline{\text{ALERT}}$. Functions as $\overline{\text{ALERT1}}$ pin.
01b = GPIO digital input. Read data from register SMBUS_SETTINGS as input to this pin. (default)
10b = GPIO digital output. Write data from this pin as output to register SMBUS_SETTINGS.
11b = SLOW. Functions as SLOW pin. Pulling the pin high overrides the programmed sample rate and results in a sample rate of 8 sps (Slow mode). Configuring the pin as SLOW pin takes priority over other settings, including GPIO Triggered mode.

bit 9:8 **SLOW_ALERT0**[1:0]: Selects the signals for the A0 pin, SLOW/$\overline{\text{ALERT}}$ function.
If pin A0 is configured as GPIO pin, the R/W data for the pin is stored in register SMBUS_SETTINGS.
While the A0 pin is multifunction, Microchip recommends using A0 as SLOW/$\overline{\text{ALERT}}$ pin.

00b = $\overline{\text{ALERT}}$. Functions as $\overline{\text{ALERT0}}$ pin.
01b = GPIO digital input. Read data from register SMBUS_SETTINGS as input to this pin. (default)
10b = GPIO digital output. Write data from this pin as output to register SMBUS_SETTINGS.
11b = SLOW. Functions as SLOW pin. Pulling the pin high overrides the programmed sample rate and results in a sampling rate of 8 sps (Slow mode). Configuring the pin as SLOW pin takes priority over other settings, including GPIO Triggered mode.

bit 7:5 **AVERAGE**[2:0]: Selects how many samples are included in rolling average.

000b = 4
001b = 8 (default)
010b = 16
011b = 32
100b = Reserved. Do not select this option.
101b = 64
110b = Reserved. Do not select this option.
111b = 128

bit 4 **AA**: Configures Adaptive Accumulation, which emulates a sample mode of 8,192 sps for all samples rates when using the Slow function. The Adaptive Accumulation function works in conjunction with the SAMPLE_MODE[3:0] bits.
For more details, see **Section 4.8.1** and **Section 4.8.2**.

0b = Disables adaptive accumulation. The results in the accumulation register do not change when the SLOW pin is pulled high (default).
1b = Enables adaptive accumulation. The results in the accumulation register change when the SLOW pin is pulled high to match results obtained at 8,192 sps.

bit 3:2 **ACC_CONFIG**[1:0]: Configures accumulator to sum V_{POWER} calculations or V_{SENSE} or V_{BUS} samples.

00b = Accumulator sums V_{POWER} calculations (default)
01b = Accumulator sums V_{SENSE} measurements
10b = Accumulator sums V_{BUS} measurements
11b = Reserved. Do not select this option.

bit 1:0 **AUTO_REFRESH**[1:0]: Configures Auto-refresh. A Refresh (any) command occurs after a conversion cycle completes. In Single-shot Average sample mode, a Refresh (any) command occurs only after the configured number of samples are averaged (8 samples by default). This is controlled by the AVERAGE[2:0] bits in this register.
While Auto-refresh is enabled, manual Refresh (any) commands are ignored. Disabling the feature allows PAC1811 to execute manual Refresh (any) commands.
When Auto-refresh is enabled, functional changes are not applied. Before modifying register values, ensure Auto-refresh is disabled. Auto-refresh can be re-enabled afterwards.

00b = Disables Auto-refresh. Requires manual Refresh (any) commands (default).
01b = Enables Auto-refresh. Resets accumulator and accumulator count.
PAC1811 executes a Limited Refresh to move V_{BUS}, V_{SENSE}, V_{POWER}, accumulator data and accumulator count to the I^2C domain.
10b = Enables Auto-refresh. Does not reset accumulator and accumulator count.
PAC1811 executes a Limited Refresh_V to move V_{BUS}, V_{SENSE}, V_{POWER}, accumulator data and accumulator count to the I^2C domain.
11b = Reserved. Do not select this option.

REGISTER 6-3: ACC_COUNT (ADDRESS 02H)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
ACC_COUNT[31:24]							
bit 31							bit 24

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
ACC_COUNT[23:16]							
bit 23							bit 16

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
ACC_COUNT[15:8]							
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
ACC_COUNT[7:0]							
bit 7							bit0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	X = Bit is unknown

bit 31:0 **ACC_COUNT**[31:0]: Accumulator Count. This register stores the number of accumulated (summed) V_{POWER} calculations (default), V_{BUS} measurements or V_{SENSE} measurements in the VACC register. A Refresh command resets the register, while a Refresh_V command does not.

REGISTER 6-4: VACC (ADDRESS 03H)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VACC[55:48]							
bit 55							bit 48

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VACC[47:40]							
bit 47							bit 40

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VACC[39:32]							
bit 39							bit 32

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VACC[31:24]							
bit 31							bit 24

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VACC[23:16]							
bit 23							bit 16

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VACC[15:8]							
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VACC[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	X = Bit is unknown

bit 55:0 **VACC**[55:0]: The Accumulator (VACC) stores, by default, the accumulated sum of V_{POWER} calculations. It can accumulate V_{BUS} or V_{SENSE} measurements if the ACC_CONFIG[1:0] bits in the CONTROL register are set to **01b** for V_{BUS} or **10b** for V_{SENSE}.
The stored values are 56-bit unsigned numbers, unless either V_{BUS} or V_{SENSE} is configured to have a Bipolar range. In that case, the values are stored using 55 bits and one sign bit (2's complement).
A Refresh command resets the register, while a Refresh_V does not.
When changing the type of results (V_{BUS}, V_{SENSE} or V_{POWER}) accumulated in the VACC register using a Refresh_V command, already accumulated results are not reset. This results in the VACC register containing both new and old values. Send a Refresh command to completely reset the register.
This register uses 16 bits to store V_{BUS} and V_{SENSE} results and 32 bits for V_{POWER} calculations.

Note 1: Power is always calculated using signed numbers for V_{BUS} and V_{SENSE}. However, if both V_{BUS} and V_{SENSE} are measured using the default unipolar mode, power is reported as an unsigned number. This can cause very small discrepancies between a manual comparison of $V_{BUS} \times V_{SENSE}$ and the results that PAC1811 calculates and accumulates for V_{POWER}. PAC1811 performs calculations using more bits than the reported results for V_{BUS} and V_{SENSE}. Thus, in some cases, values stored in the VPOWER and VACC registers are more accurate than calculations using the values stored in the VBUS and VSENSE registers.

2: This register accumulates both positive and negative values even in Unipolar mode. Thus, if negative or near zero currents are measured, send a Refresh command to ensure the correct accumulated values are stored.

REGISTER 6-5: VBUS (ADDRESS 04H)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VBUS[15:8]							
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VBUS[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	X = Bit is unknown

bit 15:0 **VBUS**[15:0]: This register stores the most recent V_{BUS} measurement (sample) as a digitized value. This value is a 16-bit unsigned number, unless V_{BUS} is configured to have a bipolar range. In that case, the value is stored using 15 bits and one sign bit (2's complement).
Refresh or Refresh_V commands do not reset this register.

REGISTER 6-6: VSENSE (ADDRESS 05H)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VSENSE[15:8]							
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VSENSE[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	X = Bit is unknown

bit 15:0 **VSENSE**[15:0]: This register stores the most recent V_{SENSE} measurement (sample) as a digitized value. This value is a 16-bit unsigned number, unless V_{SENSE} is configured to have a bipolar range. In that case, the value is stored using 15 bits and one sign bit (2's complement).
Refresh or Refresh_V commands do not reset this register.

REGISTER 6-7: VBUS_AVG (ADDRESS 06H)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VBUS_AVG[15:8]							
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VBUS_AVG[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	X = Bit is unknown

bit 15:0 **VBUS_AVG**[15:0]: This register contains the rolling average of V_{BUS} measurements (samples).
The rolling average is a 16-bit unsigned number, unless V_{BUS} is configured to have a bipolar range. In that case, the rolling average is stored using 15 bits and one sign bit (2's complement).
Refresh or Refresh_V commands do not reset this register.
When reading register VBUS_AVG, PAC1811 NACKs the register Read command until the internal buffer is full (valid average value).

Note: During a Bulk Read action, PAC1811 does not NACK the incorrect value.

REGISTER 6-8: VSENSE_AVG (ADDRESS 07H)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VSENSE_AVG[15:8]							
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VSENSE_AVG[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	X = Bit is unknown

bit 15:0 **VSENSE_AVG**[15:0]: This register contains the rolling average of V_{SENSE} measurements (samples).
The rolling average is a 16-bit unsigned number, unless V_{SENSE} is configured to have a bipolar range. In that case, the rolling average is stored using 15 bits and one sign bit (2's complement).
Refresh or Refresh_V commands do not reset this register.
When reading register VSENSE_AVG, PAC1811 NACKs the register Read command until the internal buffer is full (valid average value).

Note: During a Bulk Read action, PAC1811 does not NACK the incorrect value.

REGISTER 6-9: VPOWER (ADDRESS 08H)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VPOWER[31:24]							
bit 31							bit 24

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VPOWER[23:16]							
bit 23							bit 16

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VPOWER[15:8]							
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VPOWER[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	X = Bit is unknown

bit 31:0 **VPOWER**[31:0]: This register contains the result of a $V_{BUS} \times V_{SENSE}$ calculation. This result represents proportional power.
The result is a 32-bit unsigned number, unless either V_{BUS} or V_{SENSE} is set to have a bipolar range. In that case, the result is stored using 31 bits and one sign bit (2's complement). This result is then summed in the accumulator (register VACC).
Refresh or Refresh_V commands do not reset the register.

Note: Power is always calculated using signed numbers for V_{BUS} and V_{SENSE}. However, if both V_{BUS} and V_{SENSE} are measured using the default unipolar mode, power is reported as an unsigned number. This can cause very small discrepancies between a manual comparison of $V_{BUS} \times V_{SENSE}$ and the results that PAC1811 calculates and accumulates for V_{POWER}. PAC1811 performs calculations using more bits than the reported results for V_{BUS} and V_{SENSE}. Thus, in some cases, values stored in the VPOWER and VACC registers are more accurate than calculations using the values stored in the VBUS and VSENSE registers.

REGISTER 6-10: VBUS_MIN (ADDRESS 09H)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VBUS_MIN[15:8]							
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VBUS_MIN[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	X = Bit is unknown

bit 15:0 **VBUS_MIN**[15:0]: This register contains the minimum value measured for V_{BUS}.
The value is a 16-bit unsigned number, unless V_{BUS} is configured to have a bipolar range. In that case, the value is stored using 15 bits and one sign bit (2's complement).
The value is determined by a single data conversion and is independent of averaging or N-Samples limits.
A Refresh command resets the register, while a Refresh_V command does not.

REGISTER 6-11: VBUS_MAX (ADDRESS 0AH)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VBUS_MAX[15:8]							
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VBUS_MAX[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	X = Bit is unknown

bit 15:0 **VBUS_MAX**[15:0]: This register contains the maximum value measured for V_{BUS}.
The value is a 16-bit unsigned number, unless V_{BUS} is configured to have a bipolar range. In that case, the value is stored using 15 bits and one sign bit (2's complement).
The value is determined by a single data conversion and is independent of averaging or N-Samples limits.
A Refresh command resets the register, while a Refresh_V command does not.

REGISTER 6-12: VSENSE_MIN (ADDRESS 0BH)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VSENSE_MIN[15:8]							
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VSENSE_MIN[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	X = Bit is unknown

bit 15:0 **VSENSE_MIN**[15:0]: This register contains the minimum value measured for V_{SENSE}.
The value is a 16-bit unsigned number, unless V_{SENSE} is configured to have a bipolar range. In that case, the value is stored using 15 bits and one sign bit (2's complement).
The value is determined by a single data conversion and is independent of averaging or N-Samples limits.
A Refresh command resets the register, while a Refresh_V command does not.

REGISTER 6-13: VSENSE_MAX (ADDRESS 0CH)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VSENSE_MAX[15:8]							
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VSENSE_MAX[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	X = Bit is unknown

bit 15:0 **VSENSE_MAX**[15:0]: This register contains the maximum value measured for V_{SENSE}.
The value is a 16-bit unsigned number, unless V_{SENSE} is configured to have a bipolar range. In that case, the value is stored using 15 bits and one sign bit (2's complement).
The value is determined by a single data conversion and is independent of averaging or N-Samples limits.
A Refresh command resets the register, while a Refresh_V command does not.

REGISTER 6-14: VPOWER_MIN (ADDRESS 0DH)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VPOWER_MIN[31:24]							
bit 31							bit 24

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VPOWER_MIN[23:16]							
bit 23							bit 16

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VPOWER_MIN[15:8]							
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VPOWER_MIN[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	X = Bit is unknown

bit 31:0 **VPOWER_MIN**[31:0]: This register contains the minimum calculated V_{POWER} value (V_{BUS} × V_{SENSE}). The value is a 32-bit unsigned number, unless either V_{BUS} or V_{SENSE} are configured to have a bipolar range. In that case, the value is stored using 31 bits and one sign bit (2's complement).
The value is determined by a single data conversion and is independent of averaging or N-Samples limits.
A Refresh command resets the register, while a Refresh_V command does not.

Note: Power is always calculated using signed numbers for V_{BUS} and V_{SENSE}. However, if both V_{BUS} and V_{SENSE} are measured using the default unipolar mode, power is reported as an unsigned number. This can cause very small discrepancies between a manual comparison of V_{BUS} × V_{SENSE} and the results that PAC1811 calculates and accumulates for V_{POWER}. PAC1811 performs calculations using more bits than the reported results for V_{BUS} and V_{SENSE}. Thus, in some cases, values stored in the VPOWER and VACC registers are more accurate than calculations using the values stored in the VBUS and VSENSE registers.

REGISTER 6-15: VPOWER_MAX (ADDRESS 0EH)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VPOWER_MAX[31:24]							
bit 31							bit 24

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VPOWER_MAX[23:16]							
bit 23							bit 16

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VPOWER_MAX[15:8]							
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VPOWER_MAX[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	X = Bit is unknown

bit 31:0 **VPOWER_MAX**[31:0]: This register contains the maximum calculated V_{POWER} value ($V_{BUS} \times V_{SENSE}$). The value is a 32-bit unsigned number, unless either V_{BUS} or V_{SENSE} are configured to have a bipolar range. In that case, the value is stored using 31 bits and one sign bit (2's complement).
The value is determined by a single data conversion and is independent of averaging or N-Samples limits.
A Refresh command resets the register, while a Refresh_V command does not.

Note: Power is always calculated using signed numbers for V_{BUS} and V_{SENSE}. However, if both V_{BUS} and V_{SENSE} are measured using the default unipolar mode, power is reported as an unsigned number. This can cause very small discrepancies between a manual comparison of $V_{BUS} \times V_{SENSE}$ and the results that PAC1811 calculates and accumulates for V_{POWER}. PAC1811 performs calculations using more bits than the reported results for V_{BUS} and V_{SENSE}. Thus, in some cases, values stored in the VPOWER and VACC registers are more accurate than calculations using the values stored in the VBUS and VSENSE registers.

REGISTER 6-16: CONTROL_LAT (ADDRESS 0FH)

R-0	R-0	R-1	R-0	R-0	R-1	R-0	R-1
SAMPLE_MODE[3:0]				GPIO_ALERT1[1:0]		SLOW_ALERT0[1:0]	
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
AVERAGE[2:0]			AA	ACC_CONFIG[1:0]		AUTO_REFRESH[1:0]	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	X = Bit is unknown

This register contains a copy of register CONTROL.The bits in this register reflect the settings that were active before the most recent Refresh (any) command.
The values in the CONTROL register can be programmed, but not yet activated by a Refresh (any) command, while the values in the CONTROL_ACT register are the currently active settings.
The CONTROL_LAT register allows the host to determine the settings that were active prior to the most recent Refresh (any) command and therefore, the settings correspond to the dataset stored in the readable registers.
This register is valid when the results registers are valid, 125 µs after a Refresh (any) command.

bit 15:12 **SAMPLE_MODE**[3:0]: Selects one of the sample modes listed below. These modes are exclusive – only one mode can be set at any given time.
One of the sample rate options is Sleep state for when no sampling occurs.
When switching sample modes during a conversion cycle, the ADC continues the current sample mode until the conversion completes and then switches to the new sample mode. Registers CONTROL and CONTROL_ACT update.
Switching from a Continuous sample mode to a Single-shot mode triggers an extra conversion cycle.
When using a GPIO Triggered sample mode, first configure the desired pin (A0 or A1) as an input by setting the SLOW_ALERT0[1:0] or GPIO_ALERT1[1:0] bits to **01b**.

0000b = 8,192 sps (see **Section 4.8.1**)
0001b = 4,096 sps
0010b = 1,024 sps (default)
0011b = 256 sps
0100b = 64 sps
0101b = 8 sps (Slow mode) (see **Section 4.2.8**)
0110b = Single-shot mode (see **Section 4.9.1**)
0111b = Single-shot Average mode
1000b = Single-shot Awake mode
1001b = Single-shot Awake Average mode
1010b = V_{BUS} Only at 16,384 sps (see **Section 4.2.9**)
1011b = V_{SENSE} Only at 16,384 sps (see **Section 4.2.9**)
1100b = GPIO (A0) Triggered Single-shot Awake mode, Edge (see **Section 4.9.1.4**)
1101b = GPIO (A1) Triggered Single-shot Awake mode, Edge (see **Section 4.9.1.4**)
1110b = Sleep state (see **Section 4.2.6**)
1111b = Sleep state (see **Section 4.2.6**)

bit 11:10 **GPIO_ALERT1**[1:0]: Selects the signals for the A1 pin, GPIO/$\overline{\text{ALERT}}$ function.
If pin A1 is configured as GPIO pin, the R/W data for the pin is stored in register SMBUS_SETTINGS.
While the A1 pin is multifunction, Microchip recommends using A1 as GPIO/$\overline{\text{ALERT}}$ pin.

00b = $\overline{\text{ALERT}}$. Functions as $\overline{\text{ALERT1}}$ pin.
01b = GPIO digital input. Read data from register SMBUS_SETTINGS as input to this pin. (default)
10b = GPIO digital output. Write data from this pin as output to register SMBUS_SETTINGS.
11b = SLOW. Functions as SLOW pin. Pulling the pin high overrides the programmed sample rate and results in a sample rate of 8 sps (Slow mode). Configuring the pin as SLOW pin takes priority over other settings, including GPIO Triggered mode.

bit 9:8 **SLOW_ALERT0**[1:0]: Selects the signals for the A0 pin, SLOW/$\overline{\text{ALERT}}$ function.
If pin A0 is configured as GPIO pin, the R/W data for the pin is stored in register SMBUS_SETTINGS.
While the A0 pin is multifunction, Microchip recommends using A0 as SLOW/$\overline{\text{ALERT}}$ pin.

00b = $\overline{\text{ALERT}}$. Functions as $\overline{\text{ALERT0}}$ pin.
01b = GPIO digital input. Read data from register SMBUS_SETTINGS as input to this pin. (default)
10b = GPIO digital output. Write data from this pin as output to register SMBUS_SETTINGS.
11b = SLOW. Functions as SLOW pin. Pulling the pin high overrides the programmed sample rate and results in a sampling rate of 8 sps (Slow mode). Configuring the pin as SLOW pin takes priority over other settings, including GPIO Triggered mode.

bit 7:5 **AVERAGE**[2:0]: Selects how many samples are included in rolling average.

000b = 4
001b = 8 (default)
010b = 16
011b = 32
100b = Reserved. Do not select this option.
101b = 64
110b = Reserved. Do not select this option.
111b = 128

bit 4 **AA**: Configures Adaptive Accumulation, which emulates a sample mode of 8,192 sps for all samples rates when using the Slow function. The Adaptive Accumulation function works in conjunction with the SAMPLE_MODE[3:0] bits.
For more details, see **Section 4.8.1** and **Section 4.8.2**.

0b = Disables adaptive accumulation. The results in the accumulation register do not change when the SLOW pin is pulled high (default).
1b = Enables adaptive accumulation. The results in the accumulation register change when the SLOW pin is pulled high to match results obtained at 8,192 sps.

bit 3:2 **ACC_CONFIG**[1:0]: Configures accumulator to sum V_{POWER} calculations or V_{SENSE} or V_{BUS} samples.

00b = Accumulator sums V_{POWER} calculations (default)
01b = Accumulator sums V_{SENSE} measurements
10b = Accumulator sums V_{BUS} measurements
11b = Reserved. Do not select this option.

bit 1:0 **AUTO_REFRESH**[1:0]: Configures Auto-refresh. A Refresh (any) command occurs after a conversion cycle completes. In Single-shot Average sample mode, a Refresh (any) command occurs only after the configured number of samples are averaged (8 samples by default). This is controlled by the AVERAGE[2:0] bits in this register.
While Auto-refresh is enabled, manual Refresh (any) commands are ignored. Disabling the feature allows PAC1811 to execute manual Refresh (any) commands.
When Auto-refresh is enabled, functional changes are not applied. Before modifying register values, ensure Auto-refresh is disabled. Auto-refresh can be re-enabled afterwards.

00b = Disables Auto-refresh. Requires manual Refresh (any) commands (default).
01b = Enables Auto-refresh. Resets accumulator and accumulator count.
PAC1811 executes a Limited Refresh to move V_{BUS}, V_{SENSE}, V_{POWER}, accumulator data and accumulator count to the I^2C domain.
10b = Enables Auto-refresh. Does not reset accumulator and accumulator count.
PAC1811 executes a Limited Refresh_V to move V_{BUS}, V_{SENSE}, V_{POWER}, accumulator data and accumulator count to the I^2C domain.
11b = Reserved. Do not select this option.

REGISTER 6-17: NEG_PWR_FSR_LAT (ADDRESS 10H)

U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
–	–	–	–	CFG_VS[1:0]		CFG_VB[1:0]	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	X = Bit is unknown

This register contains a copy of register NEG_PWR_FSR. The bits in this register reflect the settings that were active before the most recent Refresh (any) command.
The values in register NEG_PWR_FSR can be programmed, but not yet activated by a Refresh (any) command, while the values in the NEG_PWR_FSR_ACT register are the currently active settings.
The NEG_PWR_FSR_LAT register shows the settings that were active prior to the most recent Refresh (any) command and therefore, the settings correspond to the dataset stored in the readable registers.
This register is valid when the results registers are valid, one conversion cycle after a Refresh (any) command.

bit 7:4 Unimplemented at this time. Always reads **0**.

bit 3:2 **CFG_VS**[1:0]: Configure FSR for V_{SENSE} measurements.

00b = V_{SENSE} is in Unipolar 0-FSR mode: 0V to +100 mV FSR (default)
01b = V_{SENSE} is in Bipolar ± FSR mode: –100 mV to +100 mV FSR
10b = V_{SENSE} is in Bipolar ± FSR/2 mode: –50 mV to +50 mV FSR/2
11b = Reserved

bit 1:0 **CFG_VB**[1:0]: Configure FSR for V_{BUS} measurements.

00b = V_{BUS} is in Unipolar 0-FSR mode: 0V to +42V FSR (default)
01b = V_{BUS} is in Bipolar ± FSR mode: –42V to +42V FSR
10b = V_{BUS} is in Bipolar ± FSR/2 mode: –21V to +21V FSR/2
11b = Reserved

REGISTER 6-18: ALERT_STATUS (ADDRESS 11H)

U-0	U-0	RC-0	RC-0	RC-0	RC-0	RC-0	RC-0
–	–	RV	FV	RC	FC	OC	UC
bit 15							bit 8

RC-0	RC-0	RC-0	RC-0	RC-0	RC-0	U-0	U-0
OV	UV	OPC	OPW	ACC_OVF	ACC_COUNT	–	–
bit 7							bit 0

Legend:			
RC = Readable only bit. Cleared when read and the conversion cycle completes.			
W = Writable bit		U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	X = Bit is unknown

Read this register to determine the cause of an alert. For more details, see **Section 4.10.3**.
This register is cleared when read and another conversion cycle completes. If the condition that triggered the alert is still present when the conversion cycle completes, the bit associated with that type of alert remains set.
The register updates without requiring a Refresh (any) command.
The overcurrent, undercurrent, overpower, overvoltage and undervoltage alerts are disabled by default. To enable these alerts, set the corresponding bits in the ALERT_ENABLE register.

Note: No alert shows up in the ALERT_STATUS register unless it is first enabled in the ALERT_ENABLE register.

bit 15:14 Unimplemented at this time. Always reads **0**.

bit 13 **RV**: Status of the Fast Rising Voltage alert.

0b = Alert for Fast Rising Voltage is not triggered
1b = Alert for Fast Rising Voltage was triggered

bit 12 **FV**: Status of the Fast Falling Voltage alert.

0b = Alert for Fast Falling Voltage is not triggered
1b = Alert for Fast Falling Voltage was triggered

bit 11 **RC**: Status of the Fast Rising Current alert.

0b = Alert for Fast Rising Current is not triggered
1b = Alert for Fast Rising Current was triggered

bit 10 **FC**: Status of the Fast Falling Current alert.

0b = Alert for Fast Falling Current is not triggered
1b = Alert for Fast Falling Current was triggered

bit 9 **OC**: Status of the Overcurrent alert.

0b = Alert for Overcurrent is not triggered
1b = Alert for Overcurrent was triggered

bit 8 **UC**: Status of the Undercurrent alert.

0b = Alert for Undercurrent is not triggered
1b = Alert for Undercurrent was triggered

bit 7 **OV**: Status of the Overvoltage alert.

0b = Alert for Overvoltage is not triggered
1b = Alert for Overvoltage was triggered

bit 6 **UV**: Status of the Undervoltage alert.

0b = Alert for Undervoltage is not triggered
1b = Alert for Undervoltage was triggered

bit 5 **OPC**: Status of the Overpower Critical alert.

0b = Alert for Overpower Critical is not triggered
1b = Alert for Overpower Critical was triggered

bit 4 **OPW**: Status of the Overpower Warning alert.

0b = Alert for Overpower Warning is not triggered
1b = Alert for Overpower Warning was triggered

bit 3 **ACC_OVF**: This bit signals when the accumulator overflows or exceeds its fullness limit specified in the ACC_FULL_LIMIT register.

0b = Alert for Accumulator Overflow is not triggered
1b = Alert for Accumulator Overflow was triggered

bit 2 **ACC_COUNT**: This bit signals when the accumulator count overflows or exceeds its fullness limit specified in the ACC_FULL_LIMIT register.

0b = Alert for Accumulator Count is not triggered
1b = Alert for Accumulator Count was triggered

bit 1:0 Unimplemented at this time. Always reads **0**.

REGISTER 6-19: SMBUS_SETTINGS (ADDRESS 12H)

R/W-0	R/W-0	R-0	R/W-1	R/W-0	R/W-0	U-0	R/W-0
GPIO_DATA1	GPIO_DATA0	ANY_ALERT	POR	TIMEOUT	BYTE_COUNT	–	I2C_HISPEED
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	X = Bit is unknown

This register is used to activate the SMBus functionality. It is also used to store I/O data for R/$\overline{W}$ on I/O pins.
Bits in this register can be written or read at any time and are active immediately.
A Refresh (any) command is not required to activate the settings or update the register.

bit 7 **GPIO_DATA1**: R/W data for pin A1. GPIO/$\overline{ALERT}$ function if pin A1 is configured as GPIO pin.
If the A1 pin is configured as a GPIO input, then **0b** = low and **1b** = high.
For more details on how to configure pin A1 as GPIO pin, see Register 6-2.

Note 1: To write to this bit, the A1 pin must be set as GPIO output pin, else PAC1811 ignores the Write command.

2: When pin A1 is selected as $\overline{ALERT}$ pin, this bit becomes read-only.

3: While the default for this bit is **0b**, the hardware setup impacts its initial value. For example, if pin A1 is externally pulled high, the initial value of the GPIO_DATA1 bit upon reading is **1b**.

4: When pin A1 is not configured as GPIO output, the input value is stored in this bit. This includes when pin A1 is connected to the VDD, SDA, SCL or GND pin.

0b = Pulls the A1 pin low when configured to be a GPIO output (default).
1b = Pulls the A1 pin high to the external pull-up voltage using an external resistor when the A1 pin is configured as GPIO output.

bit 6 **GPIO_DATA0**: R/W data for pin A0. GPIO/$\overline{ALERT}$ function if pin A0 is configured as GPIO pin.
If the A0 pin is configured as a GPIO input, then **0b** = low and **1b** = high.
For more details on how to configure pin A0 as GPIO pin, see Register 6-2.

Note 1: To write to this bit, the A1 pin must be set as GPIO output pin, else PAC1811 ignores the Write command.

2: When pin A0 is selected as $\overline{ALERT}$ pin, this bit becomes read-only.

3: While the default for this bit is **0b**, the hardware setup impacts its initial value. For example, if pin A0 is externally pulled high, the initial value of the GPIO_DATA0 bit upon reading is **1b**.

4: When pin A0 is not configured as GPIO output, the input value is displayed in this bit. This includes when pin A0 is connected to the VDD, SDA, SCL or GND pin.

0b = Pulls the A0 pin low when configured to be a GPIO output (default).
1b = Pulls the A0 pin high to the external pull-up voltage using an external resistor when the A0 pin is configured as GPIO output.

bit 5 **ANY_ALERT**: This bit is set when any active alert triggers, except for the Conversion Complete alert. Clearing the alert that set the ANY_ALERT bit also clear the bit. For more details, see **Section 4.10.1**.

0b = No ALERT condition occurred. (default)
1b = An ALERT condition occurred.

bit 4 **POR**: This bit allows to determine if PAC1811 reset after it was programmed.
This bit can be cleared after a POR event and then used to determine if PAC1811 was powered cycled or reset since the latest POR event.
If a reset is detected in this manner, any non-default programming can be reconfigured.
This bit is reset only by an internal POR event.

0b = This bit was cleared over I^2C since the latest POR event occurred.
1b = A POR event occurred and this bit was not cleared since then. (default)

bit 3 **TIMEOUT**: Enable or disable the SMBus timeout functionality. For more details, see **Section 5.2**.

0b = Disables SMBus timeout. (default)
1b = Enables SMBus timeout.

bit 2 **BYTE COUNT**: This bit enables the response to the SMBus Block Read command for each register read to include the byte count data. For more details, see **Section 5.6.9**.

0b = No byte count data included in the response to a Block Read command. (default)
1b = Byte count data included in the response to a Block Read command.

bit 1 Unimplemented at this time. Always reads **0**.

bit 0 **I2C_HISPEED**: This bit enables 3.4 MHz I^2C High-speed mode operation by changing the pulse width parameters of the Spike Suppression (t_{SP}) from a maximum of 50 ns to 10 ns.
High-speed mode allows the SMBus clock to run at 3.4 MHz.

Note: Due to the changes to communication parameters when entering and exiting High-speed mode, do not program this bit as part of a Block Write. If this bit is disabled, PAC1811 NACKs the sent command, but the command is still accepted.

0b = PAC1811 operates in 1 MHz I^2C Fast-mode Plus mode. (default)
1b = PAC1811 operates in 3.4 MHz I^2C High-speed mode.

REGISTER 6-20: NEG_PWR_FSR (ADDRESS 13H)

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
–	–	–	–	CFG_VS[1:0]		CFG_VB[1:0]	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	X = Bit is unknown

This register is used to configure FSR for V_{BUS} and/or V_{SENSE}.
Bipolar ranges for V_{BUS} and V_{SENSE} enable the measurement of bipolar voltages and currents.
Issue a Refresh (any) command to copy NEG_PWR_FSR register settings to the NEG_PWR_FSR_ACT register.

bit 7:4 Unimplemented at this time. Always reads **0**.

bit 3:2 **CFG_VS**[1:0]: Configure FSR for V_{SENSE} measurements.

00b = V_{SENSE} is in Unipolar 0-FSR mode: 0V to +100 mV FSR (default)
01b = V_{SENSE} is in Bipolar ± FSR mode: –100 mV to +100 mV FSR
10b = V_{SENSE} is in Bipolar ± FSR/2 mode: –50 mV to +50 mV FSR/2
11b = Reserved

bit 1:0 **CFG_VB**[1:0]: Configure FSR for V_{BUS} measurements.

00b = V_{BUS} is in Unipolar 0-FSR mode: 0V to +42V FSR (default)
01b = V_{BUS} is in Bipolar ± FSR mode: –42V to +42V FSR
10b = V_{BUS} is in Bipolar ± FSR/2 mode: –21V to +21V FSR/2
11b = Reserved

REGISTER 6-21: REFRESH_G (ADDRESS 14H)

SEND	SEND	SEND	SEND	SEND	SEND	SEND	SEND
No data in this command, Send Byte only							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	X = Bit is unknown

This command is a Send Byte and does not contain any data.
It is intended for use with the General Call Address command. PAC1811 executes the Refresh_G command upon reception. Accumulator data, accumulator count, V_{BUS} and V_{SENSE} measurements are all updated, while accumulator and accumulator count are reset.
The host can read the updated data anytime following a Refresh_G command issued after a completed conversion cycle and until the next Refresh (any) command is issued.

REGISTER 6-22: REFRESH_V (ADDRESS 15H)

SEND	SEND	SEND	SEND	SEND	SEND	SEND	SEND
No data in this command, Send Byte only							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	X = Bit is unknown

This command is a Send Byte and does not contain any data.
PAC1811 executes the Refresh_V command upon reception. Accumulator data, accumulator count, V_{BUS} and V_{SENSE} measurements are all updated without resetting the accumulator or accumulator count.
The host can read the updated data anytime following a Refresh_V command issued after a completed conversion cycle and until the next Refresh (any) command is issued.

REGISTER 6-23: SLOW (ADDRESS 16H)

R-0	R-0	R-0	R/$\overline{W}$-0	R/$\overline{W}$-0	R/$\overline{W}$-0	R/$\overline{W}$-0	U-0
SLOW	SLOW_LH	SLOW_HL	R_RISE	R_V_RISE	R_FALL	R_V_FALL	–
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	X = Bit is unknown

This register tracks the state of the SLOW pin and transitions that occur on this pin.
It also controls the type of Limited refresh commands (if any) that occur on SLOW pin transitions. This enables the monitoring of the SLOW pin state and its transitions over I^2C, even though the SLOW pin is asynchronous to the I^2C pins (SDA and SCL) and can have a different I^2C Controller.
Values newly written to the register are activate only after sending a Refresh (any) command.
On a SLOW pin transition, a Limited Refresh command can be executed if bits R_V_FALL, R_FALL, R_V_RISE and R_RISE are set to **1b**.
These Limited Refresh and Refresh_V commands update all of the readable results registers.
The Limited Refresh command also resets the accumulators and accumulator count. These are called Limited Refresh and Limited Refresh_V commands because there is no activation of any pending changes to configuration registers.

Note: If a Limited Refresh and Limited Refresh_V command are both enabled for a specific SLOW pin transition, only the Refresh command is executed. Refresh overrides Refresh_V.

bit 7 **SLOW**: Check the status of the SLOW pin.

0b = SLOW pin pulled low.
1b = SLOW pin pulled high.

bit 6 **SLOW_LH**: Tracks if the SLOW pin transitioned from low to high since the last Refresh (any) command. The bit is reset to **0** by a Refresh or Refresh_G command.

0b = SLOW pin did not transition from low to high since the last Refresh (any) command.
1b = SLOW pin transitioned from low to high since the last Refresh (any) command.

bit 5 **SLOW_HL**: Tracks if the SLOW pin transitioned from high to low since the last Refresh (any) command. The bit is reset to **0** by a Refresh or Refresh_G command.

0b = SLOW pin did not transition from high to low since the last Refresh (any) command.
1b = SLOW pin transitioned from high to low since the last Refresh (any) command.

bit 4 **R_RISE**: Configure if a Limited Refresh command is executed on the rising edge of the SLOW pin. The bit is not reset automatically. Write to the bit to change its value.

0b = Disallows Limited Refresh commands to execute on the rising edge of the SLOW pin. (default)
1b = Allows Limited Refresh commands to execute on the rising edge of the SLOW pin.

bit 3 **R_V_RISE**: Configure if a Limited Refresh_V command is executed on the rising edge of the SLOW pin. The bit is not reset automatically. Write to the bit to change its value.

0b = Disallows Limited Refresh_V commands to execute on the rising edge of the SLOW pin. (default)
1b = Allows Limited Refresh_V commands to execute on the rising edge of the SLOW pin.

bit 2 **R_FALL**: Configure if a Limited Refresh command is executed on the falling edge of the SLOW pin. The bit is not reset automatically. Write to the bit to change its value.

0b = Disallows Limited Refresh commands to execute on the falling edge of the SLOW pin. (default)
1b = Allows Limited Refresh commands to execute on the falling edge of the SLOW pin.

bit 1 **R_V_FALL**: Configure if a Limited Refresh_V command is executed on the falling edge of the SLOW pin. The bit is not reset automatically. Write to the bit to change its value.

0b = Disallows Limited Refresh_V commands to execute on the falling edge of the SLOW pin. (default)
1b = Allows Limited Refresh_V commands to execute on the falling edge of the SLOW pin.

bit 0 Unimplemented at this time. Always reads **0**.

REGISTER 6-24: CONTROL_ACT (ADDRESS 17H)

R-0	R-0	R-1	R-0	R-0	R-1	R-0	R-1
SAMPLE_MODE[3:0]				GPIO_ALERT1[1:0]		SLOW_ALERT0[1:0]	
bit 15							bit 8

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R-0	R-0	R-0	R-0	R-0	R-0	R-0
AVERAGE[2:0]			AA	ACC_CONFIG[1:0]		AUTO_REFRESH[1:0]	
bit 7						bit 0	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	X = Bit is unknown

This register contains copy of the CONTROL register. This register reflects the settings that are currently active.
The values in the CONTROL register can be programmed, but not yet activated by a Refresh (any) command, while the values in the CONTROL_LAT register are the settings active before receiving a Refresh (any) command.
This register allows to determine the actual active settings.
This register becomes valid when the results registers are valid following a Refresh (any) command issued after a conversion cycle completes. However, when changing the sample rate followed by a Refresh command, the sample rate does not change until the current conversion cycle completes. In some cases, this can cause a delay before the conversion cycle and the CONTROL_ACT register update. This delay can be variable, depending on when in the conversion cycle the Refresh command is executed.

bit 15:12 **SAMPLE_MODE**[3:0]: Selects one of the sample modes listed below. These modes are exclusive – only one mode can be set at any given time.
One of the sample rate options is Sleep state for when no sampling occurs.
When switching sample modes during a conversion cycle, the ADC continues the current sample mode until the conversion completes and then switches to the new sample mode. Registers CONTROL and CONTROL_ACT update.
Switching from a Continuous sample mode to a Single-shot mode triggers an extra conversion cycle.
When using a GPIO Triggered sample mode, first configure the desired pin (A0 or A1) as an input by setting the SLOW_ALERT0[1:0] or GPIO_ALERT1[1:0] bits to **01b**.

0000b = 8,192 sps (see **Section 4.8.1**)
0001b = 4,096 sps
0010b = 1,024 sps (default)
0011b = 256 sps
0100b = 64 sps
0101b = 8 sps (Slow mode) (see **Section 4.2.8**)
0110b = Single-shot mode (see **Section 4.9.1**)
0111b = Single-shot Average mode
1000b = Single-shot Awake mode
1001b = Single-shot Awake Average mode
1010b = V_{BUS} Only at 16,384 sps (see **Section 4.2.9**)
1011b = V_{SENSE} Only at 16,384 sps (see **Section 4.2.9**)
1100b = GPIO (A0) Triggered Single-shot Awake mode, Edge (see **Section 4.9.1.4**)
1101b = GPIO (A1) Triggered Single-shot Awake mode, Edge (see **Section 4.9.1.4**)
1110b = Sleep state (see **Section 4.2.6**)
1111b = Sleep state (see **Section 4.2.6**)

bit 11:10 **GPIO_ALERT1**[1:0]: Selects the signals for the A1 pin, GPIO/$\overline{\text{ALERT}}$ function.
If pin A1 is configured as GPIO pin, the R/W data for the pin is stored in register SMBUS_SETTINGS.
While the A1 pin is multifunction, Microchip recommends using A1 as GPIO/$\overline{\text{ALERT}}$ pin.

00b = $\overline{\text{ALERT}}$. Functions as $\overline{\text{ALERT1}}$ pin.
01b = GPIO digital input. Read data from register SMBUS_SETTINGS as input to this pin. (default)
10b = GPIO digital output. Write data from this pin as output to register SMBUS_SETTINGS.
11b = SLOW. Functions as SLOW pin. Pulling the pin high overrides the programmed sample rate and results in a sample rate of 8 sps (Slow mode). Configuring the pin as SLOW pin takes priority over other settings, including GPIO Triggered mode.

bit 9:8 **SLOW_ALERT0**[1:0]: Selects the signals for the A0 pin, SLOW/$\overline{\text{ALERT}}$ function.
If pin A0 is configured as GPIO pin, the R/W data for the pin is stored in register SMBUS_SETTINGS.
While the A0 pin is multifunction, Microchip recommends using A0 as SLOW/$\overline{\text{ALERT}}$ pin.

00b = $\overline{\text{ALERT}}$. Functions as $\overline{\text{ALERT0}}$ pin.
01b = GPIO digital input. Read data from register SMBUS_SETTINGS as input to this pin. (default)
10b = GPIO digital output. Write data from this pin as output to register SMBUS_SETTINGS.
11b = SLOW. Functions as SLOW pin. Pulling the pin high overrides the programmed sample rate and results in a sampling rate of 8 sps (Slow mode). Configuring the pin as SLOW pin takes priority over other settings, including GPIO Triggered mode.

bit 7:5 **AVERAGE**[2:0]: Selects how many samples are included in rolling average.

000b = 4
001b = 8 (default)
010b = 16
011b = 32
100b = Reserved. Do not select this option.
101b = 64
110b = Reserved. Do not select this option.
111b = 128

bit 4 **AA**: Configures Adaptive Accumulation, which emulates a sample mode of 8,192 sps for all samples rates when using the Slow function. The Adaptive Accumulation function works in conjunction with the SAMPLE_MODE[3:0] bits.
For more details, see **Section 4.8.1** and **Section 4.8.2**.

0b = Disables adaptive accumulation. The results in the accumulation register do not change when the SLOW pin is pulled high (default).
1b = Enables adaptive accumulation. The results in the accumulation register change when the SLOW pin is pulled high to match results obtained at 8,192 sps.

bit 3:2 **ACC_CONFIG**[1:0]: Configures accumulator to sum V_{POWER} calculations or V_{SENSE} or V_{BUS} samples.

00b = Accumulator sums V_{POWER} calculations (default)
01b = Accumulator sums V_{SENSE} measurements
10b = Accumulator sums V_{BUS} measurements
11b = Reserved. Do not select this option.

bit 1:0 **AUTO_REFRESH**[1:0]: Configures Auto-refresh. A Refresh (any) command occurs after a conversion cycle completes. In Single-shot Average sample mode, a Refresh (any) command occurs only after the configured number of samples are averaged (8 samples by default). This is controlled by the AVERAGE[2:0] bits in this register.
While Auto-refresh is enabled, manual Refresh (any) commands are ignored. Disabling the feature allows PAC1811 to execute manual Refresh (any) commands.
When Auto-refresh is enabled, functional changes are not applied. Before modifying register values, ensure Auto-refresh is disabled. Auto-refresh can be re-enabled afterwards.

00b = Disables Auto-refresh. Requires manual Refresh (any) commands (default).
01b = Enables Auto-refresh. Resets accumulator and accumulator count.
PAC1811 executes a Limited Refresh to move V_{BUS}, V_{SENSE}, V_{POWER}, accumulator data and accumulator count to the I^2C domain.
10b = Enables Auto-refresh. Does not reset accumulator and accumulator count.
PAC1811 executes a Limited Refresh_V to move V_{BUS}, V_{SENSE}, V_{POWER}, accumulator data and accumulator count to the I^2C domain.
11b = Reserved. Do not select this option.

REGISTER 6-25: NEG_PWR_FSR_ACT (ADDRESS 18H)

U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
–	–	–	–	CFG_VS[1:0]		CFG_VB[1:0]	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	X = Bit is unknown

This register contains an image of the NEG_PWR_FSR. This register reflects the settings that are currently active. The values in the NEG_PWR_FSR register can be programmed, but not yet activated by a Refresh (any) command, while the values in the NEG_PWR_FSR_LAT register are the settings active before receiving a Refresh (any) command.
This register allows to determine the actual active settings.
This register becomes valid when the results registers are valid following a Refresh (any) command issued after a conversion cycle completes.

bit 7:4 Unimplemented at this time. Always reads **0**.

bit 3:2 **CFG_VS**[1:0]: Configure FSR for V_{SENSE} measurements.

00b = V_{SENSE} is in Unipolar 0-FSR mode: 0V to +100 mV FSR (default)
01b = V_{SENSE} is in Bipolar ± FSR mode: –100 mV to +100 mV FSR
10b = V_{SENSE} is in Bipolar ± FSR/2 mode: –50 mV to +50 mV FSR/2
11b = Reserved

bit 1:0 **CFG_VB**[1:0]: Configure FSR for V_{BUS} measurements.

00b = V_{BUS} is in Unipolar 0-FSR mode: 0V to +42V FSR (default)
01b = V_{BUS} is in Bipolar ± FSR mode: –42V to +42V FSR
10b = V_{BUS} is in Bipolar ± FSR/2 mode: –21V to +21V FSR/2
11b = Reserved

REGISTER 6-26: SLOW_ALERT0 (ADDRESS 19H)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
–	–	RV	FV	RC	FC	OC	UC
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
OV	UV	OPC	OPW	ACC_OVF	ACC_COUNT	ALERT_CC0	–
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	X = Bit is unknown

Write to this register to assign a specific alert signal to pin A0. $\overline{\text{ALERT0}}$ function.
Any changes to this register become active after a Refresh (any) command is sent.

Note 1: For the SLOW_ALERT0 register to control the A0 pin, the pin must be programmed for the alert function in the CONTROL register. For more details, see **Section 4.10.1**.

2: Ensure alerts are enabled in the ALERT_ENABLE register before routing the alerts to this pin.

3: Ensure alerts are disabled in the ALERT_ENABLE register before changing any limits to avoid false triggers.

bit 15:14 Unimplemented at this time. Always reads **0**.

bit 13 **RV**: Configures the Fast Rising Voltage alert.

0b = Disables the Fast Rising Voltage alert.
1b = Enables the Fast Rising Voltage alert.

bit 12 **FV**: Configures the Fast Falling Voltage alert.

0b = Disables the Fast Falling Voltage alert.
1b = Enables the Fast Falling Voltage alert.

bit 11 **RC**: Configures the Fast Rising Current alert.

0b = Disables the Fast Rising Current alert.
1b = Enables the Fast Rising Current alert.

bit 10 **FC**: Configures the Fast Falling Current alert.

0b = Disables the Fast Falling Current alert.
1b = Enables the Fast Falling Current alert.

bit 9 **OC**: Configures the Overcurrent alert.

0b = Disables the Overcurrent alert.
1b = Enables the Overcurrent alert.

bit 8 **UC**: Configures the Undercurrent alert.

0b = Disables the Undercurrent alert.
1b = Enables the Undercurrent alert.

bit 7 **OV**: Configures the Overvoltage alert.

0b = Disables the Overvoltage alert.
1b = Enables the Overvoltage alert.

bit 6 **UV**: Configures the Undervoltage alert.

0b = Disables the Undervoltage alert.
1b = Enables the Undervoltage alert.

bit 5 **OPC**: Configures the Overpower Critical alert.

0b = Disables the Overpower Critical alert.
1b = Enables the Overpower Critical alert.

bit 4 **OPW**: Configures the Overpower Warning alert.

0b = Disables the Overpower Warning alert.
1b = Enables the Overpower Warning alert.

bit 3 **ACC_OVF**: Configure the Accumulator Overflow alert. This alert triggers when the accumulator overflows or exceeds its fullness limit specified in the ACC_FULL_LIMIT register.

0b = Disables the Accumulator Overflow alert
1b = Enables the Accumulator Overflow alert

bit 2 **ACC_COUNT**: Configures the Accumulator Count Overflow alert. This alert triggers when the accumulator count overflows or exceeds its fullness limit specified in ACC_FULL_LIMIT register.

0b = Disables the Accumulator Count Overflow alert.
1b = Enables the Accumulator Count Overflow alert.

bit 1 **ALERT_CC0**: Configures the Conversion Complete alert, where the A0 pin is pulled high for 5 µs at the end of each conversion cycle.

Note 1: The A0 pin must be configured as an $\overline{\text{ALERT}}$ pin for this function to trigger.

2: The SLOW function is not available on the A0 pin when it is configured as an $\overline{\text{ALERT}}$ pin. For more details, see **Section 4.10.2**.

0b = Disables the Conversion Complete alert.
1b = Enables the Conversion Complete alert.

bit 0 Unimplemented at this time. Always reads **0**.

REGISTER 6-27: GPIO_ALERT1 (ADDRESS 1AH)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
–	–	RV	FV	RC	FC	OC	UC
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
OV	UV	OPC	OPW	ACC_OVF	ACC_COUNT	ALERT_CC1	–
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	X = Bit is unknown

Write to this register to assign a specific alert signal to the A1 pin. GPIO/$\overline{\text{ALERT1}}$ function.
Any changes to this register become active after a Refresh (any) command is sent.

Note 1: For the GPIO_ALERT1 register to control the A1 pin, the pin must be programmed for the alert function in the CONTROL register. For more details, see **Section 4.10.1**.

2: Ensure alerts are enabled in the ALERT_ENABLE register before routing the alerts to this pin.

3: Ensure alerts are disabled in the ALERT_ENABLE register before changing any limits to avoid false triggers.

bit 15:14 Unimplemented at this time. Always reads **0**.

bit 13 **RV**: Configures the Fast Rising Voltage alert.

0b = Disables the Fast Rising Voltage alert.
1b = Enables the Fast Rising Voltage alert.

bit 12 **FV**: Configures the Fast Falling Voltage alert.

0b = Disables the Fast Falling Voltage alert.
1b = Enables the Fast Falling Voltage alert.

bit 11 **RC**: Configures the Fast Rising Current alert.

0b = Disables the Fast Rising Current alert.
1b = Enables the Fast Rising Current alert.

bit 10 **FC**: Configures the Fast Falling Current alert.

0b = Disables the Fast Falling Current alert.
1b = Enables the Fast Falling Current alert.

bit 9 **OC**: Configures the Overcurrent alert.

0b = Disables the Overcurrent alert.
1b = Enables the Overcurrent alert.

bit 8 **UC**: Configures the Undercurrent alert.

0b = Disables the Undercurrent alert.
1b = Enables the Undercurrent alert.

bit 7 **OV**: Configures the Overvoltage alert.

0b = Disables the Overvoltage alert.
1b = Enables the Overvoltage alert.

bit 6 **UV**: Configures the Undervoltage alert.

0b = Disables the Undervoltage alert.
1b = Enables the Undervoltage alert.

bit 5 **OPC**: Configures the Overpower Critical alert.

0b = Disables the Overpower Critical alert.
1b = Enables the Overpower Critical alert.

bit 4 **OPW**: Configures the Overpower Warning alert.

0b = Disables the Overpower Warning alert.
1b = Enables the Overpower Warning alert.

bit 3 **ACC_OVF**: Configure the Accumulator Overflow alert. This alert triggers when the accumulator overflows or exceeds its fullness limit specified in the ACC_FULL_LIMIT register.

0b = Disables the Accumulator Overflow alert
1b = Enables the Accumulator Overflow alert

bit 2 **ACC_COUNT**: Configures the Accumulator Count Overflow alert. This alert triggers when the accumulator count overflows or exceeds its fullness limit specified in ACC_FULL_LIMIT register.

0b = Disables the Accumulator Count Overflow alert.
1b = Enables the Accumulator Count Overflow alert.

bit 1 **ALERT_CC1**: Configures the Conversion Complete alert, where the A1 pin is pulled high for 5 µs at the end of each conversion cycle.

Note 1: The A1 pin must be configured as an $\overline{\text{ALERT}}$ pin for this function to trigger.

2: The SLOW function is not available on the A1 pin when it is configured as an $\overline{\text{ALERT}}$ pin. For more details, see **Section 4.10.2**.

0b = Disables the Conversion Complete alert.
1b = Enables the Conversion Complete alert.

bit 0 Unimplemented at this time. Always reads **0**.

REGISTER 6-28: ACC_FULL_LIMIT (ADDRESS 1BH)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
ACC_FULL[5:0]						ACC_COUNT_FULL[1:0]	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'**1**' = Bit is set	'**0**' = Bit is cleared	X = Bit is unknown

This register is used to set a limit for how full the VACC and ACC_COUNT registers can be before the Accumulator Overflow and Accumulator Count Oveflow alerts are triggered.
Any changes to this register become active after a Refresh (any) command is sent.
Disable alerts in the ALERT_ENABLE register before making changes to the ACC_FULL_LIMIT register to avoid false triggers.

bit 7:2 **ACC_FULL**[5:0]: These six bits are configurable to match the six MSBs of the VACC register.
An alert triggers when the six MSBs of the VACC register ≥ the 6-bit value stored in ACC_FULL_LIMIT register.
In bipolar mode, an alert triggers if the absolute value of the VACC register is more negative or more positive than the set limit. Setting this register to **3Fh** does not generate an alert as this the maximum value that can be stored in the VACC register.

bit 1:0 **ACC_COUNT_FULL**[1:0] Configure the fullness limit for the ACC_COUNT register.

00b = 100% Full
01b = 15/16 (~ 93%) Full (default)
10b = 7/8 (~ 87%) Full
11b = 3/4 (75%) Full

REGISTER 6-29: OC_LIMIT (ADDRESS 1CH)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OC_LIMIT[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	X = Bit is unknown

bit 7:0 **OC_LIMIT**[7:0]: Configure the overcurrent (OC) limit as a 2's complement number for all current modes (unipolar or bipolar).

Note: Disable alerts in the ALERT_ENABLE register before making changes to the OC_LIMIT register to avoid false triggers.

REGISTER 6-30: UC_LIMIT (ADDRESS 1DH)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
UC_LIMIT[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	X = Bit is unknown

bit 7:0 **UC_LIMIT**[7:0]: Configure the undercurrent (UC) limit as a 2's complement number for all current modes (unipolar or bipolar).

Note: Disable alerts in the ALERT_ENABLE register before making changes to the UC_LIMIT register to avoid false triggers.

REGISTER 6-31: OP_WARNING_LIMIT (ADDRESS 1EH)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OP_WARNING_LIMIT[15:8]							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OP_WARNING_LIMIT[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	X = Bit is unknown

bit 7:0 **OP_WARNING_LIMIT**[15:0]: Configure the overpower (OP) warning limit as a 2's complement number for all current modes (unipolar or bipolar). This register functions as any limit register. However, it is intended to provide a warning when overpower conditions occur.

Note: Disable alerts in the ALERT_ENABLE register before making changes to the OP_WARNING_LIMIT register to avoid false triggers.

REGISTER 6-32: OP_CRITICAL_LIMIT (ADDRESS 1FH)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OP_CRITICAL_LIMIT[15:8]							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OP_CRITICAL_LIMIT[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	X = Bit is unknown

bit 7:0 **OP_CRITICAL_LIMIT**[15:0]: Configure the overpower (OP) critical limit as a 2's complement number for all current modes (unipolar or bipolar). This register functions as any limit register. However, it is intended to provide a critical limit for overpower conditions.

Note: Disable alerts in the ALERT_ENABLE register before making changes to the OP_CRITICAL_LIMIT register to avoid false triggers.

REGISTER 6-33: OV_LIMIT (ADDRESS 20H)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OV_LIMIT[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	X = Bit is unknown

bit 7:0 **OV_LIMIT**[7:0]: Configure the overvoltage (OV) limit as a 2's complement number for all current modes (unipolar or bipolar).

Note: Disable alerts in the ALERT_ENABLE register before making changes to the OV_LIMIT register to avoid false triggers.

REGISTER 6-34: UV_LIMIT (ADDRESS 21H)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
UV_LIMIT[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	X = Bit is unknown

bit 7:0 **UV_LIMIT**[7:0]: Configure the undervoltage (UV) limit as a 2's complement number for all current modes (unipolar or bipolar).

Note: Disable alerts in the ALERT_ENABLE register before making changes to the UV_LIMIT register to avoid false triggers.

REGISTER 6-35: STEP_LIMIT (ADDRESS 22H)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RV[1:0]		FV[1:0]		RC[1:0]		FC[1:0]	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	X = Bit is unknown

This register detects changes in the voltage or current average value. The value that is currently stored in the VBUS_AVG or VSENSE_AVG register is compared to the previously stored value.
This average value is programmable.

Note 1: The STEP_LIMIT register uses VBUS_AVG and VSENSE_AVG data. These two registers use full signed values for ADC data regardless of the settings in the NEG_PWR_FSR register. This can results in an unexpected step limit excursion.

2: Disable alerts in the ALERT_ENABLE register before making changes to the STEP_LIMIT register to avoid false triggers.

bit 7:6 **RV**[1:0]: Configure Rising Voltage limit.
When V_{BUS} increases, the new average value is checked to determine if the voltage increase is greater than the previous average stored in the VBUS_AVG register by a certain percent.

00b = 25% (default)
01b = 50%
10b = 75%
11b = 100%

bit 5:4 **FV**[1:0]: Configure Falling Voltage limit.
When V_{BUS} decreases, the new average value is checked to determine if the voltage decrease is lesser than the previous average stored in the VBUS_AVG register by a certain percent.

00b = 25% (default)
01b = 50%
10b = 75%
11b = 100%

bit 3:2 **RC**[1:0]: Configure Rising Current limit.
When V_{SENSE} increases, the new average value is checked to determine if the voltage increase is greater than the previous average stored in the VSENSE_AVG register by a certain percent.

00b = 25% (default)
01b = 50%
10b = 75%
11b = 100%

bit 1:0 **FC**[1:0]: Configure Falling Current limit.
When V_{SENSE} decreases, the new average value is checked to determine if the voltage decrease is lesser than the previous average stored in the VSENSE_AVG register by a certain percent.

00b = 25% (default)
01b = 50%
10b = 75%
11b = 100%

REGISTER 6-36: N-SAMPLES_LIMIT (ADDRESS 23H)

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
–	–	–	–	N-SAMPLES_OPC[1:0]		N-SAMPLES_OPW[1:0]	
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
N-SAMPLES_OC[1:0]		N-SAMPLES_UC[1:0]		N-SAMPLES_OV[1:0]		N-SAMPLES_UV[1:0]	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	X = Bit is unknown

This register sets the N-Samples limit that specifies how many samples must exceed the threshold before triggering an alert. The register is not reset until a conversion cycle is complete and the alert condition is cleared. After an alert is cleared, the N-SAMPLES_LIMIT register is reset.

Note: Disable alerts in the ALERT_ENABLE register before making changes to the N-SAMPLES_LIMIT register to avoid false triggers.

bit 15:12 Unimplemented at this time. Always reads **0**.

bit 11:10 **N-SAMPLES_OPC**[1:0]: Configure the number of consecutive samples that must exceed the set threshold before triggering the Overpower Critical alert.

00b = 1 sample (default)
01b = 4 samples
10b = 8 samples
11b = 16 samples

bit 9:8 **N-SAMPLES_OPW**[1:0]: Configure the number of consecutive samples that must exceed the set threshold before triggering the Overpower Warning alert.

00b = 1 sample (default)
01b = 4 samples
10b = 8 samples
11b = 16 samples

bit 7:6 **N-SAMPLES_OC**[1:0]: Configure the number of consecutive samples that must exceed the set threshold before triggering the Overcurrent alert.

00b = 1 sample (default)
01b = 4 samples
10b = 8 samples
11b = 16 samples

bit 5:4 **N-SAMPLES_UC**[1:0]: Configure the number of consecutive samples that must exceed the set threshold before triggering the Undercurrent alert.

00b = 1 sample (default)
01b = 4 samples
10b = 8 samples
11b = 16 samples

bit 3:2 **N-SAMPLES_OV**[1:0]: Configure the number of consecutive samples that must exceed the set threshold before triggering the Overvoltage alert.

00b = 1 sample (default)
01b = 4 samples
10b = 8 samples
11b = 16 samples

bit 1:0 **N-SAMPLES_UV**[1:0]: Configure the number of consecutive samples that must exceed the set threshold before triggering the Undervoltage alert.

00b = 1 sample (default)
01b = 4 samples
10b = 8 samples
11b = 16 samples

REGISTER 6-37: ALERT_ENABLE (ADDRESS 24H)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
–	–	RV	FV	RC	FC	OC	UC
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
OV	UV	OPC	OPW	ACC_OVF	ACC_COUNT	ALERT_CC	–
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	X = Bit is unknown

This register enables or disables alert functions. For more details, see **Section 4.10.3**.
Any changes to this register become active after a Refresh (any) command is sent.

Note 1: Alerts must be enabled in this register before they can be routed to an $\overline{\text{ALERT}}$ pin.

2: Disable alerts in this register before modifying any of the limit registers (OC_LIMIT, UC_LIMIT, OV_LIMIT, UV_LIMIT, OP_WARNING_LIMIT, OP_CRITICAL_LIMIT, STEP_LIMIT and N-SAMPLES_LIMIT) to avoid false triggers.

bit 15:14 Unimplemented at this time. Always reads **0**.

bit 13 **RV**: Configures the Fast Rising Voltage alert.

0b = Disables the Fast Rising Voltage alert.
1b = Enables the Fast Rising Voltage alert.

bit 12 **FV**: Configures the Fast Falling Voltage alert.

0b = Disables the Fast Falling Voltage alert.
1b = Enables the Fast Falling Voltage alert.

bit 11 **RC**: Configures the Fast Rising Current alert.

0b = Disables the Fast Rising Current alert.
1b = Enables the Fast Rising Current alert.

bit 10 **FC**: Configures the Fast Falling Current alert.

0b = Disables the Fast Falling Current alert.
1b = Enables the Fast Falling Current alert.

bit 9 **OC**: Configures the Overcurrent alert.

0b = Disables the Overcurrent alert.
1b = Enables the Overcurrent alert.

bit 8 **UC**: Configures the Undercurrent alert.

0b = Disables the Undercurrent alert.
1b = Enables the Undercurrent alert.

bit 7 **OV**: Configures the Overvoltage alert.

0b = Disables the Overvoltage alert.
1b = Enables the Overvoltage alert.

bit 6 **UV**: Configures the Undervoltage alert.

0b = Disables the Undervoltage alert.
1b = Enables the Undervoltage alert.

bit 5 **OPC**: Configures the Overpower Critical alert.

0b = Disables the Overpower Critical alert.
1b = Enables the Overpower Critical alert.

bit 4 **OPW**: Configures the Overpower Warning alert.

0b = Disables the Overpower Warning alert.
1b = Enables the Overpower Warning alert.

bit 3 **ACC_OVF**: Configure the Accumulator Overflow alert.

0b = Disables the Accumulator Overflow alert.
1b = Enables the Accumulator Overflow alert.

bit 2 **ACC_COUNT**: Configures Accumulator Count Overflow alert.

0b = Disables the Accumulator Count Overflow alert.
1b = Enables the Accumulator Count Overflow alert.

bit 1 **ALERT_CC**: Configures the alert for when a conversion cycle is complete.

0b = Disables the conversion cycle complete alert.
1b = Enables the conversion cycle complete alert.

bit 0 Unimplemented at this time. Always reads **0**.

REGISTER 6-38: ACC_COUNT_PRESET (ADDRESS 25H)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ACC_COUNT_PRE[15:8]							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ACC_COUNT_PRE[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	X = Bit is unknown

bit 15:0 **ACC_COUNT_PRE**[15:0]: Configure the preset value for the ACC_COUNT register.
The default value of this register is **0h**, but can be programmed to any value.
The preset value is a 16-bit number that represents the MSBs of the ACC_COUNT register.
Anytime the ACC_COUNT register is reset, PAC1811 sets its new value to the value stored in the ACC_COUNT_PRESET register. When the ACC_COUNT register starts incrementing, it starts from the preset value.
A Refresh or Refresh_V command is required for new preset values to take effect.

REGISTER 6-39: VACC_PRESET (ADDRESS 26H)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ACCUM_PRE[15:8]							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ACCUM_PRE[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	X = Bit is unknown

bit 15:0 **ACCUM_PRE**[15:0]: Configure the preset value for the VACC register.
The default value of this register is **0h**, but can be programmed to any value.
The preset value is a 16-bit number that represents the MSBs of the VACC register.
Anytime the VACC register is reset, PAC1811 sets its new value to the preset value stored in the VACC_PRESET register. When the VACC register starts incrementing, it starts from the preset value.
A Refresh or Refresh_V command is required for new preset values to take effect.

REGISTER 6-40: PRODUCT_ID (ADDRESS FDH)

R-1	R-0	R-0	R-0	R-0	R-1	R-0	R-0
PID[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	X = Bit is unknown

bit 7:0 **PID**[7:0]: This register contains the Product ID for PAC1811 and is set to **84h**.

REGISTER 6-41: MANUFACTURER_ID (ADDRESS FEH)

R-0	R-1	R-0	R-1	R-0	R-1	R-0	R-0
MID[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	X = Bit is unknown

bit 7:0 **MID**[7:0]: This register identifies Microchip as the manufacturer of PAC1811 and is set to **54h**.

REGISTER 6-42: REVISION_ID (ADDRESS FFH)

R-0	R-0	R-0	R-0	R-0	R-1	R-0	R-0
RID[7:0]							
bit 7							bit 0

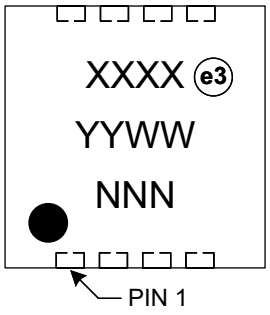
Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	X = Bit is unknown

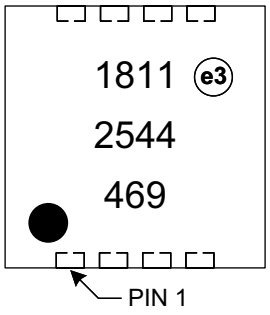
bit 7:0 **RID**[7:0]: This register identifies the PAC1811 die revision as **04h**.

7.0 PACKAGING INFORMATION

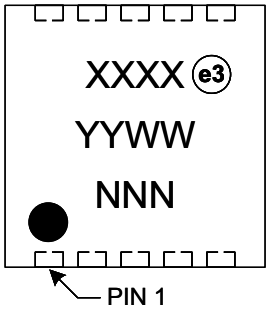
7.1 Package Marking Information

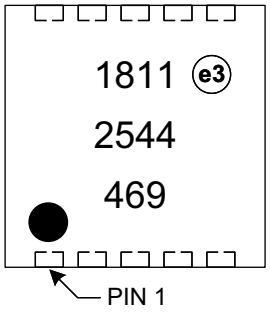
8-Lead 3x3 mm VDFN **Example:**





10-Lead 3x3 mm VDFN **Example:**





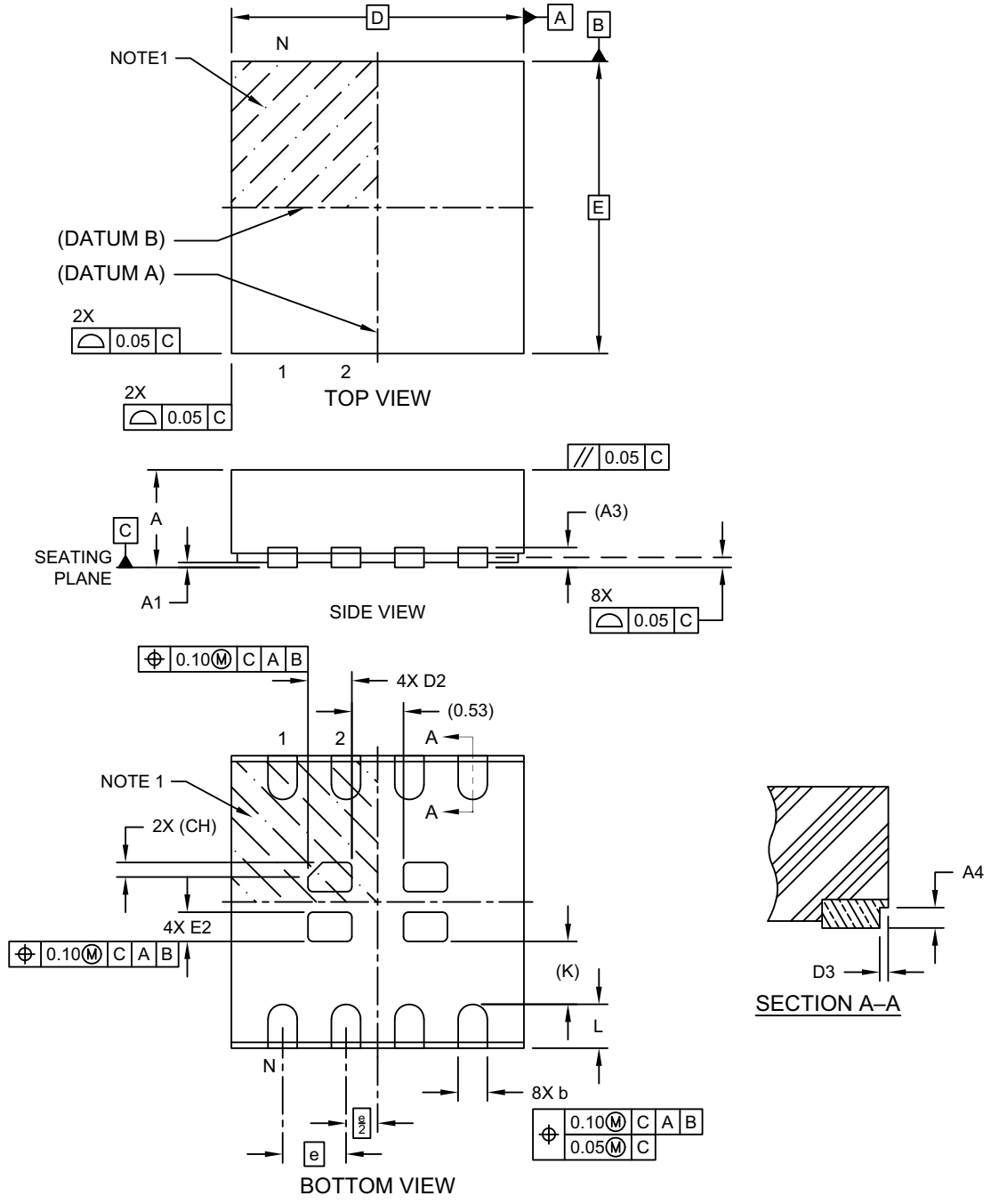
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

7.2 Package Drawings

8-Lead Very Thin Plastic Dual Flat, No Lead Package (3PW) - 3x3x1.0 mm Body [VDFN] With Multiple Exposed Pad and Stepped Wettable Flanks

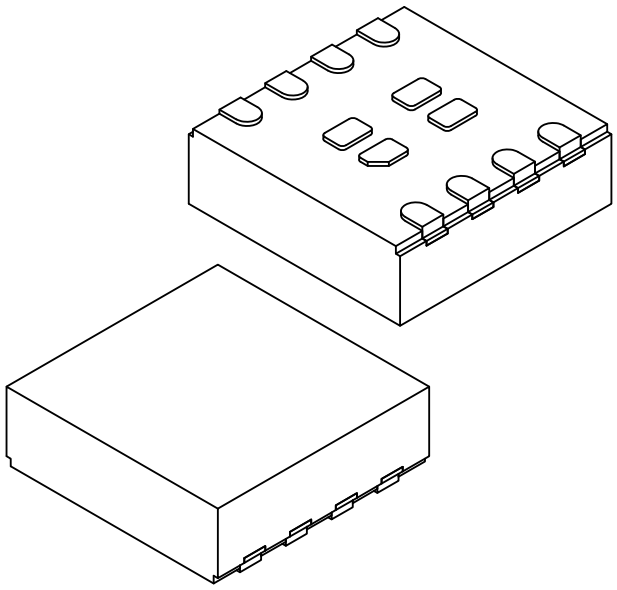
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-568 Rev B Sheet 1 of 2

8-Lead Very Thin Plastic Dual Flat, No Lead Package (3PW) - 3x3x1.0 mm Body [VDFN] With Multiple Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Length	D		3.00 BSC	
Exposed Pad Length	D2	0.35	0.45	0.55
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	0.20	0.30	0.40
Index Corner Chamfer	CH		0.15 REF	
Terminal Width	b	0.25	0.30	0.35
Terminal Length	L	0.35	0.45	0.55
Terminal-to-Exposed-Pad	K		0.65 REF	
Wettable Flank Step Cut Length	D3	0.035	0.060	0.085
Wettable Flank Step Cut Height	A4	0.10	-	0.19

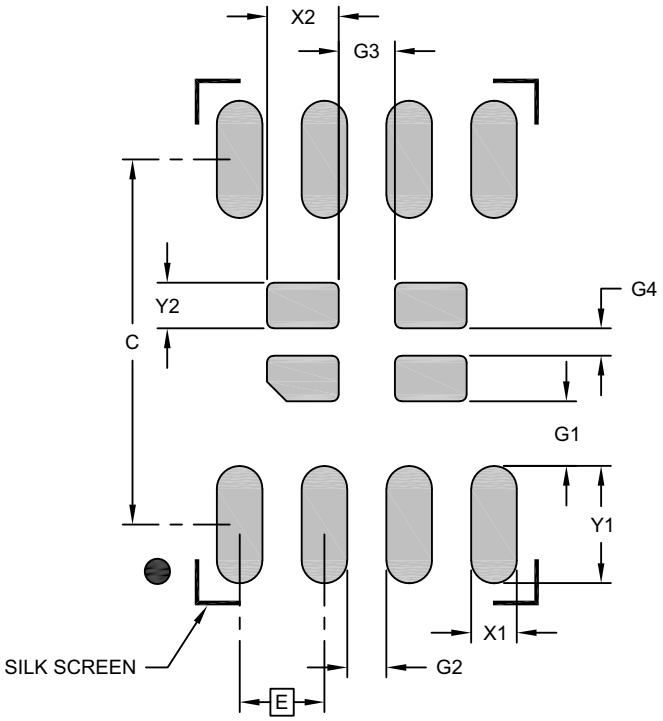
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-568 Rev B Sheet 2 of 2

8-Lead Very Thin Plastic Dual Flat, No Lead Package (3PW) - 3x3x1.0 mm Body [VDFN] With Multiple Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Center Pad Width (X4)	X2			0.55
Center Pad Length (X4)	Y2			0.35
Contact Pad Spacing	C		2.80	
Contact Pad Width (X8)	X1			0.35
Contact Pad Length (X8)	Y1			0.90
Contact Pad to Center Pad (X8)	G1	0.50		
Contact Pad to Contact Pad (X6)	G2	0.30		
Center Pad to Center Pad	G3	0.43		
Center Pad to Center Pad	G4	0.21		

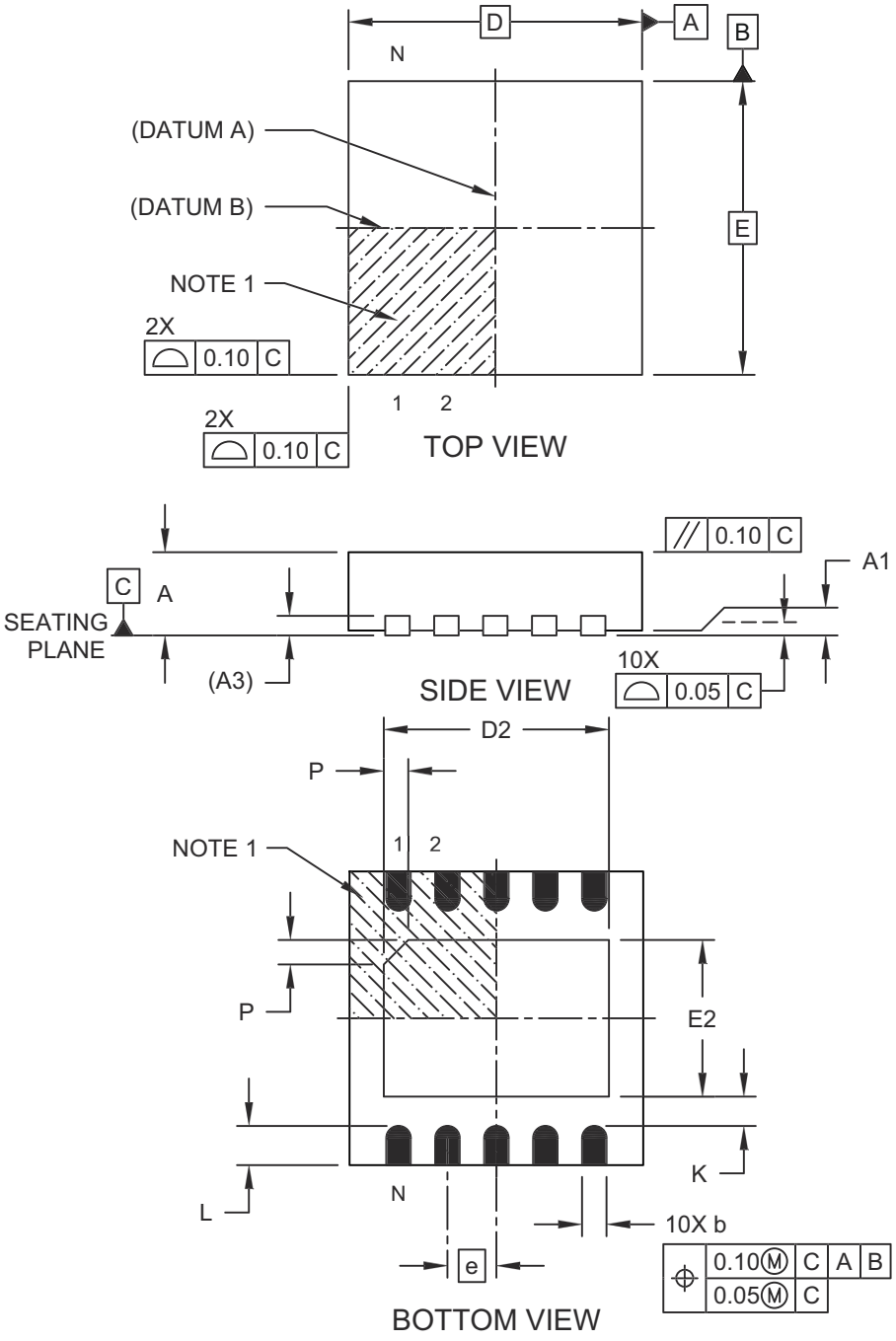
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2568 Rev B

10-Lead Very Thin Plastic Dual Flat, No Lead Package (9QX) - 3x3 mm Body [VDFN]

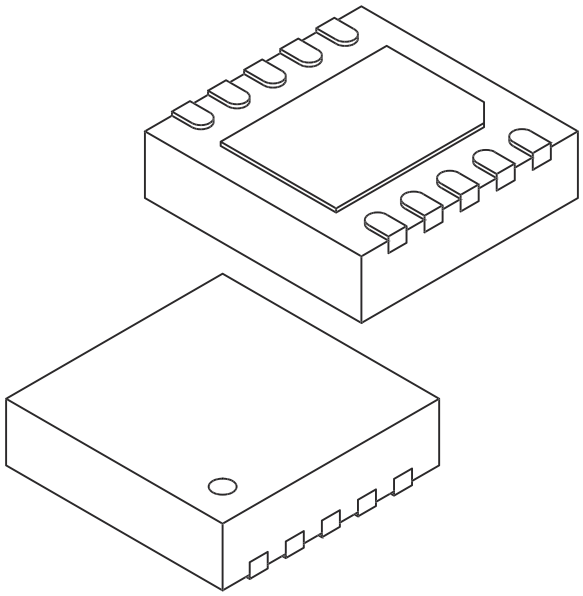
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-00206 Rev D Sheet 1 of 2

10-Lead Very Thin Plastic Dual Flat, No Lead Package (9QX) - 3x3 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		10	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	(A3)		0.20 REF	
Overall Length	D		3.00 BSC	
Exposed Pad Length	D2	2.20	2.30	2.40
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.50	1.60	1.70
Exposed Pad Chamfer	P	-	0.25	-
Terminal Width	b	0.18	0.25	0.30
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.25	0.30	-

Notes:

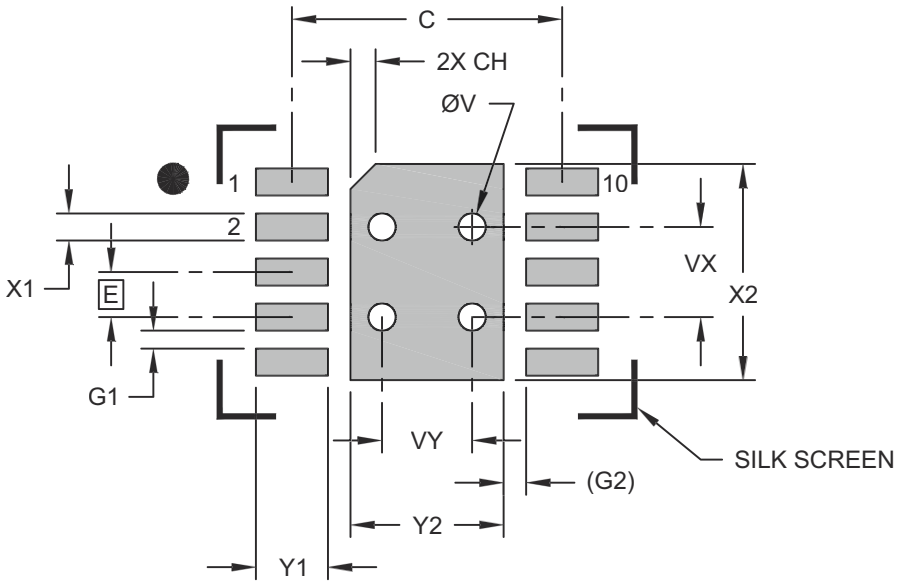
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-00206 Rev D Sheet 2 of 2

10-Lead Very Thin Plastic Dual Flat, No Lead Package (9QX) - 3x3 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	Y2			1.70
Optional Center Pad Length	X2			2.40
Contact Pad Spacing	C		3.00	
Center Pad Chamfer	CH		0.28	
Contact Pad Width (X10)	X1			0.30
Contact Pad Length (X10)	Y1			0.80
Contact Pad to Contact Pad (X8)	G1	0.20		
Contact Pad to Center Pad (X10)	G2		0.25 REF	
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	VX		1.00	
Thermal Via Pitch	VY		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerances, for reference only.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-02206 Rev D

APPENDIX A: REVISION HISTORY

Revision A (November 2025)

- Initial release of this document.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X[1]	-X	X	/XX	[XXX]
Device	Tape and Reel	Device Option	Temperature Range	Package	Class

Device:	PAC1811	=	Single-Channel Power Monitor with Accumulator, 42V Full Scale Range
Tape and Reel Option[1]:	T	=	Tape and Reel
Device Option	1	=	High-Side Power Monitor
	2	=	High-Side or Low-Side Power Monitor with Hardware Power-down
Temperature Range:	E	=	-40°C to +125°C (Extended)
Package:	3P	=	Very Thin Plastic Dual Flat, No Lead (3PW), 3x3 mm body, 8-Lead (VDFN) with Multiple Exposed Pad and Stepped Wettable Flanks
	9Q	=	Very Thin Plastic Dual Flat, No Lead (9QX), 3x3 mm body, 10-Lead (VDFN)
Class:	Blank	=	Non-automotive
	VAO	=	Automotive

Examples:

a) PAC1811T-1E/3P = Single-Channel Power Monitor, Tape and Reel, High-Side, Extended Temperature, 8-Lead VDFN Package

b) PAC1811T-2E/9Q = Single-Channel Power Monitor, Tape and Reel, High-Side or Low-Side with Hardware Power-down, Extended Temperature, 10-Lead VDFN Package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

PRODUCT IDENTIFICATION SYSTEM (AUTOMOTIVE)

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X[(1)]	-X	X	/XX	[XXX]
Device	Tape and Reel	Device Option	Temperature Range	Package	Class

Device:	PAC1811	=	Single-Channel Power Monitor with Accumulator, 42V Full Scale Range
Tape and Reel Option[(1)]:	T	=	Tape and Reel
Device Option	1	=	High-Side Power Monitor
	2	=	High-Side or Low-Side Power Monitor with Hardware Power-down
Temperature Range:	E	=	-40°C to +125°C (Extended)
Package:	3P	=	Very Thin Plastic Dual Flat, No Lead (3PW), 3x3 mm body, 8-Lead (VDFN) with Multiple Exposed Pad and Stepped Wettable Flanks
	9Q	=	Very Thin Plastic Dual Flat, No Lead (9QX), 3x3 mm body, 10-Lead (VDFN)
Class:	Blank	=	Non-automotive
	VAO	=	Automotive

Examples:

a) PAC1811T-1E/3PVAO = Single-Channel Power Monitor, Tape and Reel, High-Side, Extended Temperature, 8-Lead VDFN Package, Automotive

b) PAC1811T-2E/9QVAO = Single-Channel Power Monitor, Tape and Reel, High-Side or Low-Side with Hardware Power-down, Extended Temperature, 10-Lead VDFN Package, Automotive

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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