NEH7100

Inductorless energy harvesting PMIC with battery protection, LDO, USB charging and I²C

Rev. 1 — 17 December 2024 Product data sheet

1. General description

The NEH7100 is a high-performance power management IC (PMIC) for energy harvesting solutions in low-power applications. It has a rich set of auxiliary features, such as storage element protection, USB charging and LDO / load switch.

The NEH7100 is optimized to harvest energy from light sources (from a wide range of indoor and outdoor PV cells). Other energy sources can also be used, such as kinetic (movement, vibrations), thermal variation and electromagnetic, but might need external auxiliary components. The NEH7100 gathers energy from a suitable harvester to charge a storage element, such as a rechargeable battery or a supercapacitor.

Nexperia's advanced maximum power point tracking (MPPT) uses an embedded hill-climbing algorithm to deliver maximum power to the storage element. The MPPT is compatible with any suitable harvester, and optimizes efficiency as frequent as every 0.5 seconds for excellent performance in rapidly changing harvesting conditions.

The NEH7100 is available in 28-lead, 4 mm x 4 mm HVQFN28 package.

2. Features and benefits

- Harvesting power range: 15 μW to 50 mW
- Ultra-fast MPPT interval
- Battery protection features:
  - Over-voltage protection (OVP)
  - Low-voltage detection (LVD)
  - Over-current protection (OCP)
- USB charging up to 200 mA
- LDO with configurable output voltage
- Configurable via hard-coding or I²C
- Coldstart, supporting "battery-less" design
- Small BOM with no inductor required
- Suitable for batteries, supercapacitors and hybrid capacitors

3. Applications

- Smart remote controls: TV, gaming, AV control, key-fob
- Wireless PC devices: keyboard, mouse, headphones
- Industrial sensors: electronic shelf labels, asset trackers and beacons
- Tire pressure sensors
- Wearable devices: watch, body band and health devices

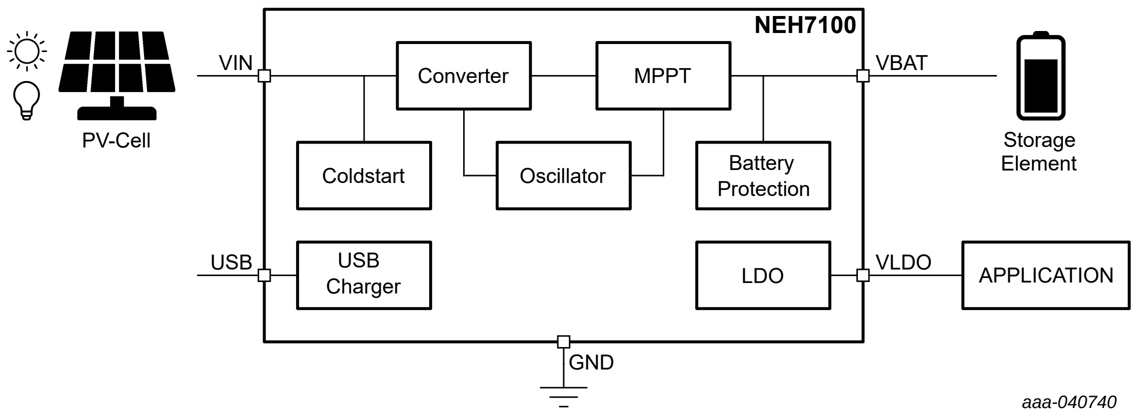

Fig. 1. NEH7100 typical solar energy harvesting system

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
NEH7100BU	-40 °C to 85 °C	HVQFN28	plastic, leadless thermal enhanced very thin quad flat package; 28 terminals;0.4 mm pitch; 4 mm x 4 mm x 0.85 mm body	SOT8080-1

5. Pinning information

5.1. Pinning configuration

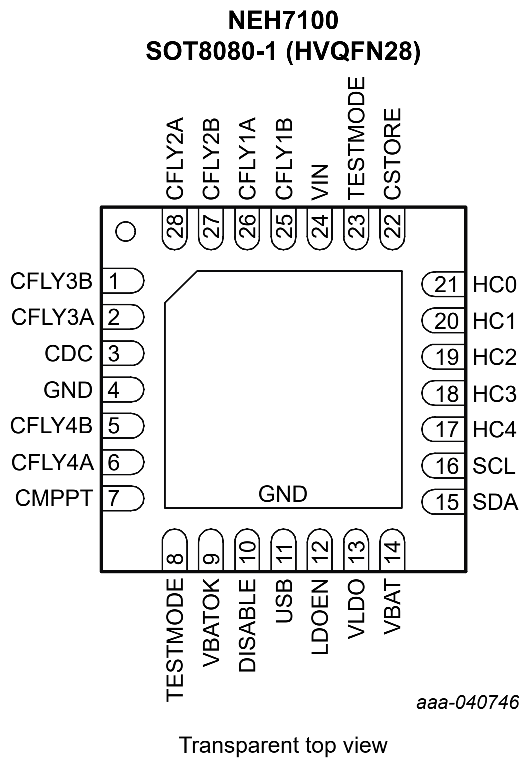

Fig. 2. SOT8080-1 (HVQFN28) 4 mm x 4 mm package

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5.2. Pinning description

Table 2. Pinning description

Pin	Symbol	Description
1	CFLY3B	flying-capacitor terminal B, 3rd stage
2	CFLY3A	flying-capacitor terminal A, 3rd stage
3	CDC	boost converter filter capacitor
4	GND	ground
5	CFLY4B	flying-capacitor terminal B, 4th stage
6	CFLY4A	flying-capacitor terminal A, 4th stage
7	CMPPT	filter capacitor for MPPT
8	TESTMODE	reserved; should be left floating
9	VBATOK	indicates if battery voltage is above configured LVD level
10	DISABLE	active high. Disable mode sets the device in low-power consumption. Connect to GND to enable, connect to V_{BAT} to disable.
11	USB	USB 5V input for charging storage element connected to V_{BAT}.
12	LDOEN	LDO enable, active high. Connect to V_{BAT} level to enable. Connect to GND to disable
13	VLDO	LDO output. LDO input is internally connected to VBAT. Connect to application load.
14	VBAT	output of the energy harvester and power supply for PMIC. Connect storage element to this pin.
15	SDA	I²C serial data input / output
16	SCL	I²C serial clock input
17	HC4	hard-code bit [4]. Connect to GND for a logic low, to CSTORE for a logic high
18	HC3	hard-code bit [3]. Connect to GND for a logic low, to CSTORE for a logic high
19	HC2	hard-code bit [2]. Connect to GND for a logic low, to CSTORE for a logic high
20	HC1	hard-code bit [1]. Connect to GND for a logic low, to CSTORE for a logic high
21	HC0	hard-code bit [0]. Connect to GND for a logic low, to CSTORE for a logic high
22	CSTORE	internal supply pin
23	TESTMODE	reserved; should be left either floating or connected to GND
24	VIN	input for connecting a harvester
25	CFLY1B	flying-capacitor terminal B, 1st stage
26	CFLY1A	flying-capacitor terminal A, 1st stage
27	CFLY2B	flying-capacitor terminal B, 2nd stage
28	CFLY2A	flying-capacitor terminal A, 2nd stage
PAD	GND	ground pad, should be connected to ground plane with vias

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6. Specifications

6.1. Absolute maximum ratings

Table 3. Absolute maximum ratings

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{PC}	power converter pins: CFLY1x, CFLY2x		-0.3	2.0	V
	power converter pins: CFLY3x, CFLY4x, CDC, CMPPT, CSTORE		-0.3	5.5	V
V_{CONFIG}	configuration pins: DISABLE, LDOEN, SDA, SCL, HCx		-0.3	5.5	V
V_{IN}	input pin: VIN	using bench power supply with low series resistance	-0.3	2.0	V
		using PV-cell or current-limited source	-0.3	5.5	V
V_{POWER}	power pins: VBAT, USB		-0.3	5.5	V
I_{IN}	input current (VIN pin)		-	140	mA
T_j	junction temperature		-50	+125	°C
T_{stg}	storage temperature		-65	+150	°C

6.2. ESD ratings

Table 4. ESD ratings

Symbol	Parameter	Conditions	Value	Unit
V_{ESD}	electrostatic discharge voltage	HBM: ANSI/ESDA/JEDEC JS-001	± 2000	V
		CDM: ANSI/ESDA/JEDEC JS-002	± 500	V

6.3. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BAT}	battery voltage		0	-	4.5	V
T_{amb}	ambient temperature		-40	-	+85	°C

6.4. Thermal information

Table 6. Thermal characteristics

Symbol	Parameter	SOT8080-1	Unit
$R_{\theta(ja)}$	junction-to-ambient thermal resistance	57.8	°C/W
$R_{\theta(jc)}$	junction-to-case (top) thermal resistance	73.4	°C/W
$\Psi_{(jt)}$	junction-to-case (top) thermal characterization parameter	25.1	°C/W

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6.5. Electrical characteristics

Table 7. Electrical characteristics

V_{BAT} = 3.7 V. Typical values specified at T_{amb} = 25 °C, Min and Max values specified at T_{amb} = –40 °C to 85 °C. Voltages are referenced to GND (ground = 0 V). V_{MPP} represents the maximum power point voltage at VIN.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies and start-up						
V_{BAT}	battery voltage	To start device with input power on V_{IN}	0		4.5	V
		Minimum voltage to start device without input power on V_{IN}	-	2.9	3.6	V
		Minimum voltage required to keep device running after start and without power on V_{IN}	-	2	-	V
$I_{DISABLE}$	disable mode current	$V_{DISABLE} = V_{BAT}$	-	13	150	nA
I_Q	quiescent current (LDO disabled)	no input power, V_{IN} is floating; LDO disabled	-	1.5	5	μA
$I_{Q(LDO)}$	quiescent current (LDO enabled)	no input power, V_{IN} is floating; LDO enabled	-	2.1	6.5	μA
t_{start}	start-up time	time from applying V_{BAT} to rising edge of VBATOK; No input power on V_{IN}	-	720	-	ms
Power converter						
η	nominal efficiency	V_{MPP} = 2 V	-	94	-	%
		V_{MMP} = 1 V	-	90	-	%
		V_{MPP} = 0.5 V	-	85	-	%
		V_{MPP} = 0.25 V	-	75	-	%
$P_{IN(low)}$	input power range, low end	efficiency = 70%; V_{MPP} = 2 V	-	65	-	μW
		efficiency = 60%; V_{MPP} = 1 V	-	55	-	μW
		efficiency = 50%; V_{MPP} = 0.5 V	-	45	-	μW
		efficiency = 40%; V_{MPP} = 0.25 V	-	53	-	μW
$P_{IN(high)}$	input power range, high end	efficiency = 70%; V_{MPP} = 2 V	-	69	-	mW
		efficiency = 60%; V_{MPP} = 1 V	-	52	-	mW
		efficiency = 50%; V_{MPP} = 0.5 V	-	23	-	mW
		efficiency = 40%; V_{MPP} = 0.25 V	-	10	-	mW
$V_{IN(min)}$	minimum input voltage	Main converter active, cold start inactive; efficiency ≥ 40%. I_{IN} = 1 mA	-	0.23	-	V
$f_{CONV(low)}$	frequency at low-end power		-	30	-	kHz
$f_{CONV(high)}$	frequency at high-end power		-	1.1	-	MHz
t_{MPPT}	MPPT interval	Set values (Table 8)	0.5		64	sec
$t_{MPPT(acc)}$	MPPT interval inaccuracy		-	10	-	%
Cold start						
$V_{IN(CS)}$	minimum V_{IN} cold start voltage	P_{IN} > 12 μW	-	270	-	mV
$P_{IN\_CS(min)}$	minimum cold start input power	V_{IN} = 270 mV	-	12	-	μW

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Battery protection						
V_{BAT_OVP}	over-voltage protection (OVP)	Set value (see Table 17)	2.7	-	4.5	V
V_{BAT_LVD}	low-voltage detection (LVD)	Set value (see Table 18)	2.2	-	3.7	V
$V_{BAT(acc)}$	over-voltage protection (OVP) and low-voltage detection (LVD) threshold inaccuracy		-	-1	-	%
$V_{LVD(hys)}$	low-voltage detection (LVD) hysteresis	Voltage difference between LVD falling and rising threshold	-	150	-	mV
USB features						
USB_OVP	USB over-voltage	Set value (see Table 17)	2.7	-	4.5	V
USB_OCP	USB over-current	Set value (see Table 13)	0.5	-	200	mA
I_{BAT}	storage element charging current via USB		-	0.8 × setting	-	mA
$V_{BAT(acc)}$	storage element over-voltage inaccuracy via USB	5 V on USB pin	-	-1	-	%
$I_{BAT(acc)}$	storage element charging current inaccuracy	5 V on USB pin; relative to 0.8 × setting	-	-6	-	%
LDO features						
V_{LDO}	LDO voltage	Set value (see Table 14)	1.2	-	3.6	V
$V_{LDO(acc)}$	LDO voltage inaccuracy	I_{LDO} = 1 mA	-	-1	-	%
$I_{LDO(max)}$	maximum LDO output current	V_{BAT} = VLDO_nom + 0.5 V; $V_{BAT(min)}$ = 2.5 V	-	200	-	mA
$V_{LDO(drop)}$	LDO dropout voltage	I_{LDO} = 200mA	-	130	-	mV
t_{LDO_on}	LDO turn-on time	from LDO_EN rising edge until V_{LDO} = 95%; I_{LDO} = 200 mA; V_{LDO} = 3.6 V; V_{BAT} = 4 V	-	0.5	-	s
$\Delta V_{LDO(line)}$	LDO line regulation	V_LDO inaccuracy over V_{BAT} range. I_{LDO} = 1 mA; 2.5 V < V_{BAT} < 4.5 V and V_{BAT} > V_{LDO} + 0.5 V	-	0.2	-	%
$\Delta I_{LDO(load)}$	LDO load regulation	V_LDO inaccuracy over I_{LDO} range. I_{LDO} < 200 mA; V_{BAT} = $V_{LDO(nom)}$ + 0.5 V; $V_{BAT(min)}$ = 2.5 V	-	-1.5	-	%
I²C parameters						
I²C_addr	I²C address			3C		hex
$V_{DD(I^2C)}$	I²C bus voltage		1.2	-	4.5	V
V_{IL}	SDA/SCL input logic low level		-	-	0.5	V
V_{IH}	SDA/SCL input logic high level		1.0	-	-	V
V_{OL}	SDA output logic low level	I_{SDA} = 3 mA	-	-	0.4	V
f_{SCL}	SCL clock frequency		-	-	100	kHz
t_{LOW}	low period of SCL clock		4.7	-	-	µs
t_{HIGH}	high period of SCL clock		4.0	-	-	µs
t_{HD}	data hold time		300	-	-	ns
t_{SU}	data set-up time		250	-	-	ns

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Logic levels						
$V_{OL\_BATOK(low)}$	VBATOK output logic low level	I_{sink} = 1 mA	-	-	0.2	V
$V_{OH\_BATOK(high)}$	VBATOK output logic high level	I_{source} = 1 mA	V_{BAT} - 0.4	-	-	V
$V_{IL\_LDOEN(low)}$	LDO enable pin (LDOEN) input logic low level		-	-	0.5	V
$V_{IH\_LDOEN(high)}$	LDO enable pin (LDOEN) input logic high level		1	-	-	V
$V_{IL\_DIS(low)}$	DISABLE input logic low level		-	-	0.4	V
$V_{IH\_DIS(high)}$	DISABLE input logic high level		V_{BAT} - 0.4	-	-	V

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6.6. Typical characteristics

At recommended operating conditions; V_{BAT} = 3.7 V; typical values are at 25°C (unless otherwise noted). V_{MPP} represents the maximum power point voltage at VIN.

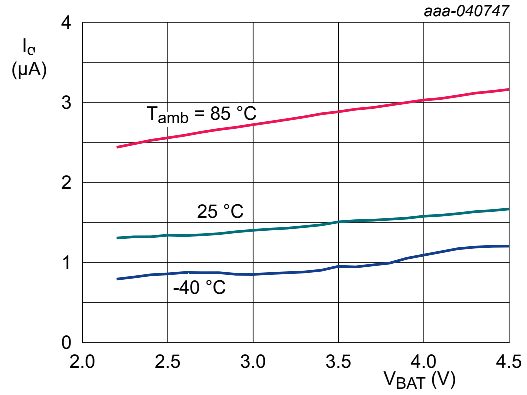

Fig. 3. Quiescent current vs. V_{BAT} over temperature, LDO disabled

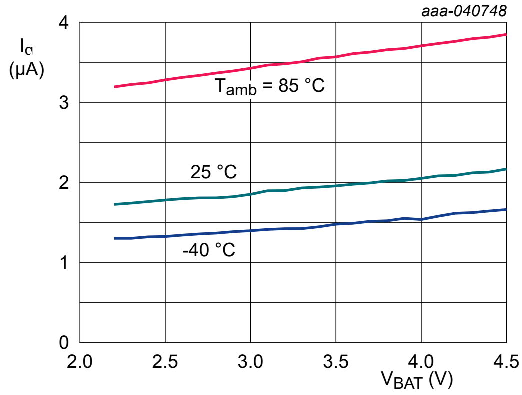

Fig. 4. Quiescent current vs. V_{BAT} over temperature, LDO enabled

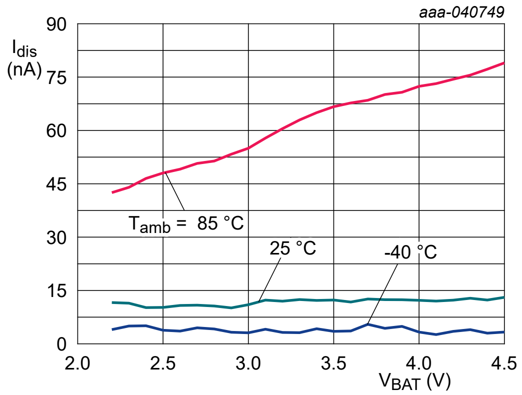

Fig. 5. Disable current vs. V_{BAT} over temperature

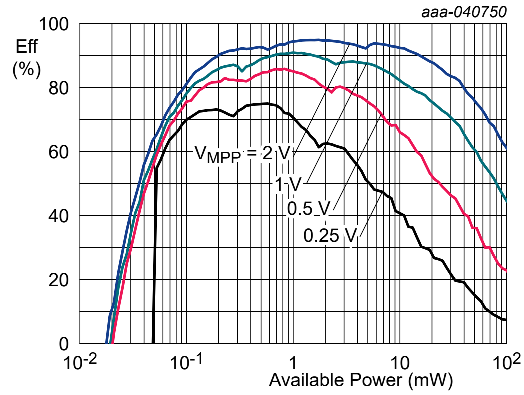

Fig. 6. Efficiency versus P_{av} over boosting factors

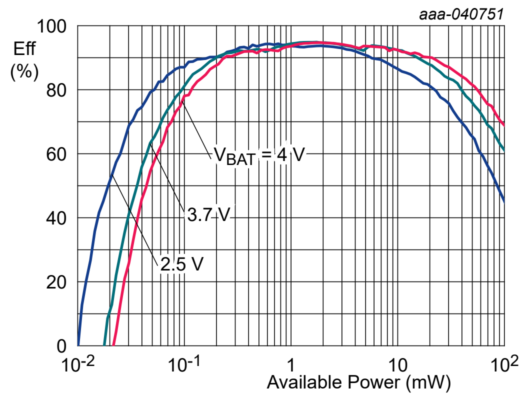

Fig. 7. Efficiency vs. P_{av} over V_{BAT}, VIN = V_{MPP}

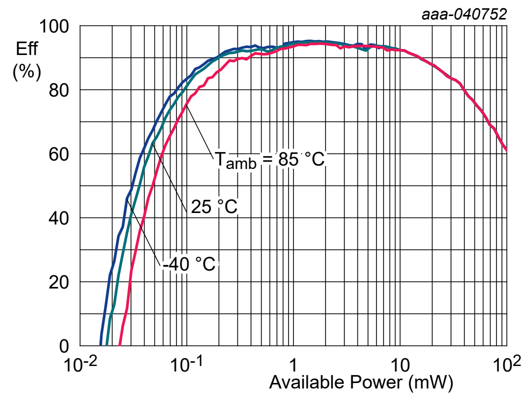

Fig. 8. Efficiency vs. P_{av} over temperature, V_{MPP} = 2 V

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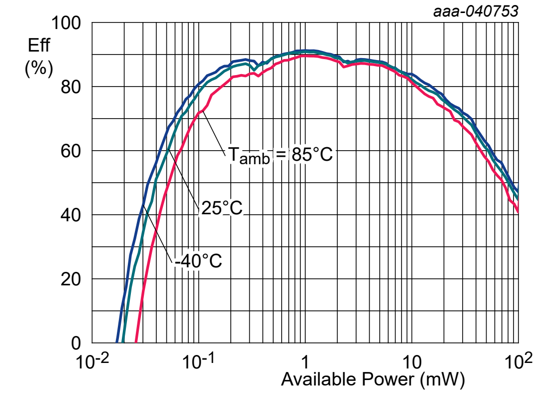

Fig. 9. Efficiency vs. P_{av} over temperature, V_{MPP} = 1 V

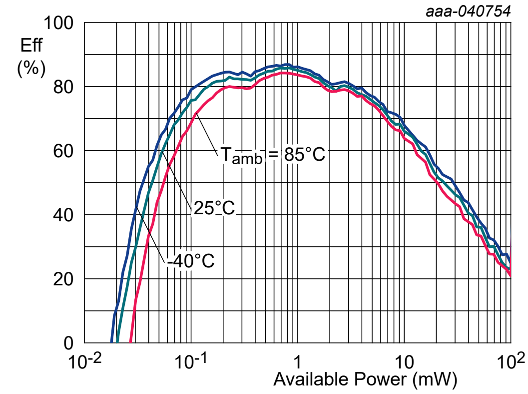

Fig. 10. Efficiency vs. P_{av} over temperature, V_{MPP} = 0.5 V

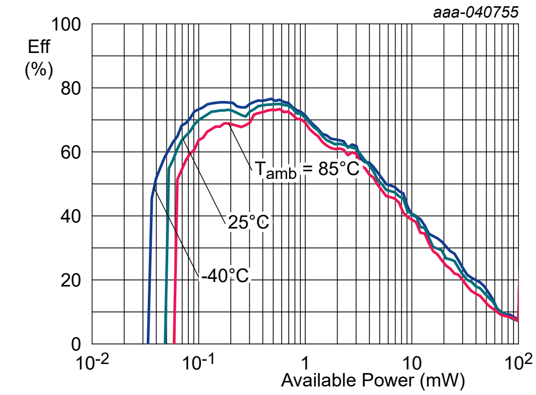

Fig. 11. Efficiency vs. P_{av} over temperature, V_{MPP} = 0.25 V

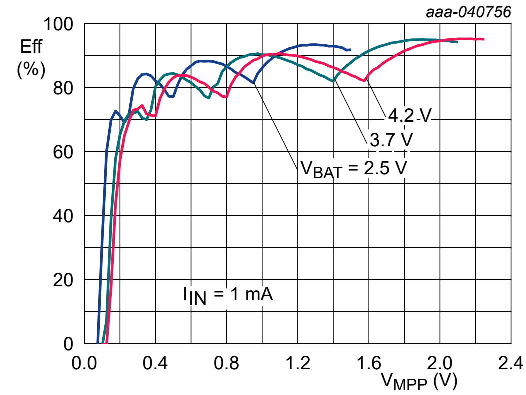

Fig. 12. Efficiency vs. V_{MPP} over V_{BAT}

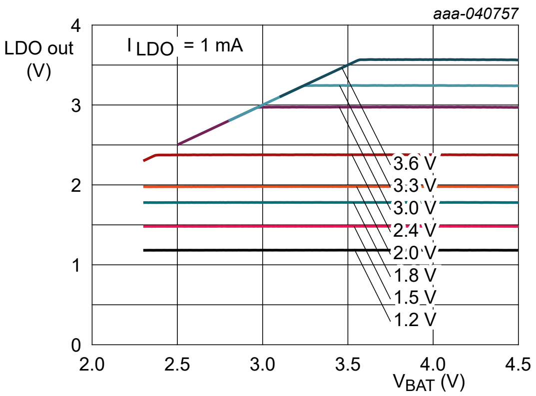

Fig. 13. V_{LDO} vs. V_{BAT} over LDO set voltages

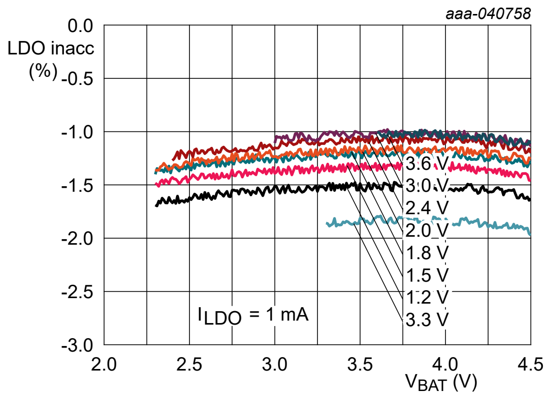

Fig. 14. LDO inaccuracy vs. V_{BAT} over LDO set voltages

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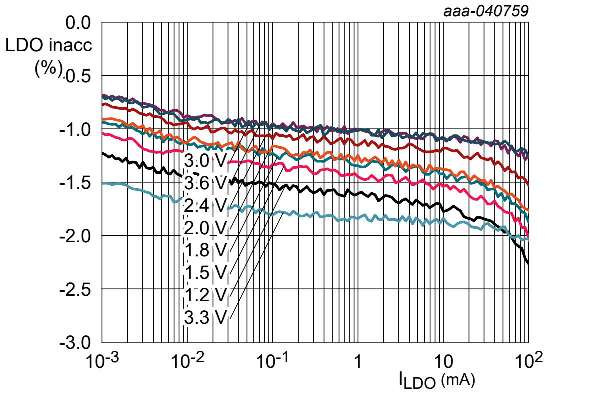


Fig. 15. LDO inaccuracy vs. I_{LDO} over LDO set voltages

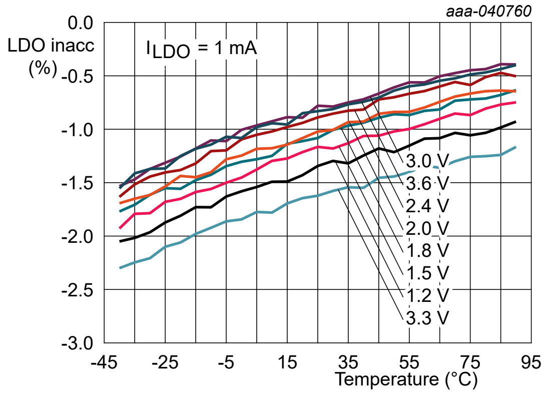
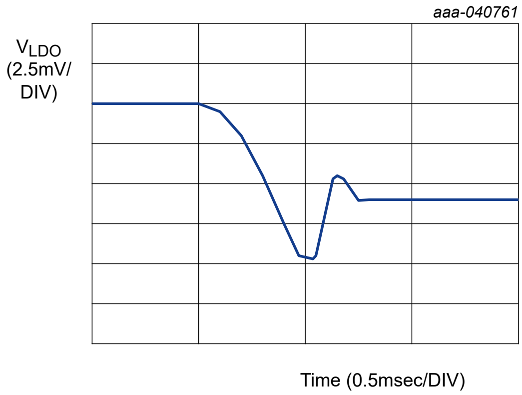
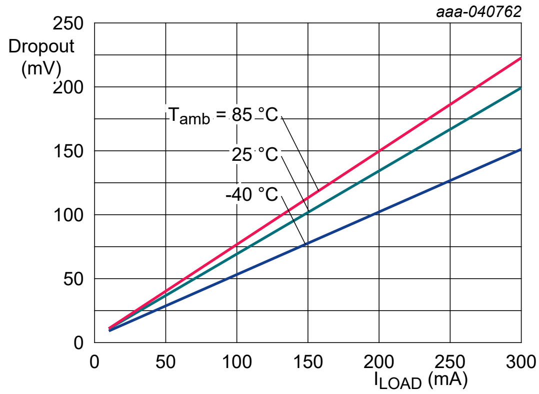


Fig. 16. LDO inaccuracy vs. temperature over LDO set voltages



LDO set voltage = 1.8 V
Load step from no load to 1 mA

Fig. 17. LDO load transient vs. time



LDO set voltage = 3.6 V

Fig. 18. LDO dropout voltage vs. I_{LDO} over temperature

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7. Detailed description

7.1. Overview

NEH7100 is an energy harvesting PMIC with a wide variety of auxiliary features as shown in the block diagram in Fig. 19.

The converter boosts the input voltage at VIN of the NEH7100 to a level suitable to charge the storage element connected to VBAT. The MPPT block searches for the best configuration of the power converter for the highest output power. The storage element is protected against over charging by OVP circuitry. Similarly, the LVD circuit indicates when the storage element voltage is too low. In case the storage element is empty, the NEH7100 can resume operation via coldstart. As an alternative to energy harvesting, the storage element can also be charged via USB. The integrated LDO connected to VBAT provides a stable, regulated output voltage for the application. The NEH7100 can be configured via hard-code pins and I^2C.

7.2. Block diagram

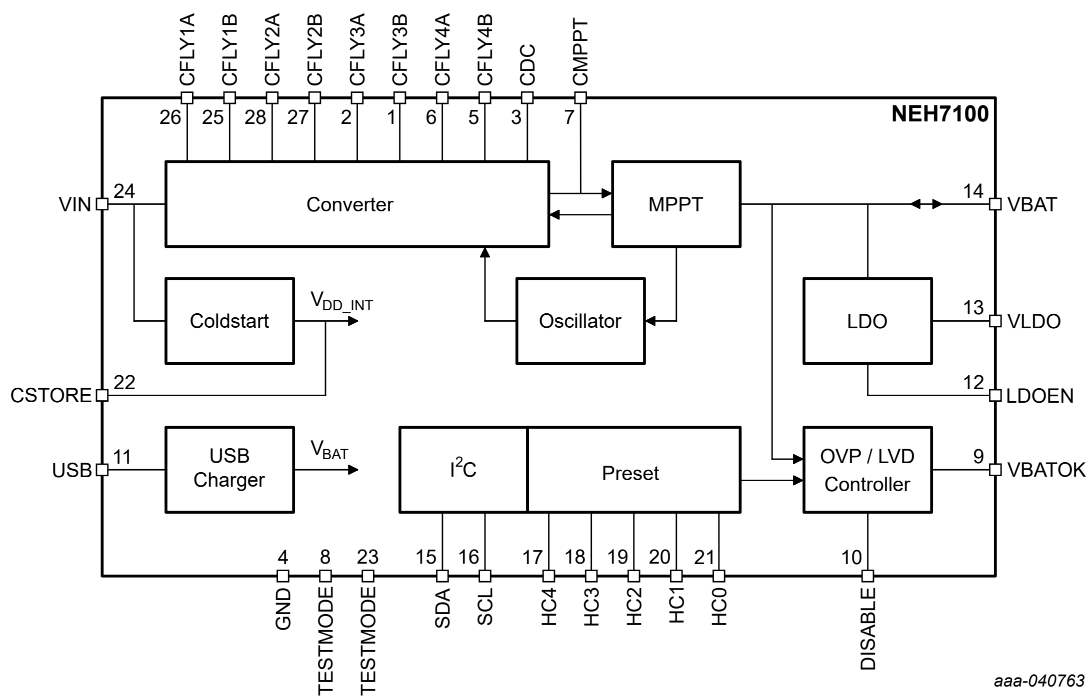

Fig. 19. NEH7100 functional diagram

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7.3. Feature descriptions

7.3.1. Converter / MPPT

The main converter of the NEH7100 boosts the input voltage, V_{IN}, to the storage element voltage, V_{BAT}. In normal operation, V_{STORE} is internally connected to V_{BAT}. Boosting factor and switching frequency of the converter are dynamically chosen by the MPPT hill-climbing algorithm for the best efficiency. Regularly, the MPPT engine checks whether a better configuration is available. The MPPT procedure is performed once every MPPT interval. The default MPPT interval is 1 second. The MPPT interval can be changed via register 0x05 defining the range from 0.5 to 64 s, see Table 8.

Table 8. MPPT interval, register *0x05* <2:0>

Bit <2>	Bit <1>	Bit <0>	MPPT interval (s)
0	0	0	0.5
0	0	1	1
0	1	0	2
0	1	1	4
1	0	0	8
1	0	1	16
1	1	0	32
1	1	1	64

The MPPT search range for selecting the optimal boosting factor and switching frequency can be reduced. Both the lower and upper search boundaries can be set via I²C. Tightening the search boundaries can help in shortening MPPT search time and therewith (slightly) reducing current consumption. By default the full range is used by the MPPT engine.

The boosting factor (BF) boundaries can be configured via register 0x04.

Table 9. $BF_{(min)}$, register *0x04* <1:0>

Bit <1>	Bit <0>	Lower boundary boosting factor range
0	0	2x
0	1	4x
1	0	8x
1	1	16x

Table 10. $BF_{(max)}$, register *0x04* <5:4>

Bit <5>	Bit <4>	Upper boundary boosting factor range
0	0	2x
0	1	4x
1	0	8x
1	1	16x

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Similar to limiting boosting factor range, frequency range can also be limited. This is done via register 0x03.

Table 11. Frequency$_{(min)}$, register *0x03* <2:0>

Bit <2>	Bit <1>	Bit <0>	Lower boundary frequency range
0	0	0	32 kHz
0	0	1	64 kHz
0	1	0	128 kHz
0	1	1	256 kHz
1	0	0	512 kHz
1	0	1	1.024 MHz
1	1	0	32 kHz
1	1	1	32 kHz

Table 12. Frequency$_{(max)}$, register *0x03* <6:4>

Bit <6>	Bit <5>	Bit <4>	Upper boundary frequency range
0	0	0	32 kHz
0	0	1	64 kHz
0	1	0	128 kHz
0	1	1	256 kHz
1	0	0	512 kHz
1	0	1	1.024 MHz
1	1	0	1.024 MHz
1	1	1	1.024 MHz

7.3.2. Coldstart

Normally, the NEH7100 operates from the storage element, connected to VBAT. In case the storage element is depleted, the NEH7100 can resume operation via its coldstart feature. The device will collect energy from the harvester to power itself (via C_{STORE}) and subsequently charge the storage element (via V_{BAT}). The coldstart feature of the NEH7100 implements a controlled process, see Fig. 20. It needs a minimum input voltage of 270 mV and a minimum available input power of 12 μW to get the device running.

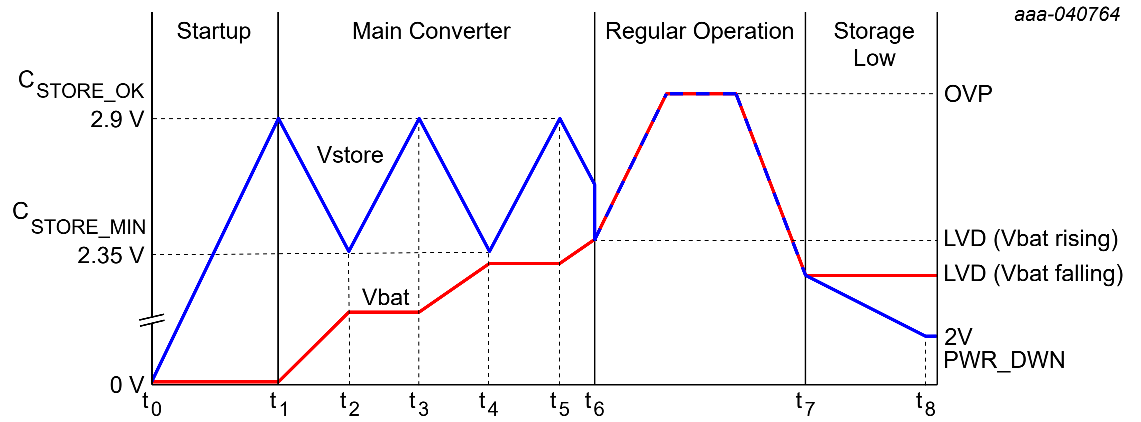

Fig. 20. Coldstart sequence

At the beginning of the coldstart operation, the coldstart power converter charges C_{STORE} using energy available from V_{IN}. Once the voltage across C_{STORE} reaches 2.9 V (C_{STORE_OK}) at t_1, the device starts up. At this moment, the coldstart power converter is disabled and the main power converter is enabled. The main power converter starts charging the storage element at V_{BAT}, C_{STORE} is not being charged anymore. Since the main power converter consumes current from C_{STORE}, V_{STORE} starts to go down. At t_2, when it reaches 2.35 V (C_{STORE_MIN}) the main power converter switches to charging C_{STORE}. This behavior continues to be repeated until V_{BAT} reaches the LVD(Rising) threshold at t_6, on which V_{BAT} and C_{STORE} are shorted together.

The main power converter continues to charge V_{BAT} until the OVP threshold is reached. If there is no available energy at V_{IN}, the storage element at V_{BAT} and C_{STORE} will be discharged due to the current consumption of the chip and the application. Once V_{BAT} reaches the LVD(Falling) threshold while discharging, V_{BAT} and C_{STORE} are disconnected from each other. The device is still turned on and checking if there is any available power on V_{IN}. In case power is available at V_{IN} the process as indicated between t_1 and t_6 applies. In case no energy is available at V_{IN}, V_{STORE} keeps on lowering. Finally, if V_{STORE} falls below 2 V (PWR_DWN), the device is turned off. As soon as minimum power and voltage are present at V_{IN}, the device will automatically start the sequence at t_0.

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7.3.3. USB charging

In addition to obtaining energy via the harvester, the storage element can also be charged via the USB pin. The charger can be configured for a certain current limit, see Table 13. USB charging is automatically enabled when a voltage higher than 4 V is detected on the USB pin. The USB Charger uses CC charging until the OVP limit is reached where the charger changes to CV charging. The nominal USB charging current is equal to 80% of the maximum charging current setting. This is done to ensure that the maximum charging current, due to process and temperature variation, does not exceed the values shown in Table 13.

Table 13. USB charging current, register *0x01* <2:0>

Bit <2>	Bit <1>	Bit <0>	USB maximum charging current (mA)
0	0	0	0.5
0	0	1	1
0	1	0	2
0	1	1	10
1	0	0	50
1	0	1	100
1	1	0	150
1	1	1	200

NEH7100 USB charging current is defaulted during start up to assume the HC pin configuration. The charging current level is applied according to Table 19.

7.3.4. Application LDO

To provide the required voltage to the application, an LDO is integrated. The LDO can be enabled and disabled using the LDOEN pin. The LDO output voltage can be set via register 0x01 over the range of 1.2 V to 3.6 V, see Table 14 as well as Section 7.3.7.

The LDO is supplied from VBAT and can deliver 200 mA with a dropout voltage below 300 mV. Optimal closed-loop stability requires the LDO capacitor value to be 47 µF. The capacitor should be placed as close a possible to the VLDO pin.

Table 14. LDO output, register 0x01 <5:3>

Bit <5>	Bit <4>	Bit <3>	LDO output (V)
0	0	0	1.2
0	0	1	1.5
0	1	0	1.8
0	1	1	2.0
1	0	0	2.4
1	0	1	3.0
1	1	0	3.3
1	1	1	3.6

The LDO has a bypass mode to connect the VLDO pin to V_{BAT}. In this case V_{VLDO} will follow V_{BAT} instead of regulating to the set voltage. There is also a control option on how the LDO is disabled. It can be either automatically disabled when the internal BATOK flag drops to 0, which happens when V_{BAT} drops below the LVD threshold, or disabled only when the LDOEN pin voltage is set to 0 V. The bypass and LDO control can both be configured through register 0x01

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Table 15. LDO Bypass, register 0x01 <7>

Bit <7>	LDO Bypass
0	Normal mode: Operating as LDO
1	Bypass mode: LDO acts as a switch. V_{VLDO} will follow V_{BAT} when the LDO is enabled

Table 16. LDO Control, register 0x01 <6>

Bit <6>	LDO CTRL
0	The LDO is enabled by the LDOEN pin. The LDO is disabled either by the LDOEN pin or the internal VBATOK flag.
1	LDO is enabled and disabled by the LDOEN pin setting

7.3.5. Storage element over-voltage protection (OVP)

V_{BAT} of NEH7100 is actively limited to a programmable voltage level to protect the storage element against over-charging. The level should be chosen such that it is close to, but below the allowed maximum charge voltage as specified in the storage element data sheet. This over-voltage protection applies for both charging via energy harvesting and charging via USB port. The OVP level can be set via register 0x00, see Table 17 as well as Section 7.3.7.

Table 17. Over-voltage protection levels, register *0x00* <3:0>

Bit <3>	Bit <2>	Bit <1>	Bit <0>	Limit voltage (V)
0	0	0	0	2.7
0	0	0	1	2.9
0	0	1	0	3.1
0	0	1	1	3.3
0	1	0	0	3.4
0	1	0	1	3.5
0	1	1	0	3.6
0	1	1	1	3.7
1	0	0	0	3.8
1	0	0	1	3.9
1	0	1	0	4.0
1	0	1	1	4.1
1	1	0	0	4.2
1	1	0	1	4.3
1	1	1	0	4.4
1	1	1	1	4.5

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7.3.6. Low voltage detection (LVD)

NEH7100 measures the storage element voltage to detect a too low voltage. The LVD threshold voltage can be set via register 0x00, see Table 18 as well as Section 7.3.7. If the storage element voltage is below the LVD threshold voltage, VBATOK is low. The LVD rising threshold voltage is LVD falling threshold voltage plus 150 mV. When V_{BAT} rises above the LVD rising threshold, the VBATOK pin voltage rises to V_{BAT}.

Table 18. Low-voltage detection levels, (falling storage element voltage) register *0x00* <7:4>

Bit <7>	Bit <6>	Bit <5>	Bit <4>	LVD (V)
0	0	0	0	2.2
0	0	0	1	2.3
0	0	1	0	2.4
0	0	1	1	2.5
0	1	0	0	2.6
0	1	0	1	2.7
0	1	1	0	2.8
0	1	1	1	2.9
1	0	0	0	3.0
1	0	0	1	3.1
1	0	1	0	3.2
1	0	1	1	3.3
1	1	0	0	3.4
1	1	0	1	3.5
1	1	1	0	3.6
1	1	1	1	3.7

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7.3.7. Hard-code settings and I²C

The NEH7100 can be configured in two ways: by hard-code settings pins HC0 to HC4 or via I²C programming. The hard-code settings enable easy configuration of the few most important parameters, while the I²C provide a wide range of configurable parameters. The hard-code settings are interpreted at the moment of power-up,V_{STORE} reaching C_{STORE_OK} level of the device, and are not read again until the next power cycle. The HC input should be either connected to a logic "0" (GND) or "1" (V_{STORE}). It is required to use V_{STORE}, rather than VBAT, as a logic "1" or "HIGH" reference to guarantee correct HC settings during coldstart operation. The hard-code configuration options can be found in Table 19. An I²C controller can communicate to NEH7100 using SDA and SCL pins on address 0x3C. Communication to the NEH7100 via I²C is based upon a register map table, see Table 24.

Table 19. Hard-code settings

<table>
<tr><th>HC4</th><th>HC3</th><th>HC2</th><th>HC1</th><th>HC0</th><th>OVP (V)</th><th>LVD (V)</th><th>LDO (V)</th><th>OCP (mA)</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td rowspan="8">4.2</td><td>3.5</td><td>3.3</td><td rowspan="8">200</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>3.2</td><td>3.0</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>2.6</td><td>2.4</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td rowspan="5">2.2</td><td>2.0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1.8</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1.5</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1.2</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>By-pass</td></tr>
<tr><td colspan="9"></td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td rowspan="11">4.0</td><td rowspan="2">3.5</td><td rowspan="2">3.3</td><td>100</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>50</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td rowspan="9">3.3</td><td>3.0</td><td rowspan="4">100</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>2.4</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>2.0</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td rowspan="2">1.8</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>50</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1.5</td><td rowspan="2">100</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td rowspan="2">1.2</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>10</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>By-pass</td><td>100</td></tr>
<tr><td colspan="9"></td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td rowspan="8">3.5</td><td>2.6</td><td>2.4</td><td rowspan="2">150</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td rowspan="7">2.5</td><td>2.0</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td rowspan="2">1.8</td><td>200</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>150</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td rowspan="2">1.5</td><td>200</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td rowspan="3">150</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1.2</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>By-pass</td></tr>
<tr><td colspan="9"></td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td rowspan="5">3.1</td><td rowspan="5">2.2</td><td>2.0</td><td rowspan="5">2</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1.8</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1.5</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1.2</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>By-pass</td></tr>
</table>

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8. Application and implementation

8.1. Typical application

A typical PV-cell application is shown in Fig. 21. Table 20 lists the Bill of Materials.

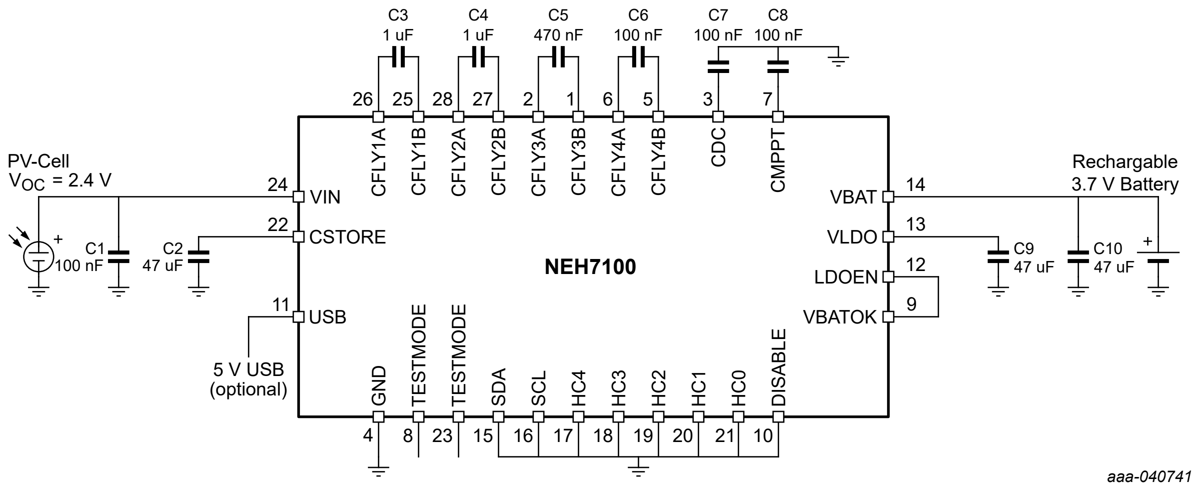

Fig. 21. Typical PV-Cell application

Table 20. Bill of Materials

Quantity	Reference designator	Value	Description	Manufacturer Part Number
1	U1	NEH7100	Energy Harvesting PMIC	NEH7100
4	C1, C6, C7, C8	0.1 µF ±10% 10 V	ceramic capacitor X5R 0402 (1005 Metric)	GRM155R61A104KA01J
3	C2, C9, C10	47 µF ±20% 6.3 V	ceramic Capacitor X5R 0603 (1608 Metric)	GRM188R60J476ME15D
2	C3, C4	1 µF ±20% 10 V	ceramic capacitor X5R 0402 (1005 Metric)	GRM153R61A105ME95D
1	C5	0.47 µF ±10% 10 V	ceramic capacitor X5R 0402 (1005 Metric)	GRM155R61A474KE15D
1	PV-Cell	-	PV-cell with V_{OC} = 2.4 V	-
1	rechargeable battery	-	3.7 V battery	-

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8.2. Optimizing application, reducing number of capacitors

The NEH7100 is capable of boosting the input voltage by 2, 4, 8 or 16 times to V_{BAT}. Depending on the used harvester and storage element, not all boosting factors might be needed. In this case one or more boosting factors can be bypassed. The associated capacitor(s) can be removed resulting in a reduced bill-of-material (BOM) and thus cost saving.

For best overall performance, the harvester's maximum-power-point voltage, V_{MPP}, should fit within the configured input voltage range. Fig. 22 depicts the overall efficiency versus the harvester's V_{MPP} given V_{BAT} = 3.7 V. In case a harvester is not likely to operate in a part of the input voltage range, the input range might be reduced by excluding boosting factors. The maximum-power-point voltage is a characteristic of a harvester and varies based on environmental conditions such as light intensity and temperature. The V_{MPP} of a harvester is not always explicitly mentioned in its datasheet. For PV-cells, a good indicator for V_{MPP} is the open-circuit voltage (V_{OC}) parameter. The relation between V_{OC} and V_{MPP}:

$$V_{MPP} = 0.7 \ldots 0.9 \cdot V_{OC}$$

The typical MPP ratio (V_{MPP}/V_{OC}) of a PV-cell is 0.8.

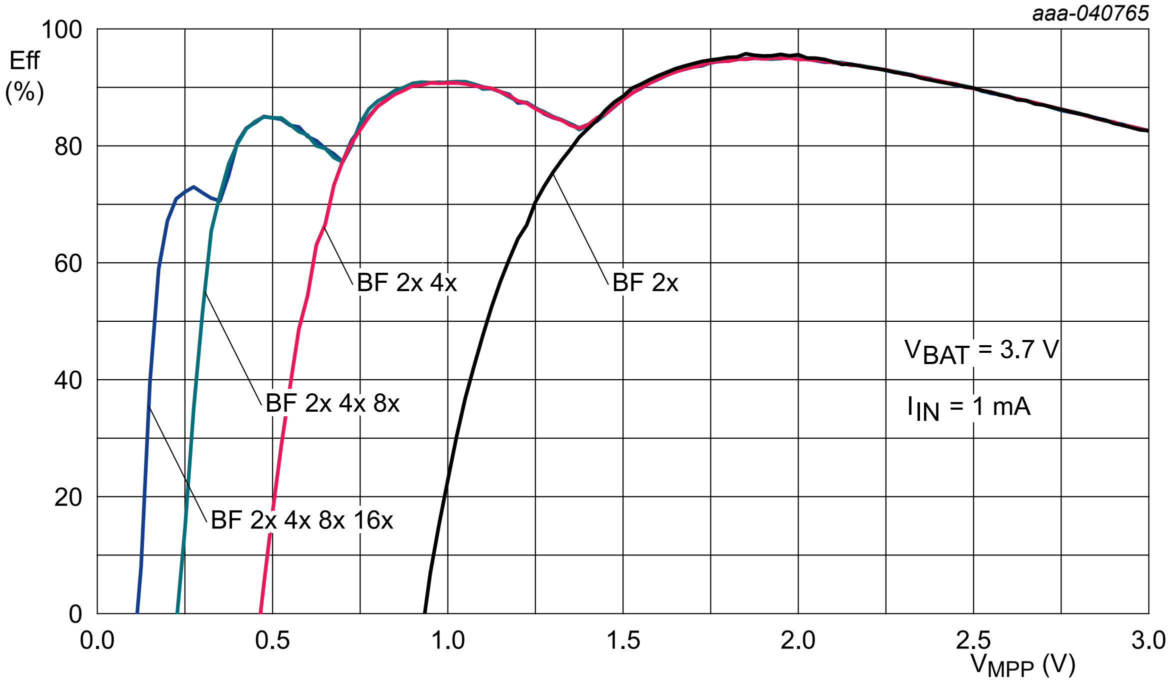

Fig. 22. Reduced Boosting factors

Table 21 provides the overview of V_{MPP} range for each boosting factor combination. The overall efficiency is not affected by reducing boosting factors if the harvester's V_{MPP} fits within the configured voltage range. The recommended V_{OC} range assumes a MPP ratio of 0.8

Table 21. V_{MPP} range for boosting factor combinations, V_{BAT} = 3.7 V

Available Boosting Factors	V_{MPP} (V)	V_{OC} (V)
2, 4, 8, 16	0.15 to 3	0.19 to 3.75
2, 4, 8	0.3 to 3	0.38 to 3.75
2, 4	0.63 to 3	0.78 to 3.75
2	1.25 to 3	1.56 to 3.75

Fig. 23 to Fig. 26 show the four related configurations with different number of boosting factors enabled.

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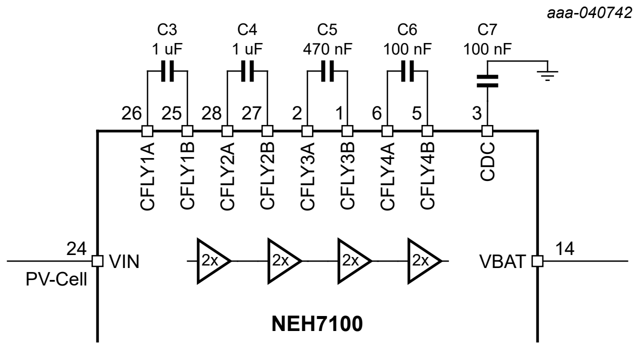

Fig. 23. Boosting factors: 2, 4, 8, 16

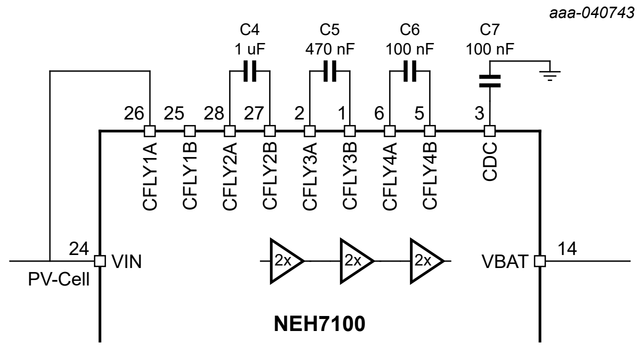

Fig. 24. Boosting factors: 2, 4, 8

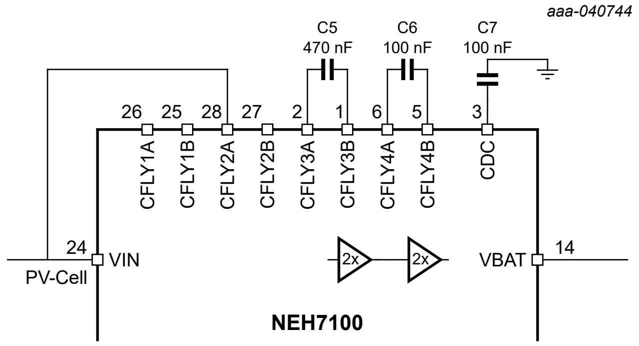

Fig. 25. Boosting factors: 2, 4

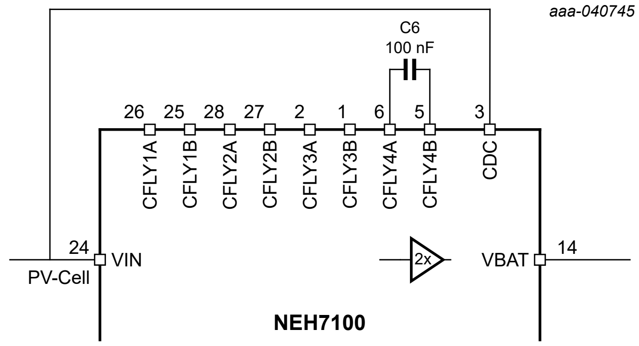

Fig. 26. Boosting factor: 2

Table 22 summarizes which capacitors can be omitted. For the reduced boosting factor configurations, a connection should be made between the input (VIN) and a particular flying-capacitor input pin.

Table 22. Configuration for reduced boosting factors

Available Boosting Factors	Capacitor(s) removed	Connection from VIN to
2, 4, 8, 16	-	-
2, 4, 8	C3	CFLY1A
2, 4	C3, C4	CFLY2A
2	C3, C4, C5, C7	CDC

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8.3. Harvesting efficiency

The overall efficiency (Eff) of the NEH7100 in combination with a harvester comprises two components (see Fig. 27):

1) $Eff_{converter}$ The efficiency of the power converter in the NEH7100
2) Eff_{match} The matching efficiency between the NEH7100 and the harvester

The total efficiency can be described as:

$$Eff = Eff_{converter} \cdot Eff_{match}$$

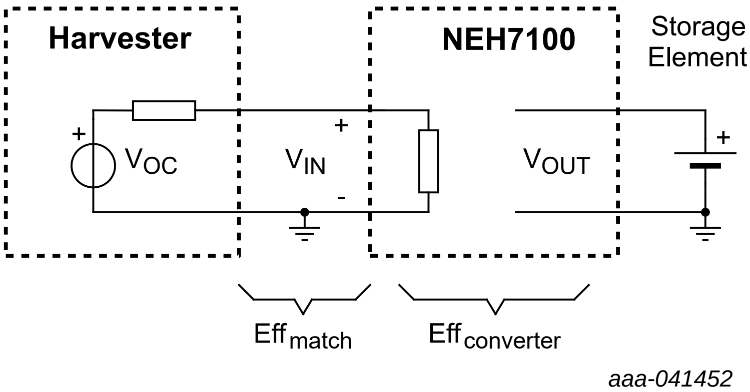

Fig. 27. Matching and converter efficiency

8.3.1. Power converter efficiency

In practice, a power converter has losses from input power (P_{IN}) to output power (P_{OUT}). The ratio of the output power and input power is typically referred to as the power-converter efficiency:

$$Eff_{converter} = \frac{P_{OUT}}{P_{IN}} \cdot 100 \ \%$$

For common inductive and capacitive power converters this efficiency is in the range of 80 % to 95 %. Several characteristics can have an impact on this efficiency, such as: ratio of the output voltage and input voltage, quality and size of the converter capacitors. In its targeted power range the converter efficiency of the NEH7100 is about 94 %.

8.3.2. Matching efficiency

In general, power transfer between components is optimized by matching the receiving input impedance with the transmitting output impedance. In a harvesting system it is also important to transfer power from harvester to the power converter in the most efficient manner to minimize loss of harvested energy. How optimal the power transfer between harvester and power converter is, can be expressed by matching efficiency.

The matching efficiency is defined as:

$$Eff_{match} = \frac{P_{IN}}{P_{available}} \cdot 100 \ \%$$

Where P_{IN} is the actual power at the input of the power converter and $P_{available}$ is the maximum power that can be achieved at the input (which is at 100% matching).

From the graphs in Section 6.6, (Fig. 6 to Fig. 12), it can be seen that the matching efficiency as part of the overall efficiency has a dependency on the ratio of V_{MPP} and V_{BAT}. The V_{BAT} relation can be understood from the perspective that the capacitive power converter has a given boost factor between input and output:

$$V_{IN} = \frac{V_{BAT}}{\text{boosting factor}}$$

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Where the boosting factor of the NEH7100 can be 2, 4, 8 or 16. The maximum power-point voltage (V_{MPP}) is the voltage on the power converter's input where most power is delivered by the harvester.

Thus, for optimal matching efficiency a harvester should be chosen with a V_{MPP} close to V_{BAT} / boosting factor. Since the efficiency of the PMIC is highest at the lowest boosting factor, this is the preferred boosting factor. In case the optimum PV cell is not available, the impact on the overall efficiency is limited, i.e. up to about 10 %, see Fig. 12. This limited efficiency impact is as a result of the MPPT algorithm that can change more configuration parameters of the power converter than only the boosting factor.

8.4. Charge current measurement

For determining the best possible power converter configuration, the NEH7100 has an integrated current measurement. The measurement engine can be used to estimate the charging current to the storage element.

The current is measured across a sense resistor. There are four possible sense resistors. Each sense resistor is dedicated for a certain current range. Depending on the current, a sense resistor is dynamically chosen. Which current range is applied for the measurement can be read from the I_RANGE register 0x09. After every MPPT optimization cycle, a new value is written in I_MEASURE register 0x0A. The register value needs to be converted into a charge current.

Table 23. Calculating charge current

I_RANGE 0x09<1:0>	I_{BAT} (A)
00	70.6 nA * I_MEASURE (0x0A)
01	478 nA * I_MEASURE (0x0A)
10	4.71 µA * I_MEASURE (0x0A)
11	67.5 µA * I_MEASURE (0x0A)

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9. Register map

Table 24. Register map

Address (HEX)	Bits	Field name	Description (Bold face values are reset values)	READ WRITE	Power ON value (HEX)
0x00	7:4	LVD	falling low-voltage detection level (V)	R/W	set by hard-code pins
			0000: 2.2		
			0001: 2.3		
			0010: 2.4		
			0011: 2.5		
			0100: 2.6		
			0101: 2.7		
			0110: 2.8		
			0111: 2.9		
			1000: 3.0		
			1001: 3.1		
			1010: 3.2		
			1011: 3.3		
			1100: 3.4		
			1101: 3.5		
			1110: 3.6		
			1111: 3.7		
	3:0	OVP	over-voltage protection level (V)		
			0000: 2.7		
			0001: 2.9		
			0010: 3.1		
			0011: 3.3		
			0100: 3.4		
			0101: 3.5		
			0110: 3.6		
			0111: 3.7		
			1000: 3.8		
			1001: 3.9		
			1010: 4.0		
			1011: 4.1		
			1100: 4.2		
			1101: 4.3		
			1110: 4.4		
			1111: 4.5		

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Address (HEX)	Bits	Field name	Description (Bold face values are reset values)	READ WRITE	Power ON value (HEX)
0x01	7	LDO_BP	mode control of the LDO when LDOEN is high.	R/W	set by hard-code pins
			0: Normal mode: Operating as LDO		
			1: Bypass mode: LDO acts as a switch. V_{LDO} will follow V_{BAT}		
	6	LDO_CTRL	Sets how LDO responds on VBATOK = 0		
			0: LDO automatically disables on VBATOK = 0, even if LDOEN is high		
			1: LDO acts based on LDOEN setting		
	5:3	VLDO	LDO output voltage (V)		
			000: 1.2		
			001: 1.5		
			010: 1.8		
			011: 2.0		
			100: 2.4		
			101: 3.0		
			110: 3.3		
			111: 3.6		
	2:0	I_{USB_max}	maximum storage element charging current (mA) via USB		
			000: 0.5		
			001: 1		
			010: 2		
			011: 10		
			100: 50		
			101: 100		
			110: 150		
			111: 200		
0x02	7:0	Reserved	reserved	R/W	-

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Address (HEX)	Bits	Field name	Description (Bold face values are reset values)	READ WRITE	Power ON value (HEX)
0x03	7	Reserved	reserved	R/W	70
	6:4	$f_{(max)}$	PC upper boundary frequency range		
			000: 32 kHz		
			001: 64 Hz		
			010: 128 kHz		
			011: 256 kHz		
			100: 512 kHz		
			101: 1.024 MHz		
			110 and **111: 1.024 MHz**		
	3	Reserved	reserved		
	2:0	$f_{(min)}$	PC lower boundary frequency range		
			000: 32 kHz		
			001: 64 kHz		
			010: 128 kHz		
			011: 256 kHz		
			100: 512 kHz		
			101: 1.024 MHz		
			110 and 111: 32 kHz		
0x04	7:6	Reserved	reserved	R/W	30
	5.4	BF_{MAX}	upper boundary boosting factor range		
			00: 2x		
			01: 4x		
			10: 8x		
			11: 16x		
	3:2	Reserved	reserved		
	1:0	BF_{MIN}	lower boundary boosting factor range		
			00: 2x		
			01: 4x		
			10: 8x		
			11: 16x		
0x05	7:3	Reserved	reserved	R/W	01
	2:0	MPPT interval	MPPT interval		
			000: 0.5 s		
			001: 1 s		
			010: 2 s		
			011: 4 s		
			100: 8 s		
			101: 16 s		
			110: 32s		
			111: 64 s		
0x06	7:0	Reserved	reserved	R/W	-
0x07	7:0	Chip_ID	product ID and version	R	-
			Chip_ID = ‘0x15’		

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Address (HEX)	Bits	Field name	Description (Bold face values are reset values)	READ WRITE	Power ON value (HEX)
0x08	7:5	Reserved	reserved	R	-
	4	OVP_OUT	OVP flag (active high)		
			0: V_{BAT} is below OVP threshold		
			1: V_{BAT} is above OVP threshold		
	3	LVD_OUT	LVD flag (active high)		
			0: V_{BAT} is above LVD threshold		
			1: V_{BAT} is below LVD threshold		
	2	SDF	shutdown flag (active high)		
			0: Harvesting mode, sufficient harvesting		
			1: Device will be in low-power consumption mode, (too) low battery harvesting current measured. When current increases, harvesting will resume.		
	1	OCF	overcurrent flag (active high)		
			0: I_{BAT} is below OCP level as specified in Table 19		
			1: I_{BAT} is above OCP level as specified in Table 19		
	0	Chip_OK	Chip OK Flag – (active high)		
			0: cold start not done		
			1: cold start done, main converter on and internal blocks started		
0x09	7:2	Reserved	reserved	R	-
	1:0	I_RANGE	MPPT engine latest selected current range		
0x0A	7:0	I_MEASURED	MPPT engine latest current measurement. The formula for I_{BAT} current depends on the used I_RANGE (register 0x09<1:0>) for the measurement.	R	-
			I_{BAT} = I_MEASURED * 70.6 nA (I_RANGE 00)		
			I_{BAT} = I_MEASURED * 478 nA (I_RANGE 01)		
			I_{BAT} = I_MEASURED * 4.71 μA (I_RANGE 10)		
			I_{BAT} = I_MEASURED * 67.5 μA (I_RANGE 11)		

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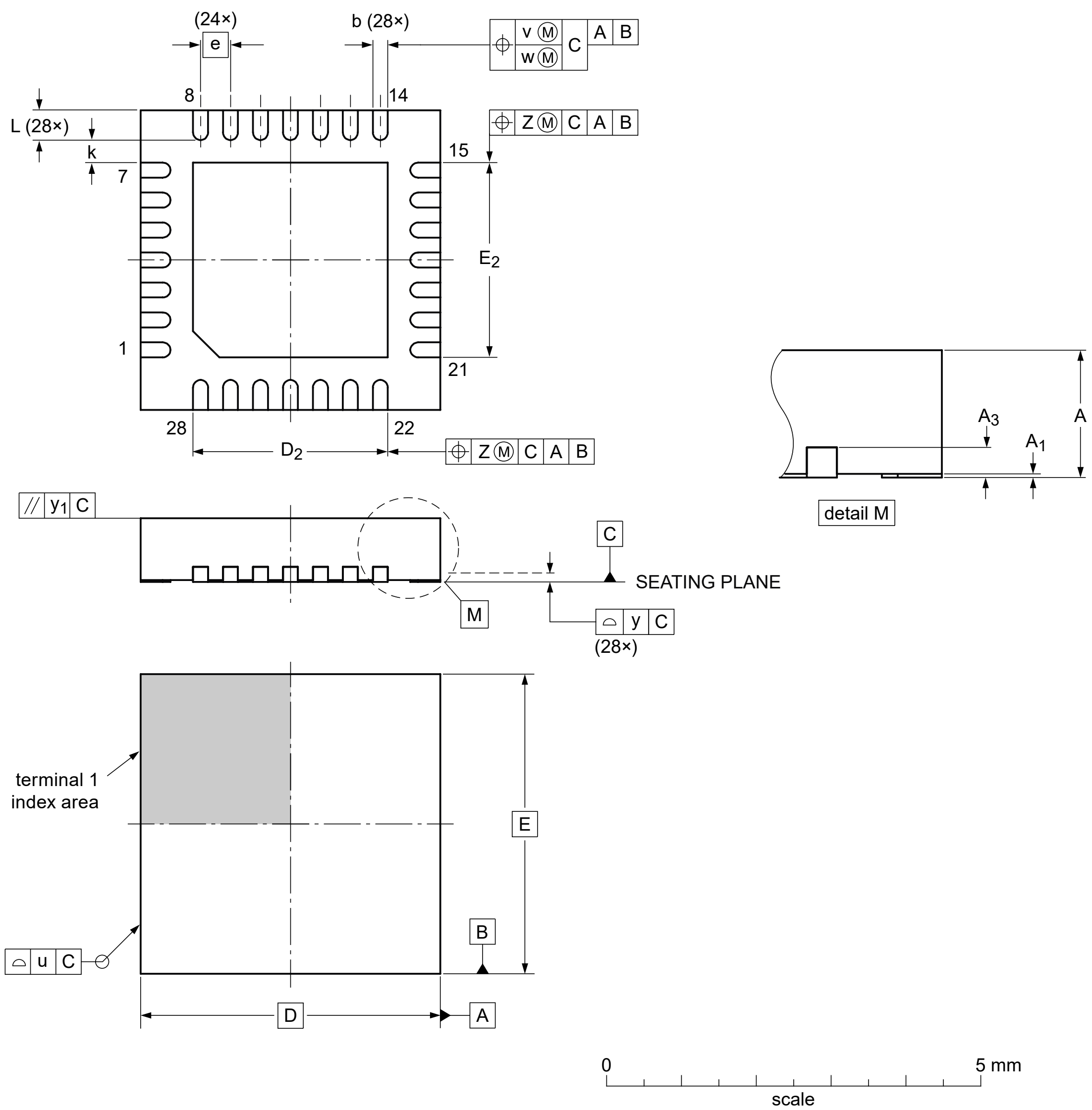
10. Package outline

HVQFN28: plastic, leadless thermal enhanced very thin quad flat package; 28 terminals; 0.4 mm pitch; 4 mm x 4 mm x 0.85 mm body **SOT8080-1**



Dimensions (mm are the original dimensions)

Unit[1]		A	A_1	A_3	b	D	D_2	E	E_2	e	k	L	u	v	w	y	y_1	z
mm	max	0.90	0.05	0.2 REF	0.25	4.0 BSC	2.7	4.0 BSC	2.7	0.4 BSC	0.3 REF	0.5	0.1	0.07	0.05	0.08	0.1	0.1
	nom	0.85	0.02		0.20		2.6		2.6			0.4						
	min	0.80	0		0.17		2.5		2.5			0.3						

sot8080-1_po

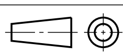
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8080-1		MO-220				23-09-12

Fig. 28. Package outline SOT8080-1 (HVQFN28)

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11. Revision history

Table 25. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NEH7100 v.1	20241217	Product data sheet	-	-

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12. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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