MPM54313

16V, Triple 3A Power Module with I²C Interface

DESCRIPTION

The MPM54313 is a triple 3A, fully integrated power module with an I²C interface. The MPM54313 offers a complete power solution with built-in power-on/-off sequencing control, configurable soft start, compensation, and various protection thresholds.

Constant-on-time (COT) control provides ultra-fast transient response. The output voltage (V_{OUT}) can be adjusted via the I²C bus or preset by the multiple-time programmable (MTP) memory. The power on/off sequence is also configurable via the MTP, or it can be controlled via the I²C bus online.

The device offers configurable active voltage positioning (AVP), which generates a droop voltage that allows up to three outputs to be paralleled with passive current balancing. In addition, buck A and buck B can operate in parallel for up to 6A in interleaving mode, which allows for active current balancing.

Full protection features include under-voltage lockout (UVLO), over-current protection (OCP), over-voltage protection (OVP), under-voltage protection (UVP), and thermal shutdown.

The MPM54313 requires a minimal number external components, and it is available in a compact BGA (8mmx9mmx2.58mm) package.

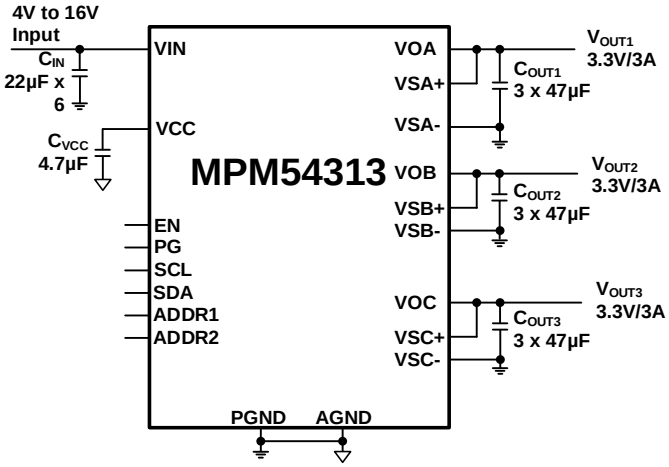
FEATURES

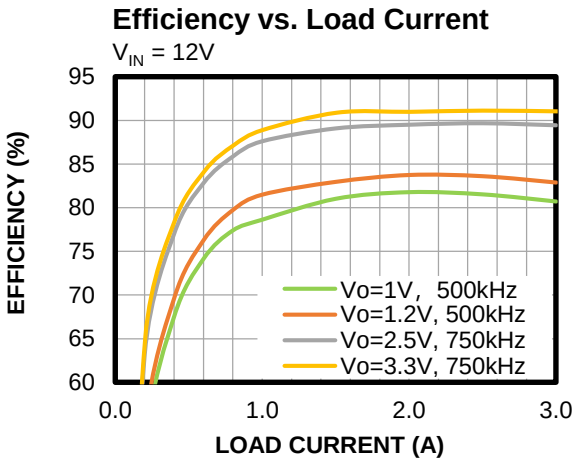
- Wide 4V to 16V Input Voltage (V_{IN}) Range
- Adaptive Constant-On-Time (COT) Control for Ultra-Fast Transient Response
- Parallel Operation with Passive or Active Current Balancing
- I²C-Configurable Output Voltage (V_{OUT})
- Configurable 500kHz to 1000kHz Switching Frequency (f_{SW})
- Differential V_{OUT} Remote Sense
- Accurate V_{OUT}, Output Current (I_{OUT}), and Junction Temperature (T_J) Monitoring via I²C
- Open-Drain Power Good (PG) Indication
- Configurable I²C Slave Address
- Selectable Pulse-Frequency Modulation (PFM) / Pulse-Width Modulation (PWM) Mode, Adjustable Frequency via I²C
- Pre-Biased Start-Up
- Over-Current Protection (OCP), Under-Voltage Protection (UVP), Under-Voltage Lockout (UVLO), Thermal Shutdown, and Over-Voltage Protection (OVP)
- Available in a BGA (8mmx9mmx2.58mm) Package

APPLICATIONS

- FPGA and ASIC Power Supplies
- Networking and Telecommunication
- Optical Module Power Supplies

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPM54313GBJ-xxxx	BGA (8mmx9mmx2.58mm)	*See Below*	3
MPM54313GBJ-0000			

* For Tray, add suffix -T (e.g. MPM54313GBJ-xxxx-T).

* For Tape & Reel, add suffix -Z (e.g. MPM54313GBJ-xxxx-Z).

* "xxxx" is the configuration code identifier for the register setting stored in the MTP. The default number is "0000". Each "x" can be a hexadecimal value between 0 and F. Work with an MPS FAE to create this unique number, even if ordering the "0000" code. The MPM54313GBJ-0000 is the default configuration.

TOP MARKING

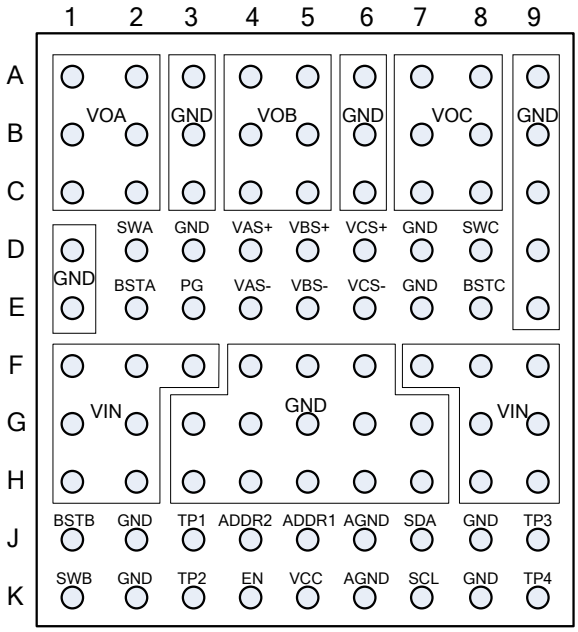
MPSYYWW
MP54313
LLLLLLLLL
M

MPS: MPS prefix
YY: Year code
WW: Week code
MP54313: Part number
LLLLLLLLL: Lot number

M: Module

PACKAGE REFERENCE

TOP VIEW



BGA (8mmx9mmx2.58mm)

PIN FUNCTIONS

Pin #	Name	Description
A1, A2, B1, B2, C1, C2	VOA	**Buck A output.** Output of channel A.
A4, A5, B4, B5, C4, C5	VOB	**Buck B output.** Output of channel B.
A3, B3, C3, A6, B6, C6, A9, B9, C9, D9, E9, D7, E7, D1, E1, F4, F5, F6, G3, G4, G5, G6, G7, H3, H4, H5, H6, H7, J2, K2, J8, K8	GND	**Power ground.**
A7, A8, B7, B8, C7, C8	VOC	**Buck C output.** Output of channel C.
E4	VSA-	**Remote sense ground for buck A.** Kelvin connect VSA- to the output capacitor's ground node on buck A.
D4	VSA+	**Positive feedback for buck A.** Connect buck A's output directly to this pin, or make the connection through a feedback resistor divider. Connect VSA+ to VSB+ during dual-phase interleaving work mode.
E5	VSB-	**Remote sense ground for buck B.** Kelvin connect VSB- to the output capacitor's ground node on buck B.
D5	VSB+	**Positive feedback for buck B.** Connect buck B's output directly to this pin, or make the connection through a feedback resistor divider. Connect VSB+ to VSA+ during dual-phase interleaving work mode.
D6	VSC+	**Positive feedback for buck C.** Connect buck C's output directly to this pin, or make the connection through a feedback resistor divider.
E6	VSC-	**Remote sense ground for buck C.** Kelvin connect VSC- to the output capacitor's ground node on buck C.
E2	BSTA	**Buck A bootstrap.** Float this pin.
D2	SWA	**Buck A switching node.** Float this pin.
E3	PG	**Power good input/output, open-drain driver.** The MPM54313 asserts the PG pin to indicate valid and stable output voltages. When any enabled regulator falls below the under-voltage (UV) threshold, the MPM54313 de-asserts PG by driving the signal low.
K7	SCL	**I²C bus clock.**
J7	SDA	**I²C bus data.**
D8	SWC	**Buck C switching node.** Float this pin.
E8	BSTC	**Buck C bootstrap.** Float this pin.
F1, F2, F3, F7, F8, F9, G1, G2, G8, G9, H1, H2, H8, H9	VIN	**Supply voltage input.** Ceramic capacitors are required to decouple the input rail. Connect VIN using a wide PCB trace.
K1	SWB	**Buck B switching node.** Float this pin.
J3, K3, J9, K9	TP1, TP2, TP3, TP4	**Test pins.** Float these test pins.
J4	ADDR2	**Address for I²C bus.** Nine I²C addresses can be selected by pulling the ADDR1 and ADDR2 pins high, low, or leaving them floating.
J5	ADDR1	**Address for I²C bus.** Nine I²C addresses can be selected by pulling the ADDR1 and ADDR2 pins high, low, or leaving them floating.
K4	EN	**Enable signal of the power module.** Drive the EN pin high to enable the power module; drive it low to disable the power module.
J1	BSTB	**Buck B bootstrap.** Float this pin.

PIN FUNCTIONS *(continued)*

Pin #	Name	Description
K5	VCC	**Internal 3.3V LDO output.** The driver and control circuits are powered from the VCC voltage. Decouple VCC with a 1μF ceramic capacitor placed as close to VCC pin as possible.
J6, K6	AGND	**Analog ground.** it is recommended to connect AGND to the power ground pin.

PIN MAP

Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
A1	VOA	B1	VOA	C1	VOA	D1	GND	E1	GND
A2	VOA	B2	VOA	C2	VOA	D2	SWA	E2	BSTA
A3	GND	B3	GND	C3	GND	D3	GND	E3	PG
A4	VOB	B4	VOB	C4	VOB	D4	VAS+	E4	VAS-
A5	VOB	B5	VOB	C5	VOB	D5	VBS+	E5	VBS-
A6	GND	B6	GND	C6	GND	D6	VCS+	E6	VCS-
A7	VOC	B7	VOC	C7	VOC	D7	GND	E7	GND
A8	VOC	B8	VOC	C8	VOC	D8	SWC	E8	BSTC
A9	GND	B9	GND	C9	GND	D9	GND	E9	GND
Pin #	**Function**	**Pin #**	**Function**	**Pin #**	**Function**	**Pin #**	**Function**	**Pin #**	**Function**
F1	VIN	G1	VIN	H1	VIN	J1	BSTB	K1	SWB
F2	VIN	G2	VIN	H2	VIN	J2	GND	K2	GND
F3	VIN	G3	GND	H3	GND	J3	TP1	K3	TP2
F4	GND	G4	GND	H4	GND	J4	ADDR2	K4	EN
F5	GND	G5	GND	H5	GND	J5	ADDR1	K5	VCC
F6	GND	G6	GND	H6	GND	J6	AGND	K6	AGND
F7	VIN	G7	GND	H7	GND	J7	SDA	K7	SCL
F8	VIN	G8	VIN	H8	VIN	J8	GND	K8	GND
F9	VIN	G9	VIN	H9	VIN	J9	TP3	K9	TP4

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) 18V
V_{SWA} / V_{SWB} / V_{SWC} (DC) .....-0.3V to V_{IN} + 0.3V
V_{BSTA} / V_{BSTB} / V_{BSTC}..... V_{SW} + 4V
VOA / VOB / VOC..... 6V
V_{CC} 4.5V
V_{CC}, ADDR1, ADDR2, PG (1s) (2)……..…..…6V
All other pins .....-0.3V to +4.3V
Continuous power dissipation (T_A = 25°C) (6)
……7.67W
Junction temperature (T_J) .....150°C
Storage temperature..... -65°C to +170°C

ESD Ratings

Human body model (HBM) ..... ±2kV
Charged-device model (CDM) ..... ±2kV

Recommended Operating Conditions (3)

Input voltage (V_{IN}) .....4V to 16V
Output voltage (V_{OUT}).....0.4V to 5.5V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (4) (5) (6) (7) (8)

BGA (8mmx9mmx2.58mm)
θ_{JA}.....16.3°C/W
θ_{JC_TOP}.....0.2°C/W
θ_{JB}.....1.27°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) Voltage rating during MTP programming.
3) The device is not guaranteed to function outside of its operating conditions.
4) θ_{JA} is junction-to-ambient thermal resistance, θ_{JC_TOP} is junction-to-case top thermal characterization parameter, and θ_{JB} is junction-to-board thermal characterization parameter.
5) The thermal parameter is based on test on an MPS evaluation board (EVM54313-BJ-00A) under no airflow cooling conditions in a standard enclosure. The board size is 8.1cmx8.1cm, 4-layer, top/bottom copper thickness is 2oz, mid-layer 1/2 copper thickness is 1oz.
6) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature.
7) The junction-to-case top thermal characterization parameter, θ_{JC_TOP}, estimates the junction temperature in the real system, based on equation $T_J = \theta_{JC\_TOP} \times P_{LOSS} + T_{CASE\_TOP}$, where P_{LOSS} is the module's entire power loss in a real application, and T_{CASE_TOP} is the case top temperature.
8) The junction-to-board thermal characterization parameter, θ_{JB}, is an estimation of the junction temperature in the real system, based on equation $T_J = \theta_{JB} \times P_{LOSS} + T_{BOARD}$, where P_{LOSS} is the module's entire power loss in a real application, and T_{BOARD} is the board temperature.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C (9), typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (no switching)	I_{IN}	No switching, FB high, PFM, no I²C communication		6.34		mA
Default switching frequency	f_{SW}	Reg 0Fh = 0xAA		1000		kHz
Input Voltage (V_{IN})						
V_{IN} over-voltage (OV) rising threshold	$V_{IN\_OV\_R}$	90h, bit[0] = 1'b1		15		V
V_{IN} OV hysteresis	$V_{IN\_OV\_HYS}$			0.25		V
V_{IN} under-voltage lockout (UVLO) rising threshold	$V_{IN\_UVLO\_R}$	90h, bit[1] = 1'b1, AFh, bits[1:0] = 2'b00	2.85	3.05	3.25	V
V_{IN} UVLO hysteresis	$V_{IN\_UVLO\_HYS}$			0.25		V
EN						
EN logic high voltage	V_{EN_H}		1.2			V
EN logic low voltage	V_{EN_L}				0.35	V
EN internal pull-down resistance	R_{EN_DOWN}			2.7		MΩ
ADDR						
ADDR1/2 logic high voltage	V_{ADDR_H}		1.2			V
ADDR1/2 logic low voltage	V_{ADDR_L}				0.35	V
Buck Regulators						
Buck A feedback voltage accuracy	VAS+	Reg 25h, bit[3] = 1'b1, Reg 15h = 0x90	3.31	3.36	3.41	V
Buck B feedback voltage accuracy	VBS+	Reg 25h, bit[2] = 1'b1, Reg 16h = 0x90	3.31	3.36	3.41	V
Buck C feedback voltage accuracy	VCS+	Reg 25h, bit[1] = 1'b1, Reg 17h = 0x90	3.31	3.36	3.41	V
V_{OUT} under-voltage (UV) rising threshold				85%		V_{OUT}
V_{OUT} UV falling threshold				80%		V_{OUT}
Low-side current limit (source)	$I_{LS\_VALLEY1}$			3.6		A
Minimum on time (10)	t_{ON_MIN1}			30		ns
Minimum off time (10)	t_{OFF_MIN1}			120		ns
Output over-voltage protection (OVP) rising threshold	V_{OVP1_H}			112%		V_{REF}
Output OVP recovery threshold	V_{OVP1_L}			109%		V_{REF}
Soft-start time for VOA	t_{SS_B1}	Reg 12h, bits[7:6] = 2b'10, V_{OUT} = 10% to 90%		2		ms
Soft-start time for VOB	t_{SS_B2}	Reg 12h, bits[5:4] = 2b'10, V_{OUT} = 10% to 90%		2		ms
Soft-start time for VOC	t_{SS_B3}	Reg 12h, bits[3:2] = 2b'10, V_{OUT} = 10% to 90%		2		ms
Discharge resistance	R_{DIS}	Reg 0Eh, bit[3:1] = 3b'000/111	-40%	10/2	+40%	Ω

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C (9), typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Analog-to-Digital Converter (ADC)						
Output voltage readback accuracy		V_{OUT} = 3.3V	217	220	223	LSB
Output current readback accuracy		I_{OUT} = 3A		24		LSB
Power Good (PG)						
PG UV rising	$V_{PG\_UV\_R}$	Reg 0Dh, bit[3:1] = 3b'000		98%		V_{REF}
PG UV falling	$V_{PG\_UV\_F}$			95%		V_{REF}
PG OV rising	$V_{PG\_OV\_R}$			105%		V_{REF}
PG OV falling	$V_{PG\_OV\_F}$			102%		V_{REF}
Power good, output port sink current capability	V_{PG_SINK}	Sink 1mA			0.4	V
VCC Regulator						
VCC UVLO rising threshold	V_{CC_R}		2.5	2.7	2.9	V
VCC UVLO hysteresis	V_{CC_HYS}			300		mV
VCC voltage	V_{CC}	I_{CC} = 25mA		3.3		V
VCC voltage regulation	V_{CC_RG}	I_{CC} = 0mA to 25mA		1		%
Temperature Protection						
Thermal shutdown (10)	T_{OTP_R}			145		°C
Thermal hysteresis (10)	T_{HYS}			20		°C

I²C PORT SIGNAL CHARACTERISTICS (11)

V_{IN} = 12V, T_J = -40°C to +125°C (9), typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	C_B = 100pF		C_B = 400pF		Units
			Min	Max	Min	Max	
SCL clock frequency	f_{SCHL}		0	3.4	0	0.4	MHz
Set-up time for a repeated start command	t_{SU_STA}		160		600		ns
Hold time (repeated) start command	t_{HD_STA}		160		600		ns
Low period of the SCL clock	t_{LOW}		160		1300		ns
High period of the SCL clock	t_{HIGH}		60		600		ns
Data set-up time	t_{SU_DAT}		10		100		ns
Data hold time	t_{HD_DAT}		0	70	0		ns
Rising time of SCL signal	t_{RCL}		10	40	20 x 0.1Cb	300	ns
Rising time of SCL signal after a repeated start command and after an acknowledge bit	t_{FCL1}		10	80	20 x 0.1 x C_B	300	ns
Falling time of SCL signal	t_{FCL}		10	40	20 x 0.1 x C_B	300	ns
Rising time of SDA signal	t_{FDA}		10	80	20 x 0.1 x C_B	300	ns
Falling time of SDA signal	t_{FDA}		10	80	20 x 0.1 x C_B	300	ns
Set-up time for stop command	t_{SU_STO}		160		600		ns
Bus free time between a stop and start command	t_{BUF}		160		1300		ns
Data valid time	t_{VD_DAT}			16		90	ns
Data valid acknowledge time	t_{VD_ACK}			160		900	ns
Capacitive load for each bus line	C_B	SDA and SCL line		100		400	pF
		SDAH + SDA line and SCLH + SCL line		400		400	pF
Noise margin at the low level	C_I	For each connected device		0.1 x V_{CC}	0.1 x V_{CC}		V
Noise margin at the high level	V_{NH}	For each connected device		0.2 x V_{CC}	0.2 x V_{CC}		V

Notes:

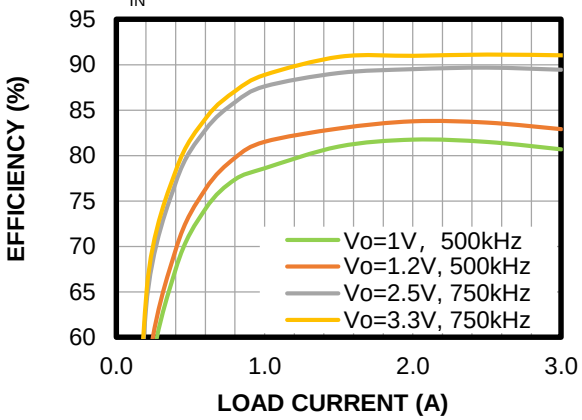
9) Not tested in production. Guaranteed by over-temperature correlation.
10) Not tested in production. Guaranteed by engineering sample characterization.
11) The maximum I²C bus voltage should be below 4V. A 1.8V or 3.3V typical bus voltage is recommended.

TYPICAL CHARACTERISTICS

Performance curves are tested on the evaluation board. V_{IN} = 12V, T_A = 25°C, unless otherwise noted.

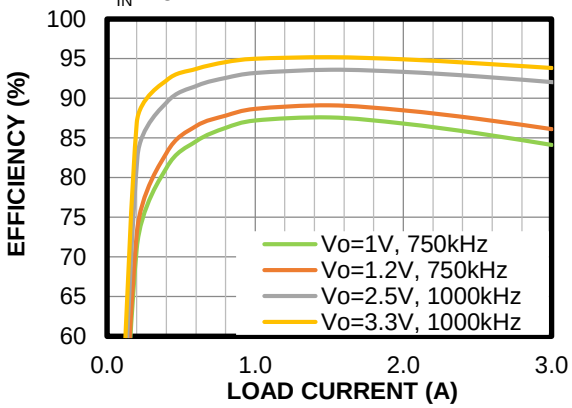
Efficiency vs. Load Current

V_{IN} = 12V



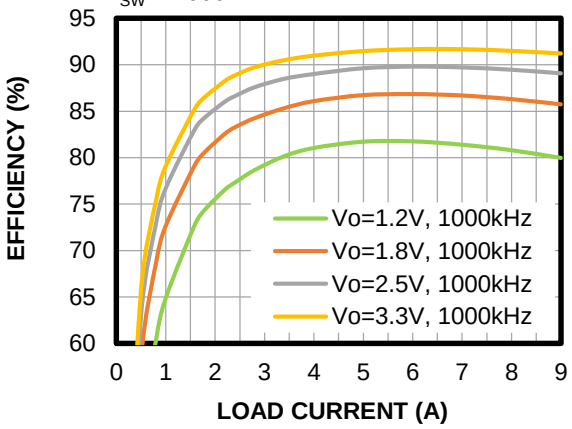
Efficiency vs. Load Current

V_{IN} = 5V



Efficiency vs. Load Current

3-phase paralleled, V_{IN} = 12V,
f_{SW} = 1000kHz

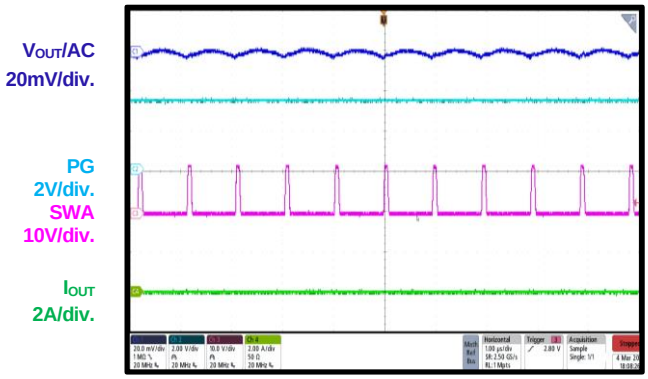


TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board. V_{IN} = 12V, T_A = 25°C, unless otherwise noted.

Steady State

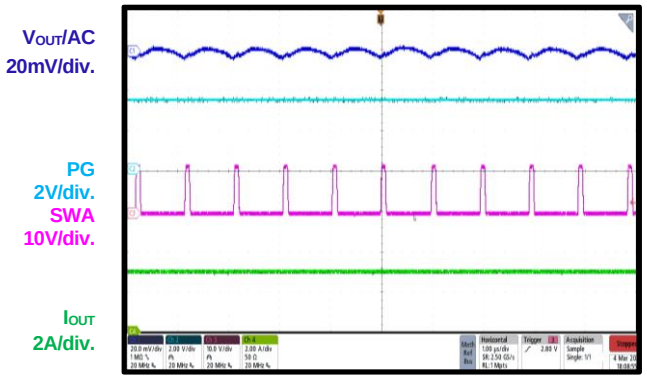
V_{IN} = 12V, V_{OUT} = 1V, I_{OUT} = 0A, C_{OUT} = 3 x 22µF, voltage ripple = 4.6mV, single channel



1µs/div.

Steady State

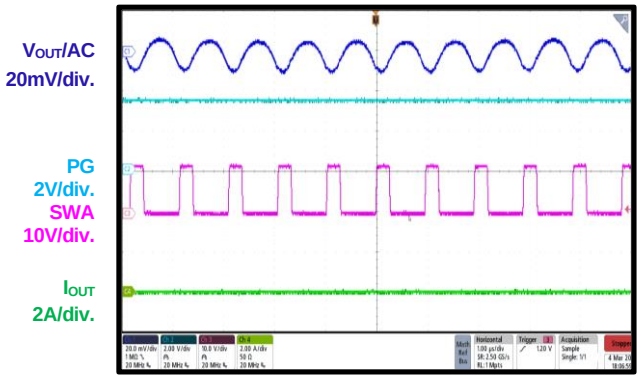
V_{IN} = 12V, V_{OUT} = 1V, I_{OUT} = 3A, C_{OUT} = 3 x 22µF, voltage ripple = 5.6mV, single channel



1µs/div.

Steady State

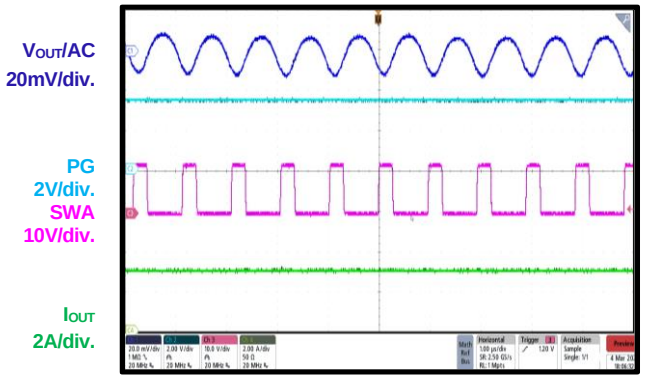
V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A, C_{OUT} = 3 x 22µF, voltage ripple = 15.8mV, single channel



1µs/div.

Steady State

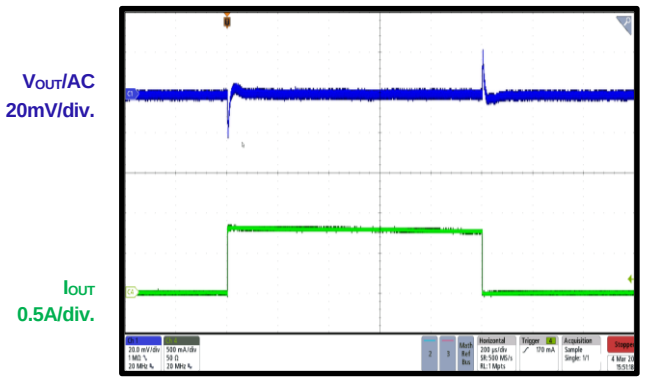
V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 3A, C_{OUT} = 3 x 22µF, voltage ripple = 16.4mV, single channel



1µs/div.

Load Transient Response

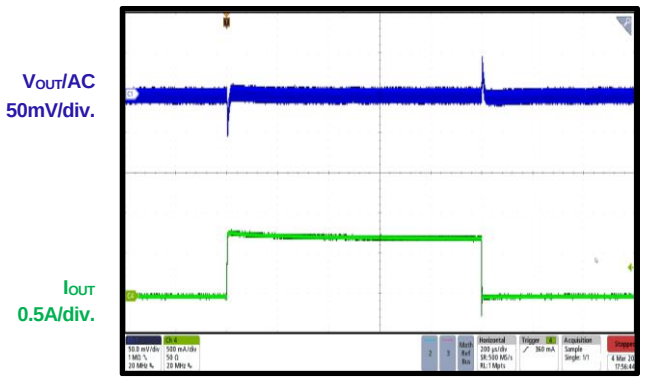
V_{IN} = 12V, V_{OUT} = 1V, I_{OUT} = 0A to 0.75A, slew rate = 10A/µs, C_{OUT} = 3 x 22µF, single channel



200µs/div.

Load Transient Response

V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A to 0.75A, slew rate = 10A/µs, C_{OUT} = 3 x 22µF, single channel



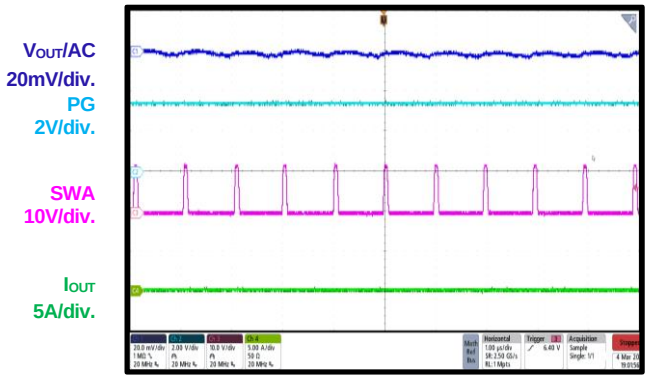
200µs/div.

TYPICAL CHARACTERISTICS

Performance waveforms are tested on the evaluation board. V_{IN} = 12V, T_A = 25°C, unless otherwise noted.

Steady State

V_{IN} = 12V, V_{OUT} = 1V, I_{OUT} = 0A,
voltage ripple = 3.1mV, three outputs in parallel



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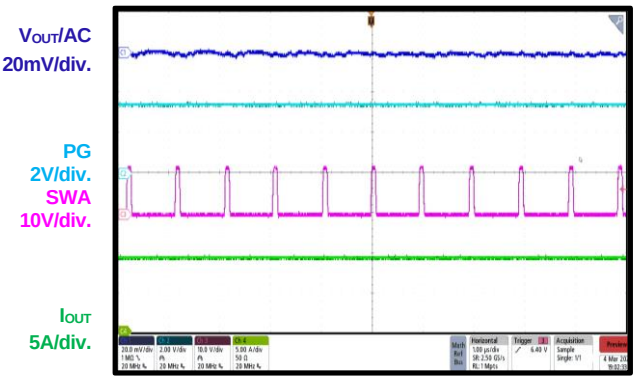
Steady State

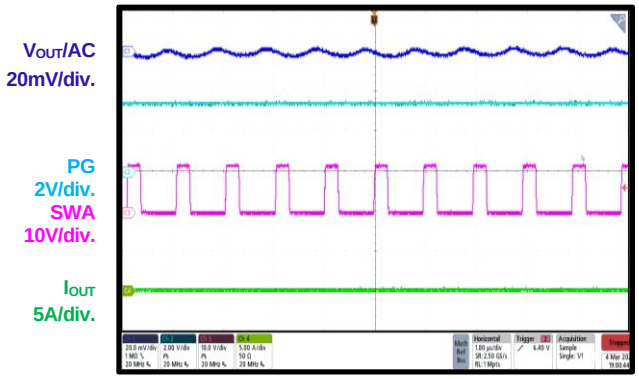
V_{IN} = 12V, V_{OUT} = 1V, I_{OUT} = 9A,
voltage ripple = 3.5mV, three outputs in parallel



1µs/div.

Steady State

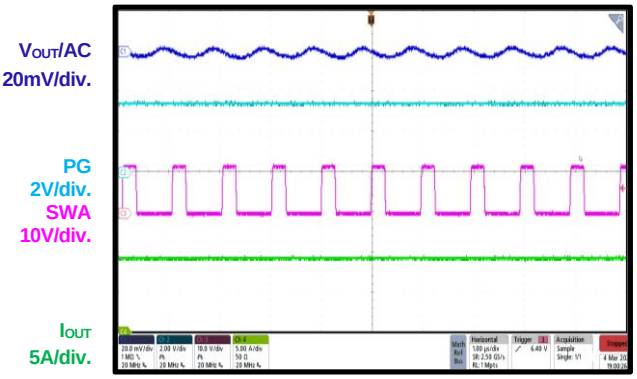
V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A,
voltage ripple = 5.8mV, three outputs in parallel



1µs/div.

Steady State

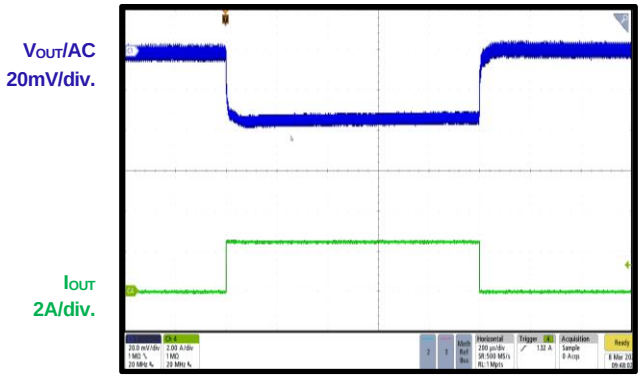
V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 9A,
voltage ripple = 6.2mV, three outputs in parallel



1µs/div.

Load Transient Response

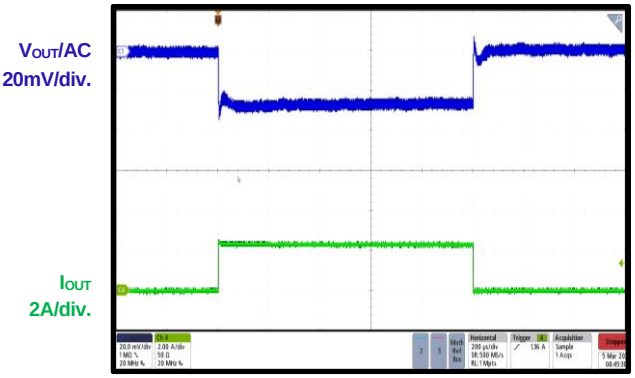
V_{IN} = 12V, V_{OUT} = 1V, I_{OUT} = 0A to 2.25A,
slew rate = 10A/µs, C_{OUT} = 9 x 22µF, three outputs in parallel



200µs/div.

Load Transient Response

V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A to 2.25A,
slew rate = 10A/µs, C_{OUT} = 9 x 22µF, three outputs in parallel



200µs/div.

FUNCTIONAL BLOCK DIAGRAM

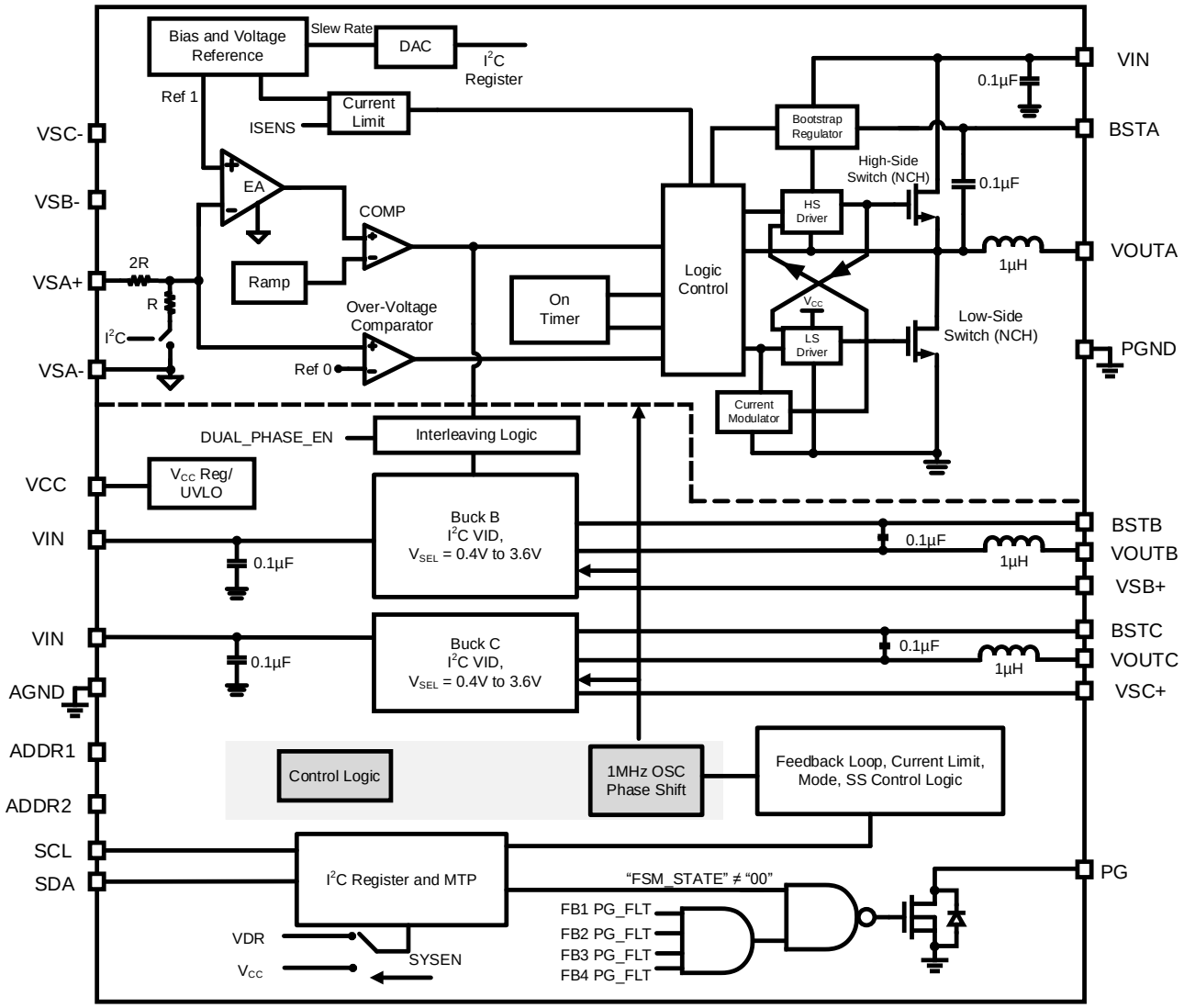


Figure 1: Functional Block Diagram

OPERATION

The MPM54313 is a triple-output power module with integrated inductor, built-in power-on/-off sequencing control, soft start, compensation, over-voltage protection (OVP), over-current protection (OCP), and under-voltage protection (UVP). Fixed-frequency constant-on-time (COT) control provides fast transient response.

Power Supply Input and Under-Voltage Protection (UVP)

VIN is the power supply of the power module. When the input voltage (V_{IN}) exceeds the UVP rising threshold voltage, the three channels' bucks (buck A, buck B, and buck C) start up if all the start-up conditions are met. The bucks shut down when V_{IN} falls below the UVP falling threshold.

Internal VCC Supply

VCC is the power supply for the internal driver and control circuitries. A decoupling capacitor is required on VCC to stabilize the regulator and reduce the ripple. The regulator takes the VIN input and operates across the full V_{IN} range. If V_{IN} exceeds 3.5V, the output of the regulator is in full regulation. If V_{IN} falls below 3.5V, the output of the regulator decreases following the changes in V_{IN}.

Enable (EN)

When V_{IN} exceeds the under-voltage lockout (UVLO) threshold, the MPM54313 can be enabled by pulling the EN pin above 1.2V. Leave the EN pin floating or pull it down to ground to disable the MPM54313. There is an internal 2.7MΩ resistor connected from the EN pin to ground.

If EN is pulled high and reaches the V_{IN} UVLO threshold, BUCKx_CTRL_REG (0Ch), bits[7:5] can enable or disable the three channels after the power-on sequence is complete. If the power-on sequence set via 19h~1Ch, bit[7] = 1'b0, then the outputs of the three channels are disabled by default. Once EN and VIN are ready, 0Ch can enable the three channels.

When the MPM54313 is disabled, the part goes into output discharge or soft shutdown mode if the two functions are enabled.

Power-On Sequence

After the VIN supply is valid and EN is pulled high, the MPM54313 executes the power-on sequence (Config0 to Config3) as configured via registers 0x19~0x1F to enable its output regulators following the specified sequence (see Figure 2). When V_{IN} reaches the UVLO threshold and EN goes to high, after a 2ms system delay, each channel follows the start-up delay time, soft-start time, and PON_SEQ_DELAY time to execute the power-on sequence. Before enabling each channel, the MPM54313 loads the default voltage value of each channel from the multiple-time programmable (MTP) memory registers.

The soft-start time for each channel can be configured via SOFT_START_REG (13h).

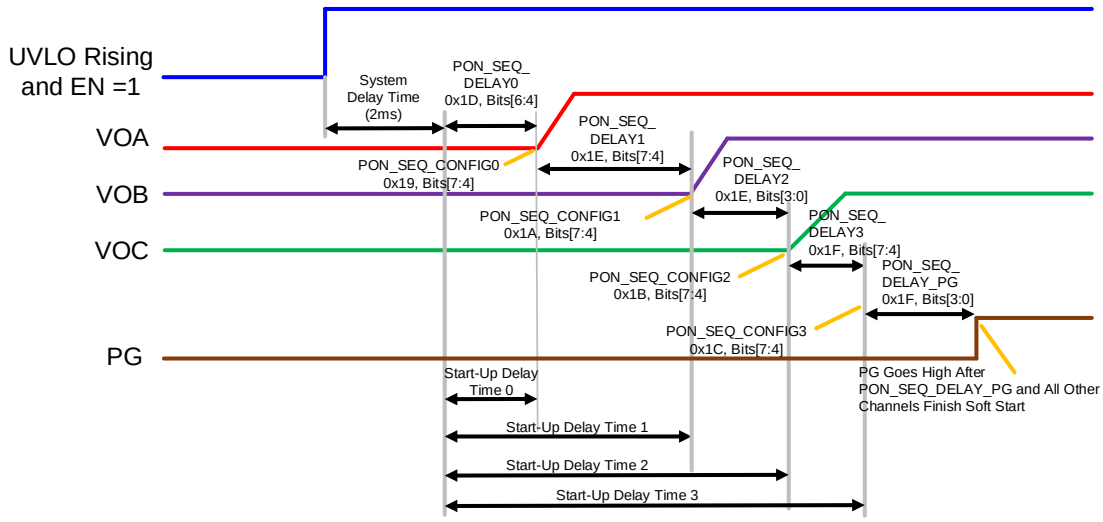


Figure 2: Power-On Timing Diagram

Power-Off Sequence

If the EN pin is logic low or V_{IN} is below its UVLO threshold, the MPM54313 enters the power-off sequence set via registers 0x1D~0x23 (see Figure 3). After each channel finishes its off delay, the MPM54313 turns off each channel sequentially via discharging or soft-stop if both of these functions are enabled. The discharge function can be enabled/disabled, and the discharge resistor can be configured via DISCHARGE_R_REG (0Eh). The soft-stop function and the soft-stop time can be configured via SOFT_STOP_EN_REG (11h), bits[7:5] and SOFT_STOP_REG (12h), bits[7:2], respectively.

During the power-off sequence while under a UVLO falling condition, if the UVLO rising threshold is detected again, all channels continue to execute the power-off sequence. Then the channels turn on sequentially following the new power-on sequence.

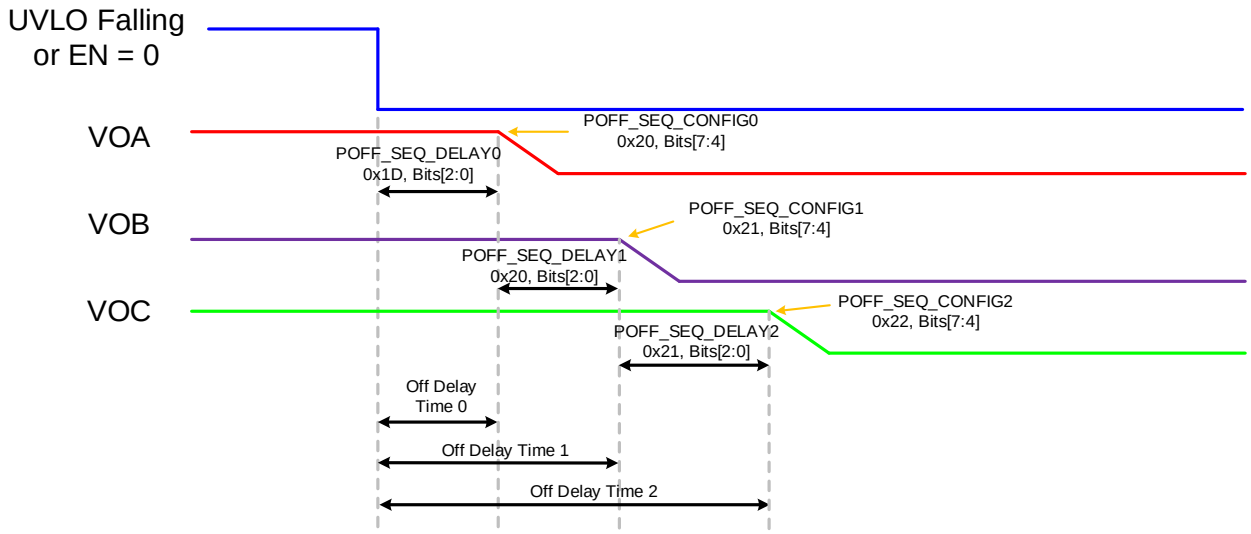


Figure 3: Power-Off Timing Diagram

Pre-Biased Start-Up

The MPM54313 has been designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the internal BST voltage is refreshed and charged, and the voltage on the internal soft-start capacitor is also charged. If the BST voltage exceeds its rising threshold voltage and the soft-start capacitor voltage exceeds the sensed output voltage at the FB pin, the device starts to work normally.

Power Good (PG)

The MPM54313 has a power good (PG) output used to indicate whether the enabled buck's output voltage is ready. The PG pin is an open-drain output. Connect the PG pin to VCC or another voltage source through a pull up resistor (e.g. 10kΩ). The PG pin is pulled high after PON_SEQ_DELAY_PG and all channels finish soft start (if they are enabled). During normal operation, the PG pin pulls low if any fault status occurs.

Output Over-Voltage Protection (OVP)

The MPM54313 monitors the output voltage (V_{OUT}) and enters OVP latch-off mode if V_{OUT} exceeds V_{OVP1_H}. After triggering output OVP, all channels turn off, and the PG pin pulls low. The MPM54313 does not automatically turn on again until the OV condition is removed, and there is either a power-on sequence or the power on EN is recycled.

Input Over-Voltage Protection (V_{IN} OVP)

If V_{IN} exceeds the 15V threshold for longer than 2µs, the MPM54313 turns off and the V_{IN} OVP status bit (STATUS_0 (00h), bit[1]) is set from 0 to 1.

Even the V_{IN} OVP condition is removed, the MPM54313 does not automatically turn on until there is either a power-on sequence or the power on EN is recycled. STATUS_0 (00h), bit[1] stays set to 1 until a power/EN recycle event, or if the host clears the fault by writing the related clear bit to 1 via CLEAR_0 (07h), bit[1].

Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

The MPM54313 has fixed 3.6A valley current limit control. When the low-side MOSFET (LS-FET) is turning on, the inductor current (I_L) is monitored. If the sensed I_L exceeds the valley current limit threshold, the device sends an over-current (OC) fault warning via OC_STATUS_CLEAR (2Ah). The high-side MOSFET (HS-FET) is not allowed to turn on until the valley current drops below the OC threshold. Meanwhile, V_{OUT} drops until it falls below its UV threshold.

If the UV and OC conditions are both triggered, OCP latches the device off. This means that the chip disables the output power stage. The MPM54313 does not automatically turn on again until the UV and OCP conditions are removed, and power is cycled on EN.

Output Discharge

To discharge the output capacitor's energy during the power-off sequence or shutdown sequence, there is discharge path from the VOx pin to ground. The discharge function can be enabled via the MTP interface, as well as the discharge resistor.

Soft Start and Soft Stop

The MPM54313 employs a soft-start and soft-stop mechanism to ensure smooth output during the power-on and power-off sequences.

When the part is enabled and the BST voltage reaches its rising threshold, the internal digital-to-analog converter (DAC) outputs a ramp voltage (reference voltage). V_{OUT} smoothly ramps up with the reference voltage. When the DAC output reaches the final voltage, it stops at that level. At this point, soft start finishes and the device enters steady state operation.

When the part is disabled, the internal DAC ramps down the reference voltage. The output voltage follows the soft-stop slew rate with the reference voltage until the output drops to 0.15V. Then soft stop is finished, and the output is discharged by a 30Ω discharge resistor.

The start-up delay, shutdown delay, and soft-start and soft-stop time can be configured via the MTP.

Interleaving for Buck A and Buck B

The MPM54313 supports 2-phase interleaving mode for buck A and buck B by setting PROTECT_REG (14h), bit[5] = 1. VSA+ should be connected to VSB+ for interleaving work mode.

Figure 4 shows how the internal SET signal is triggered when buck A/B's FB signal is below the internal REF signal. When the SET signal becomes high, only one phase's pulse-width modulation (PWM) output becomes high; the next time SET becomes high, the next phase's PWM output becomes high. This process achieves automatic interleaving.

When buck A and buck B work in dual-phase interleaving operation mode, the MPM54313 senses two phase currents and automatically tunes the buck's on time (t_{ON}) to achieve active paralleled current balancing.

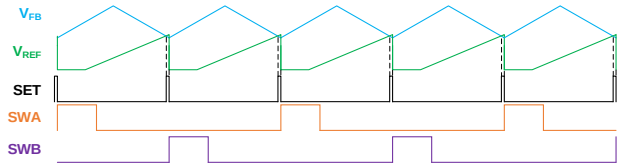


Figure 4: Dual-Phase Interleaving Mode

Active Voltage Positioning (AVP)

The MPM54313 supports active voltage positioning (AVP) by setting the AVP_EN bits (ACTIVE_POSITION_ENABLE_A/B (71h), bit[7] and ACTIVE_POSITION_ENABLE_C (79h), bit[7]) to 1 via the I²C. Once enabled, the output voltage of the corresponding channel drops in proportion with the load current. V_{DROOP} and V_{OUT} can be calculated with Equation (1) and Equation (2), respectively:

$$V_{DROOP} = I_{OUT} \times R_{DROOP} \quad (1)$$

$$V_{OUT} = V_{REF} - V_{DROOP} \quad (2)$$

Where V_{DROOP} is the droop voltage, R_{DROOP} is the droop resistance with a typical value of 40mΩ, and V_{REF} is the reference voltage of each channel.

The AVP function enables on-demand parallel operation, where the three outputs can be paralleled in any combination without pre-setting any registers (see Figure 5 on page 17). The current of the paralleled channel(s) is inherently balanced by the droop voltage created by the AVP function.

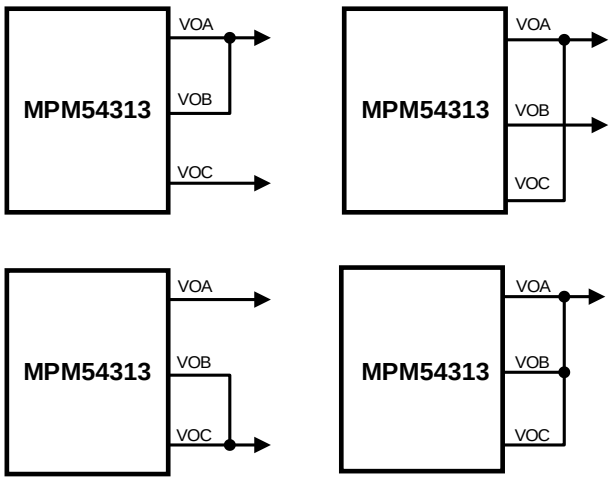


Figure 5: On-Demand Parallel Options

Analog To Digital Converter (ADC)

The MPM54313 supports an analog to digital converter (ADC) to monitor the regulator's output voltage and current/power.

Thermal Shutdown

The MPM54313 employs thermal shutdown by internally monitoring the IC's junction temperature (T_J). If T_J exceeds the 145°C threshold, the converter shuts off following the soft-stop ramp down slew rate if the function is enabled. This is non-latch protection. There is a hysteresis of about 20°C. Once T_J drops to about 125°C, the device initiates a soft start.

Multiple-Time Programmable (MTP) Configurations

After V_{IN} powers up, the system-on-chip (SoC) configures the MPM54313's I²C register and MTP. Refer to the I²C Address Selection section on page 18 for details on how to identify a valid slave address. When the SoC writes to the I²C register, the I²C register takes effect immediately; it can also be burned into the MTP. During any buck's normal operation, the I²C master can read and write to the register's data online.

I²C INTERFACE

I²C Serial Interface Description

The I²C is a two-wire, bidirectional, serial interface consisting of a data line (SDA) and a clock line (SCL). The lines are pulled to a bus voltage externally when they are idle. When connecting to the line, a master device generates the SCL signal and device address, and arranges the communication sequence. The MPM54313 interface is an I²C slave. The I²C interface adds flexibility to the power supply solution.

I²C Address Selection

Two ADDRx pins configure the lower 4 bits of the I²C address. Table 1 shows the different configurations of the two ADDRx pins for the lower 4 bits (bits[3:0]). The higher bits (bits[6:4]) can be modified by writing to I2C_ADDRESS (73h), bits[3:1], respectively.

Table 1: I²C Address of the MPM54313

ADDR1	ADDR2	I²C Address
Low	Low	0xxx 1001
Low	Float	0xxx 1100
Low	High	0xxx 1110
Float	Low	0xxx 1010
Float	Float	0xxx 1000
Float	High	0xxx 1111
High	Low	0xxx 1011
High	Float	0xxx 1101
High	High	0xxx 0111

Data Validity

One clock pulse is generated for each data bit transferred. The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can only change when the clock signal on the SCL line is low (see Figure 6).

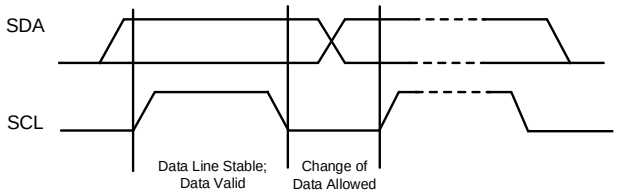


Figure 6: Bit Transfer on the I²C Bus

Start and stop commands are signaled by the master device, which signifies the beginning and the end of the I²C transfer. The start command is defined as the SDA signal transitioning from high to low while the SCL is high. The stop command is defined as the SDA signal transitioning from low to high while the SCL is high (see Figure 7).

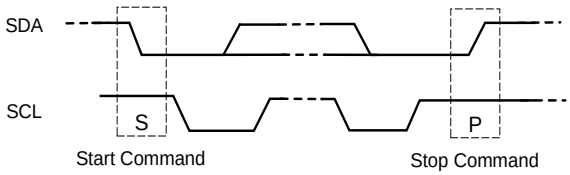


Figure 7: Start and Stop Conditions

Start and stop commands are always generated by the master. The bus is considered to be busy after the start command, and it is considered to be free again a minimum of 4.7µs after the stop command. The bus remains busy if a repeated start (Sr) command is generated instead of a stop command. The start (S) and repeated start (Sr) commands are functionally identical.

Transfer Data

Every byte put on the SDA line must be 8 bits. Each byte has to be followed by an acknowledge (ACK) bit. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (high) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse so that it remains stable low during the high period of this clock pulse.

Figure 8 shows the format for data transfers. After the start command, a slave address is sent. This address is 7 bits followed by an 8th bit data direction bit (R/W). A 0 indicates a transmission (write), and a 1 indicates a request for data (read). A data transfer is always terminated by a stop command, which is generated by the master. However, if a master device still wishes to communicate on the bus, it can generate a repeated start command and address another slave device without first generating a stop command.

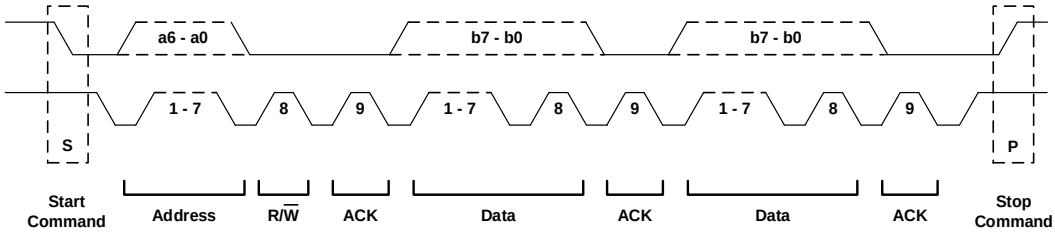


Figure 8: Complete Data Transfer

The MPM54313 requires a start command, a valid I²C address, a register address byte, and a data byte for a single data update. After receiving each byte, the MPM54313 acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the MPM54313. The MPM54313 performs an update on the falling edge of the LSB byte. Figure 9 shows an I²C write example. Figure 10 shows an I²C read example.

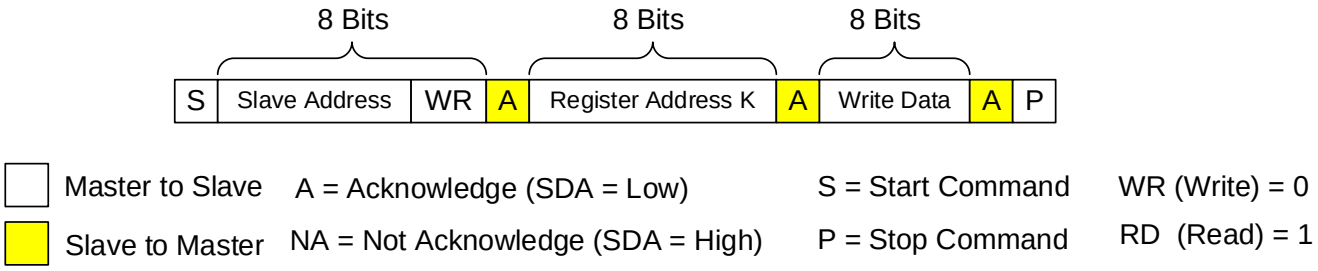


Figure 9: I²C Write Example (Write Single Register)

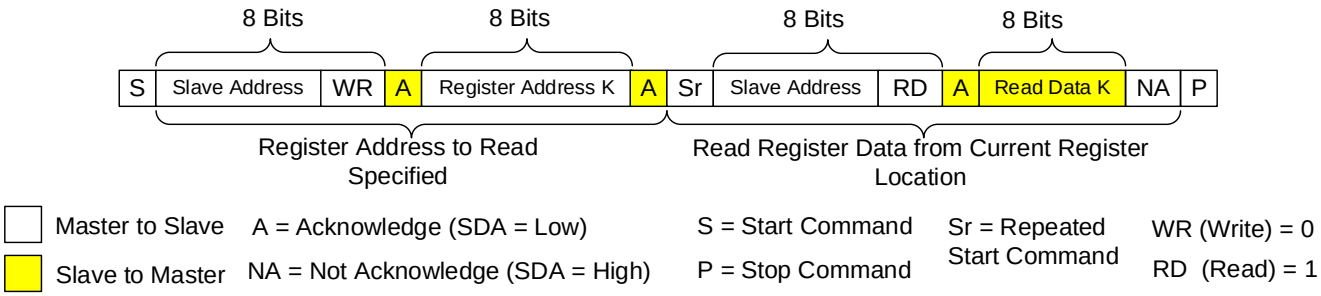


Figure 10: I²C Read Example (Read Single Register)

SUPPORTED PMBUS COMMANDS

Command Code	Command Name	Type	Bytes
00h	STATUS_0	R	1
01h	STATUS_1	R	1
02h	BUCK_A_CURRENT/PWR_METER	R	1
03h	BUCK_B_CURRENT/PWR_METER	R	1
04h	BUCK_C_CURRENT/PWR_METER	R	1
06h	BUCKX_VOLTAGE	R	1
07h	CLEAR_0	Send	1
08h	CLEAR_1	Send	1
09h	MASK_0	R/W	1
0Ah	MASK_1	R/W	1
0Bh	REMOTE_REG	R/W	1
0Ch	BUCKX_CTRL_REG	R/W	1
0Dh	PG_REG	R/W	1
0Eh	DISCHARGE_R_REG	R/W	1
0Fh	SW_FREQ_REG	R/W	1
10h	MONITOR_EN_REG	R/W	1
11h	SOFT_STOP_EN_REG	R/W	1
12h	SOFT_STOP_REG	R/W	1
13h	SOFT_START_REG	R/W	1
14h	PROTECT_REG	R/W	1
15h	BUCK_A_VOUT	R/W	1
16h	BUCK_B_VOUT	R/W	1
17h	BUCK_C_VOUT	R/W	1
19h	PON_CONFIG_0	R/W	1
1Ah	PON_CONFIG_1	R/W	1
1Bh	PON_CONFIG_2	R/W	1
1Ch	PON_CONFIG_3	R/W	1
1Dh	PON_OFF_DELAY0	R/W	1
1Eh	PON_SEQ_DELAY_1_2	R/W	1
1Fh	PON_SEQ_DELAY_3_PG	R/W	1
20h	POFF_SEQ_CONFIG_0	R/W	1
21h	POFF_SEQ_CONFIG_1	R/W	1
22h	POFF_SEQ_CONFIG_2	R/W	1
23h	POFF_SEQ_CONFIG_3	R/W	1
24h	ADC_TEMP	R	1
25h	VOUT_RANGE_SELECT	R/W	1
2Ah	OC_STATUS_CLEAR	R/W	1
30h	MTP_AUTO_REG	R/W	1
31h	PART_ID	R	1
35h	CODE_ID	R	1
36h	CODE_VERSION	R	1
71h	ACTIVE_POSITION_ENABLE_A/B	R/W	1
73h	I2C_ADDRESS	R/W	1
79h	ACTIVE_POSITION_ENABLE_C	R/W	1
90h	VIN_OV_REG	R/W	1
AFh	VIN_UVLO_REG	R/W	1

REGISTER SETTINGS

STATUS REGISTERS

The status registers (STATUS_0 and STATUS_1) are updated to 1 if the relevant event occurs. The status registers remain set to 1, even if the failing condition is no longer present, until the clear command is generated by the host. In addition, if V_{IN} falls below its UVLO threshold, the status register is initialized to 0. The PWR_GOOD interrupt may be generated by the MPM54313 at the same time that V_{IN} falls below its UVLO threshold depending on the type of event. The interrupts are only generated if they are not masked.

All read-only (RO) registers are one-time latched registers. In other words, once the MPM54313 sets those register flags, the host must explicitly clear those registers appropriately. The MPM54313 does not automatically update the registers on its own, even if the event that triggered the status is no longer present.

STATUS_0 (00h)

Format: Unsigned binary

The STATUS_0 command monitors the over-temperature (OT), buck output power not good, and V_{IN} over-voltage (OV) statuses.

Bits	Access	Bit Name	Default	Description
7	R	RESERVED	N/A	Reserved.
6	R	OVER_TEMP_STATUS	1'b0	1'b0: No critical temperature shutdown has occurred 1'b1: A critical temperature shutdown has occurred
5	R	BUCK_A_POWER_NOT_GOOD_STATUS	1'b0	1'b0: Buck A's output power is good 1'b1: Buck A's output power is not good
4	R	BUCK_B_POWER_NOT_GOOD_STATUS	1'b0	1'b0: Buck B's output power is good 1'b1: Buck B's output power is not good
3	R	BUCK_C_POWER_NOT_GOOD_STATUS	1'b0	1'b0: Buck C's output power is good 1'b1: Buck C's output power is not good
2	R	RESERVED	N/A	Reserved.
1	R	VIN_OV_STATUS	1'b0	1'b0: No V_{IN} OV condition has occurred 1'b1: A V_{IN} OV condition has occurred
0	R	RESERVED	N/A	Reserved.

STATUS_1 (01h)

Format: Unsigned binary

The STATUS_1 command monitors the buck outputs' over-voltage (OV) and under-voltage (UV) statuses.

Bits	Access	Bit Name	Default	Description
7	R	BUCK_A_OV_STATUS	1'b0	1'b0: No buck A output OV condition has occurred 1'b1: A buck A output OV condition has occurred
6	R	BUCK_B_OV_STATUS	1'b0	1'b0: No buck B output OV condition has occurred 1'b1: A buck B output OV condition has occurred
5	R	BUCK_C_OV_STATUS	1'b0	1'b0: No buck C output OV condition has occurred 1'b1: A buck C output OV condition has occurred
4	R	RESERVED	N/A	Reserved.
3	R	BUCK_A_UV_STATUS	1'b0	1'b0: No buck A output UV condition has occurred 1'b1: A buck A output UV condition has occurred

2	R	BUCK_B_UV_STATUS	1’b0	1’b0: No buck B output UV condition has occurred 1’b1: A buck B output UV condition has occurred
1	R	BUCK_C_UV_STATUS	1’b0	1’b0: No buck C output UV condition has occurred 1’b1: A buck C output UV condition has occurred
0	R	RESERVED	N/A	Reserved.

BUCK_A_CURRENT/PWR_METER (02h)

Format: Direct

The BUCK_A_CURRENT/PWR_METER command monitors buck A’s output current/power.

Bits	Access	Bit Name	Description
7:0	R	BUCK_A_ADC_ CURRENT/POWER	If register 0x10, bit[3] = 0: returns buck A’s output current or output power measurement. Returns buck A’s output current ADC report. 8’b 0000 0000: Reserved 8’b 0000 0001: 0.125A or 125mW 8’b 0000 0010: 0.25A or 250mW 8’b 0000 0011: 0.375A or 375mW … 8’b 0011 1100: 7.5A or 7500mW 8’b 0011 1101: 7.625A or 7625mW 8’b 0011 1110: 7.75A or 7750mW 8’b 0011 1111: ≥7.875A or 7875mW If register 0x10, bit[3] = 1: returns the sum of buck a, buck b, and buck c’s output power. 8’b 0000 0000: Reserved 8’b 0000 0001: 125mW 8’b 0000 0010: 250mW 8’b 0000 0011: 375mW … 8’b 1111 1100: 31500mW 8’b 1111 1101: 31625mW 8’b 1111 1110: 31750mW 8’b 1111 1111: ≥31875mW

BUCK_B_CURRENT/PWR_METER (03h)

Format: Direct

The BUCK_B_CURRENT/PWR_METER command monitors buck B’s output current/power.

Bits	Access	Bit Name	Description
7:0	R	BUCK_B_ADC_ CURRENT/POWER	Returns buck B’s output current ADC report. 8’b 0000 0000: Reserved 8’b 0000 0001: 0.125A or 125mW 8’b 0000 0010: 0.25A or 250mW 8’b 0000 0011: 0.375A or 375mW … 8’b 0011 1100 = 7.5A or 7500mW 8’b 0011 1101 = 7.625A or 7625mW 8’b 0011 1110 = 7.75A or 7750mW 8’b 0011 1111: ≥7.875A or 7875mW

BUCK_C_CURRENT/PWR_METER (04h)

Format: Direct

The BUCK_C_CURRENT/PWR_METER command monitors buck C's output current/power.

Bits	Access	Bit Name	Description
7:0	R	BUCK_C_ADC_ CURRENT/POWER	Returns buck C's output current ADC report. 8'b 0000 0000: Reserved 8'b 0000 0001: 0.125A or 125mW 8'b 0000 0010: 0.25A or 250mW 8'b 0000 0011: 0.375A or 375mW … 8'b 0011 1100: 7.5A or 7500mW 8'b 0011 1101: 7.625A or 7625mW 8'b 0011 1110: 7.75A or 7750mW 8'b 0011 1111: ≥7.875A or 7875mW

BUCKX_VOLTAGE (06h)

Format: Direct

The BUCKX_VOLTAGE command monitors each buck's output voltage.

Bits	Access	Bit Name	Description
7:0	R	BUCKX_ADC_ VOLTAGE	Changes each buck's output voltage measurement according to MONITOR_EN_REG (10h), bit[6] and bit[5]. 8'b 0000 0000: Undefined 8'b 0000 0001: 15mV 8'b 0000 0010: 30mV … 8'b 1111 1111: ≥3825mV

CLEAR REGISTERS

For each real-time status register (STATUS_0 and STATUS_1), the MPM54313 offers a way to clear the status of each event. All clear registers are write to 1 only. When 1 is written to any of the clear registers, the MPM54313 updates the status registers to a default state and removes the interrupt condition on the PWR_GOOD output signal, assuming that event is no longer present. If the failing condition is still present, the status register remains set to 1. Note that a PWR_GOOD interrupt is only applicable if that event is not masked.

The MPM54313 offers a global clear command by writing 1 to CLEAR_0 (07h), bit[0]. This command works the same way as an individual clear command. This command can be used by the host if more than one clear command is required for different registers.

CLEAR_0 (07h)

Format: Unsigned binary

The CLEAR_0 command clears buck output power not good statuses, V_{IN} over-voltage protection (OVP) statuses, and offers a global clear function for all registers.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5	R/W	CLEAR_BUCK_A_ POWER_NOT_GOOD_ STATUS	1'b0	1'b1: Clears STATUS_0 (00h), bit[5]
4	R/W	CLEAR_BUCK_B_ POWER_NOT_GOOD_ STATUS	1'b0	1'b1: Clears STATUS_0 (00h), bit[4]

3	R/W	CLEAR_BUCK_C_	1’b0	1’b1: Clears STATUS_0 (00h), bit[3]
2	R	POWER_NOT_GOOD_	N/A	Reserved.
1	R/W	CLEAR_VIN_ OVP_STATUS	1’b0	1’b1: Clears STATUS_0 (00h), bit[1]
0	R/W	CLEAR_GLOBAL	1’b0	1’b1: Clears all status registers (00h~01h)

CLEAR_1 (08h)

Format: Unsigned binary

The CLEAR_1 command clears buck A, buck B, and buck C’s output over-voltage (OV) and under-voltage (UV) statuses.

Bits	Access	Bit Name	Default	Description
7	R/W	CLEAR_BUCK_A_OV_ STATUS	1’b0	1’b1: Clears STATUS_1 (01h), bit[7]
6	R/W	CLEAR_BUCK_B_OV_ STATUS	1’b0	1’b1: Clears STATUS_1 (01h), bit[6]
5	R/W	CLEAR_BUCK_C_OV_ STATUS	1’b0	1’b1: Clears STATUS_1 (01h), bit[5]
4	R	RESERVED	N/A	Reserved.
3	R/W	CLEAR_BUCK_A_UV_ STATUS	1’b0	1’b1: Clears STATUS_1 (01h), bit[3]
2	R/W	CLEAR_BUCK_B_UV_ STATUS	1’b0	1’b1: Clears STATUS_1 (01h), bit[2]
1	R/W	CLEAR_BUCK_C_UV_ STATUS	1’b0	1’b1: Clears STATUS_1 (01h), bit[1]
0	R	RESERVED	N/A	Reserved.

MASK REGISTERS

For each real-time status register, the MPM54313 offers a way to mask the status of each event.

MASK_0 (09h)

Format: Unsigned binary

The MASK_0 command masks buck A, buck B, and buck C’s output power not good and V_{IN} over-voltage protection (OVP) statuses.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5	R/W	MASK_BUCK_A_ POWER_NOT_GOOD_ STATUS	1’b0	1’b1: Masks STATUS_0 (00h), bit[5]
4	R/W	MASK_BUCK_B_ POWER_NOT_GOOD_ STATUS	1’b0	1’b1: Masks STATUS_0 (00h), bit[4]
3	R/W	MASK_BUCK_C_ POWER_NOT_GOOD_ STATUS	1’b0	1’b1: Masks STATUS_0 (00h), bit[3]
2	R	RESERVED	N/A	Reserved.
1	R/W	MASK_VIN_OVP_ STATUS	1’b0	1’b1: Masks STATUS_0 (00h), bit[1]
0	R	RESERVED	N/A	Reserved.

MASK_1 (0Ah)

Format: Unsigned binary

The MASK_1 command masks buck A, buck B, and buck C's output over-voltage (OV) and over-current (OC) statuses.

Bits	Access	Bit Name	Default	Description
7	R/W	MASK_BUCK_A_OV_STATUS	1'b0	1'b1: Masks STATUS_1 (01h), bit[7]
6	R/W	MASK_BUCK_B_OV_STATUS	1'b0	1'b1: Masks STATUS_1 (01h), bit[6]
5	R/W	MASK_BUCK_C_OV_STATUS	1'b0	1'b1: Masks STATUS_1 (01h), bit[5]
4	R	RESERVED	N/A	Reserved.
3	R/W	MASK_BUCK_A_OC_STATUS	1'b0	1'b1: Masks STATUS_1 (01h), bit[3]
2	R/W	MASK_BUCK_B_OC_STATUS	1'b0	1'b1: Masks STATUS_1 (01h), bit[2]
1	R/W	MASK_BUCK_C_OC_STATUS	1'b0	1'b1: Masks STATUS_1 (01h), bit[1]
0	R	RESERVED	N/A	Reserved.

THRESHOLD AND CONFIGURATION REGISTERS

REMOTE_REG (0Bh)

Format: Unsigned binary

The REMOTE_REG command enables remote sensing for buck A, buck B, and buck C.

Bits	Access	Bit Name	Default	Description
7	R/W	BUCK_A_REMOTE_EN	1'b0	Enables buck A's remote sensing. 1'b0: Disabled 1'b1: Enabled
6	R/W	BUCK_B_REMOTE_EN	1'b0	Enables buck B's remote sensing. 1'b0: Disabled 1'b1: Enabled
5	R/W	BUCK_C_REMOTE_EN	1'b0	Enables buck C's remote sensing. 1'b0: Disabled 1'b1: Enabled
4:0	R	RESERVED	N/A	Reserved.

BUCKX_CTRL_REG (0Ch)

Format: Unsigned binary

The BUCKX_CTRL_REG command sets pulse-frequency modulation (PFM) or pulse-width modulation (PWM) mode for buck A, buck B, and buck C.

Bits	Access	Bit Name	Default	Description
7	R/W	BUCK_A_EN	1'b1	Enables buck A's output regulator. 1'b 0: Disabled 1'b 1: Enabled
6	R/W	BUCK_B_EN	1'b1	Enables buck B's output regulator. 1'b0: Disabled 1'b1: Enabled

5	R/W	BUCK_C_EN	1’b1	Enables buck C’s output regulator. 1’b0: Disabled 1’b1: Enabled
4	R	RESERVED	N/A	Reserved.
3	R/W	PWM_BUCK_A	1’b0	Selects buck A’s PWM mode (auto mode or forced PWM). 1’b0: Forced PWM 1’b1: Auto mode
2	R/W	PWM_BUCK_B	1’b0	Selects buck B’s PWM mode (auto mode or forced PWM). 1’b0: Forced PWM 1’b1: Auto mode
1	R/W	PWM_BUCK_C	1’b0	Selects buck C’s PWM mode (auto mode or forced PWM). 1’b0: Forced PWM 1’b1: Auto mode
0	R	RESERVED	N/A	Reserved.

PG_REG (0Dh)

Format: Unsigned binary

The PG_REG command sets buck A, buck B, and buck C’s power good (PG) threshold.

Bits	Access	Bit Name	Default	Description
7	R	RESERVED	N/A	Reserved.
6	R	RESERVED	N/A	Reserved.
5	R	RESERVED	N/A	Reserved.
4	R	RESERVED	N/A	Reserved.
3	R/W	PG_%_BUCK_A	1’b0	Set’s buck A’s PG threshold. 1’b0: 5% 1’b1: 7%
2	R/W	PG_%_BUCK_B	1’b0	Set’s buck B’s PG threshold. 1’b0: 5% 1’b1: 7%
1	R/W	PG_%_BUCK_C	1’b0	Set’s buck C’s PG threshold. 1’b0: 5% 1’b1: 7%
0	R	RESERVED	N/A	Reserved.

DISCHARGE_R_REG (0Eh)

Format: Unsigned binary

The DISCHARGE_R_REG command sets each buck’s auto-discharge mode and discharge resistance.

Bits	Access	Bit Name	Default	Description
7	R/W	AUTODIS_1	1’b0	Sets auto-discharge mode for buck A. 1’b 0: No discharge 1’b 1: Discharge
6	R/W	AUTODIS_2	1’b0	Sets auto-discharge mode for buck B. 1’b 0: No Discharge 1’b 1: Discharge

5	R/W	AUTODIS_3	1’b0	Sets auto-discharge mode for buck C. 1’b 0: No Discharge 1’b 1: Discharge
4	R	RESERVED	N/A	Reserved.
3	R/W	DIS_R_1	1’b1	Sets the discharge resistance for buck A. 1’b0: 10Ω 1’b1: 2Ω
2	R/W	DIS_R_2	1’b1	Sets the discharge resistance for buck B. 1’b0: 10Ω 1’b1: 2Ω
1	R/W	DIS_R_3	1’b1	Sets the discharge resistance for buck C. 1’b0: 10Ω 1’b1: 2Ω
0	R	RESERVED	N/A	Reserved.

SW_FREQ_REG (0Fh)

Format: Unsigned binary

The SW_FREQ_REG command sets the frequency for buck A, buck B, and buck C.

Bits	Access	Bit Name	Default	Description
7:6	R/W	BUCK_A_OUTPUT_REGULATOR_SWITCHING_FREQUENCY	2’b10	Sets buck A’s output regulator switching frequency. 2’b00: 500kHz 2’b01: 750kHz 2’b10: 1000kHz 2’b11: 1250kHz
5:4	R/W	BUCK_B_OUTPUT_REGULATOR_SWITCHING_FREQUENCY	2’b10	Sets buck B’s output regulator switching frequency. 2’b00: 500kHz 2’b01: 750kHz 2’b10: 1000kHz 2’b11: 1250kHz
3:2	R/W	BUCK_C_OUTPUT_REGULATOR_SWITCHING_FREQUENCY	2’b10	Sets buck C’s output regulator switching frequency. 2’b00: 500kHz 2’b01: 750kHz 2’b10: 1000kHz 2’b11: 1250kHz
1:0	R	RESERVED	N/A	Reserved.

MONITOR_EN_REG (10h)

Format: Unsigned binary

The MONITOR_EN_REG command enables output voltage/current monitoring.

Bits	Access	Bit Name	Default	Description
7	R/W	MON_V_EN	1’b1	Enables output voltage monitoring. 1’b0: Disable 1’b1: Enable

6:5	R/W	MON_V_SEL	2’b00	Selects which output voltage is monitored. 2’b00: Buck A 2’b01: Buck B 2’b10: Buck C 2’b11: Reserved
4	R/W	MON_IP_SEL	1’b0	Selects whether to monitor each buck’s output current or power. 1’b0: Current 1’b1: Power
3	R/W	MON_TP_SEL	1’b0	Selects whether to monitor buck A’s current or power, or the total power. 1’b0: Buck A’s current or power 1’b1: Total power
2	R/W	MON_I_EN	1’b1	Enables output current monitoring. 1’b0: Disabled 1’b1: Enabled
1	R	RESERVED	N/A	Reserved.
0	R	RESERVED	N/A	Reserved.

SOFT STOP_EN_REG (11h)

Format: Unsigned binary

The SOFT STOP_EN_REG command enables soft stop for buck A, buck B, and buck C.

Bits	Access	Bit Name	Default	Description
7	R/W	SOFT_STOP_BUCK_A	1’b0	Enables soft stop for buck A. 1’b0: Disabled 1’b1: Enabled
6	R/W	SOFT_STOP_BUCK_B	1’b0	Enables soft stop for buck B. 1’b0: Disabled 1’b1: Enabled
5	R/W	SOFT_STOP_BUCK_C	1’b0	Enables soft stop for buck C. 1’b0: Disabled 1’b1: Enabled
4:0	R	RESERVED	N/A	Reserved.

SOFT_STOP_REG (12h)

Format: Unsigned binary

The SOFT_STOP_REG command sets buck A, buck B, and buck C’s soft-stop time.

Bits	Access	Bit Name	Default	Description
7:6	R/W	SOFT_STOP_TIME_ BUCK_A	2’b01	Sets buck A’s soft-stop time. 2’b00: 0.5ms 2’b01: 1ms 2’b10: 2ms 2’b11: 4ms

5:4	R/W	SOFT_STOP_TIME_BUCK_B	2'b01	Sets buck B's soft-stop time. 2'b00: 0.5ms 2'b01: 1ms 2'b10: 2ms 2'b11: 4ms
3:2	R/W	SOFT_STOP_TIME_BUCK_C	2'b01	Sets buck C's soft-stop time. 2'b00: 0.5ms 2'b01: 1ms 2'b10: 2ms 2'b11: 4ms
1:0	R	RESERVED	N/A	Reserved.

SOFT_START_REG (13h)

Format: Unsigned binary

The SOFT_START_REG command sets buck A, buck B, and buck C's soft-start time.

Bits	Access	Bit Name	Default	Description
7:6	R/W	SOFT_START_TIME_BUCK_A	2'b01	Sets buck A's soft-start time. 2'b00: 0.5ms 2'b01: 1ms 2'b10: 1.5ms 2'b11: 2ms
5:4	R/W	SOFT_START_TIME_BUCK_B	2'b01	Sets buck B's soft-start time. 2'b00: 0.5ms 2'b01: 1ms 2'b10: 1.5ms 2'b11: 2ms
3:2	R/W	SOFT_START_TIME_BUCK_C	2'b01	Sets buck C's soft-start time. 2'b00: 0.5ms 2'b01: 1ms 2'b10: 1.5ms 2'b11: 2ms
1:0	R	RESERVED	N/A	Reserved.

PROTECT_REG (14h)

Format: Unsigned binary

The PROTECT_REG command sets protection functions, as well as the phase regulator mode for buck A and buck B.

Bits	Access	Bit Name	Default	Description
7	R	RESERVED	N/A	Reserved.
6	R/W	MTP_W	1'b0	Enables MTP writing. 1'b0: Disabled 1'b1: Enabled
5	R/W	BUCK_A/B_DUAL_EN	1'b0	Selects buck A and buck B's phase regulator mode. 1'b0: Single-phase regulator 1'b1: Dual-phase regulator
4:0	R	RESERVED	N/A	Reserved.

BUCK_A_VOUT (15h)

Format: Direct

The BUCK_A_VOUT command sets buck A's output voltage.

Bits	Access	Bit Name	Default	Description
7:0	R/W	BUCK_A_VOUT_ SETTING	0x8C	Sets buck A's output voltage setting. The V_{OUT} slew rate is 1mV/µs. If VOUT_RANGE_SELECT (25h), bit[3] = 0: buck A's output dynamic voltage scaling (DVS) range is between 0.4V and 1.2V 0x00: 0.4V 0x01: 0.41V 0x02: 0.42V 0x03: 0.43V … 0x4D: 1.17V 0x4E: 1.18V 0x4F: 1.19V 0x50: 1.2V Others: Reserved (0x51~0xFF) If VOUT_RANGE_SELECT (25h), bit[3] = 1: buck A's output DVS range is between 1.2V and 3.6V 0x00: 1.2V 0x01: 1.215V 0x02: 1.23V 0x03: 1.245V … 0x8C: 3.3V 0x8D: 3.315V 0x8E: 3.33V … 0x9F: 3.585V 0xA0: 3.6V Others: Reserved (0xA1~0xFF)

BUCK_B_VOUT (16h)

Format: Direct

The BUCK_B_VOUT command sets buck B's output voltage.

Bits	Access	Bit Name	Default	Description
7:0	R/W	BUCK_B_VOUT_ SETTING	0x8C	Sets buck B's output voltage setting. The V_{OUT} slew rate is 1mV/µs. If VOUT_RANGE_SELECT (25h), bit[2] = 0: buck B's output dynamic voltage scaling (DVS) range is between 0.4V and 1.2V 0x00: 0.4V 0x01: 0.41V 0x02: 0.42V 0x03: 0.43V … 0x4D: 1.17V 0x4E: 1.18V 0x4F: 1.19V 0x50: 1.2V Others: Reserved (0x51~0xFF) If VOUT_RANGE_SELECT (25h), bit[2] = 1: buck B's output DVS range is between 1.2V and 3.6V 0x00: 1.2V 0x01: 1.215V 0x02: 1.23V 0x03: 1.245V … 0x8C: 3.3V 0x8D: 3.315V 0x8E: 3.33V … 0x9F: 3.585V 0xA0: 3.6V Others: Reserved (0xA1~0xFF)

BUCK_C_VOUT (17h)

Format: Direct

The BUCK_C_VOUT command sets buck C's output voltage.

Bits	Access	Bit Name	Default	Description
7:0	R/W	BUCK_C_VOUT_ SETTING	0x8C	Sets buck C's output voltage setting. The V_{OUT} slew rate is 1mV/µs. If VOUT_RANGE_SELECT (25h), bit[1] = 0: buck C's output dynamic voltage scaling (DVS) range is between 0.4V and 1.2V 0x00: 0.4V 0x01: 0.41V 0x02: 0.42V 0x03: 0.43V … 0x4D: 1.17V 0x4E: 1.18V 0x4F: 1.19V 0x50: 1.2V Others: Reserved (0x51~0xFF) If VOUT_RANGE_SELECT (25h), bit[1] = 1: buck C's output DVS range is between 1.2V and 3.6V. 0x00: 1.2V 0x01: 1.215V 0x02: 1.23V 0x03: 1.245V … 0x8C: 3.3V 0x8D: 3.315V 0x8E: 3.33V … 0x9F: 3.585V 0xA0: 3.6V Others: Reserved (0xA1~0xFF)

PON_CONFIG_0 (19h)

Format: Unsigned binary

The PON_CONFIG_0 command sets the Config0 power-on sequence.

Bits	Access	Bit Name	Default	Description
7	R/W	PON_SEQ_CONFIG0	1'b1	Executes the power-on sequence for Config0. 1'b0: Do not execute Config0 1'b1: Execute Config0
6	R/W	PON_SEQ_CONFIG0_ BUCK_A	1'b1	Enables buck A's output regulator. 1'b0: Disabled 1'b1: Enabled
5	R/W	PON_SEQ_CONFIG0_ BUCK_B	1'b1	Enables buck B's output regulator. 1'b0: Disabled 1'b1: Enabled
4	R/W	PON_SEQ_CONFIG0_ BUCK_C	1'b1	Enables buck C's output regulator. 1'b0: Disabled 1'b1: Enabled
3:0	R	RESERVED	N/A	Reserved.

PON_CONFIG_1 (1Ah)

Format: Unsigned binary

The PON_CONFIG_1 command sets the Config1 power-on sequence.

Bits	Access	Bit Name	Default	Description
7	R/W	PON_SEQ_CONFIG1	1'b0	Executes the power-on sequence for Config1. 1'b0: Do not execute Config1 1'b1: Execute Config1
6	R/W	PON_SEQ_CONFIG1_ BUCK_A	1'b0	Enables buck A's output regulator. 1'b0: Disabled 1'b1: Enabled
5	R/W	PON_SEQ_CONFIG1_ BUCK_B	1'b0	Enables buck B's output regulator. 1'b0: Disabled 1'b1: Enabled
4	R/W	PON_SEQ_CONFIG1_ BUCK_C	1'b0	Enables buck C's output regulator. 1'b0: Disabled 1'b1: Enabled
3:0	R	RESERVED	N/A	Reserved.

PON_CONFIG_2 (1Bh)

Format: Unsigned binary

The PON_CONFIG_2 command sets the Config2 power-on sequence.

Bits	Access	Bit Name	Default	Description
7	R/W	PON_SEQ_CONFIG2	1'b0	Executes the power-on sequence for Config2. 1'b0: Do not execute Config2 1'b1: Execute Config2
6	R/W	PON_SEQ_CONFIG2_ BUCK_A	1'b0	Enables buck A's output regulator. 1'b0: Disabled 1'b1: Enabled
5	R/W	PON_SEQ_CONFIG2_ BUCK_B	1'b0	Enables buck B's output regulator. 1'b0: Disabled 1'b1: Enabled
4	R/W	PON_SEQ_CONFIG2_ BUCK_C	1'b0	Enables buck C's output regulator. 1'b0: Disabled 1'b1: Enabled
3:0	R	RESERVED	N/A	Reserved.

PON_CONFIG_3 (1Ch)

Format: Unsigned binary

The PON_CONFIG_3 command sets the Config3 power-on sequence.

Bits	Access	Bit Name	Default	Description
7	R/W	PON_SEQ_CONFIG3	1'b0	Executes the power-on sequence for Config3. 1'b0: Do not execute Config3 1'b1: Execute Config3

6	R/W	PON_SEQ_CONFIG3_ BUCK_A	1’b0	Enables buck A’s output regulator. 1’b0: Disabled 1’b1: Enabled
5	R/W	PON_SEQ_CONFIG3_ BUCK_B	1’b0	Enables buck B’s output regulator. 1’b0: Disabled 1’b1: Enabled
4	R/W	PON_SEQ_CONFIG3_ BUCK_C	1’b0	Enables buck C’s output regulator. 1’b0: Disabled 1’b1: Enabled
3:0	R	RESERVED	N/A	Reserved.

PON_OFF_DELAY0 (0x1D)

Format: Unsigned binary

The PON_OFF_DELAY0 command sets power-on/-off delay 0.

Bits	Access	Bit Name	Default	Description
7	R	RESERVED	N/A	Reserved.
6:4	R/W	PON_SEQ_DELAY0	3’b000	Power on delay 0 defines the time from when V_{IN} meets the UVLO rising threshold or EN goes high to when the first channel starts rising. 3’b000: 0ms 3’b001: 1ms 3’b010: 2ms 3’b011: 3ms 3’b100: 4ms 3’b101: 5ms 3’b110: 8ms 3’b111: 10ms
3	R	RESERVED	N/A	Reserved.
2:0	R/W	POFF_SEQ_DELAY0	3’b000	Power off delay 0 defines the time from when V_{IN} meets the UVLO falling threshold or EN goes low to when the first channel starts falling. 3’b000: 0ms 3’b001: 1ms 3’b010: 2ms 3’b011: 4ms 3’b100: 6ms Others: Reserved

PON_SEQ_DELAY_1_2 (1Eh)

Format: Unsigned binary

The PON_SEQ_DELAY_1_2 command sets the power-on sequence for delay 1 and delay 2.

Bits	Access	Bit Name	Default	Description
7:4	R/W	PON_SEQ_DELAY1	4'b0000	Sets the power-on sequence for delay 1. 4'b0000: 0ms 4'b0001: 1ms 4'b0010: 2ms 4'b0011: 3ms 4'b0100: 4ms 4'b0101: 5ms 4'b0110: 6ms 4'b0111: 7ms 4'b1000: 8ms 4'b1001: 9ms 4'b1010: 10ms Others: Reserved
3:0	R/W	PON_SEQ_DELAY2	4'b0000	Sets the power-on sequence for delay 2. 4'b0000: 0ms 4'b0001: 1ms 4'b0010: 2ms 4'b0011: 3ms 4'b0100: 4ms 4'b0101: 5ms 4'b0110: 6ms 4'b0111: 7ms 4'b1000: 8ms 4'b1001: 9ms 4'b1010: 10ms Others: Reserved

PON_SEQ_DELAY_3_PG (1Fh)

Format: Unsigned binary

The PON_SEQ_DELAY_3_PG command sets the power-on sequence for delay 3 and the PG delay.

Bits	Access	Bit Name	Default	Description
7:4	R/W	PON_SEQ_DELAY3	4'b0000	Sets the power-on sequence for delay 3. 4'b0000: 0ms 4'b0001: 1ms 4'b0010: 2ms 4'b0011: 3ms 4'b0100: 4ms 4'b0101: 5ms 4'b0110: 6ms 4'b0111: 7ms 4'b1000: 8ms 4'b1001: 9ms 4'b1010: 10ms Others: Reserved

3:0	R/W	PON_SEQ_DELAY_PG	4’b0000	Sets the power-on sequence for the PG delay. 4’b0000: 0ms 4’b0001: 1ms 4’b0010: 2ms 4’b0011: 3ms 4’b0100: 4ms 4’b0101: 5ms 4’b0110: 6ms 4’b0111: 7ms 4’b1000: 8ms 4’b1001: 9ms 4’b1010: 10ms Others: Reserved

POFF_SEQ_CONFIG_0 (20h)

Format: Unsigned binary

The POFF_SEQ_CONFIG_0 command sets the Config0 power-off sequence.

Bits	Access	Bit Name	Default	Description
7	R/W	POFF_SEQ_CONFIG0	1’b1	Executes the power-off sequence for Config0. 1’b0: Do not execute Config0 1’b1: Execute Config0
6	R/W	POFF_SEQ_CONFIG0_BUCK_A	1’b1	Disables buck A’s output regulator. 1’b0: Enabled 1’b1: Disabled
5	R/W	POFF_SEQ_CONFIG0_BUCK_B	1’b1	Disables buck B’s output regulator. 1’b0: Enabled 1’b1: Disabled
4	R/W	POFF_SEQ_CONFIG0_BUCK_C	1’b1	Disables buck C’s output regulator. 1’b0: Enabled 1’b1: Disabled
3	R	RESERVED	N/A	Reserved.
2:0	R/W	POFF_SEQ_DELAY1	3’b000	Sets power delay 1. 3’b000: 0ms 3’b001: 1ms 3’b010: 2ms 3’b011: 4ms 3’b100: 6ms Others: Reserved

POFF_SEQ_CONFIG_1 (21h)

Format: Unsigned binary

The POFF_SEQ_CONFIG_1 command sets the Config1 power-off sequence.

Bits	Access	Bit Name	Default	Description
7	R/W	POFF_SEQ_CONFIG1	1’b0	Executes the power-off sequence for Config1. 1’b0: Do not execute Config1 1’b1: Execute Config1
6	R/W	POFF_SEQ_CONFIG1_BUCK_A	1’b1	Disables buck A’s output regulator. 1’b0: Enabled 1’b1: Disabled

5	R/W	POFF_SEQ_CONFIG1_BUCK_B	1'b1	Disables buck B's output regulator. 1'b0: Enabled 1'b1: Disabled
4	R/W	POFF_SEQ_CONFIG1_BUCK_C	1'b1	Disables buck C's output regulator. 1'b0: Enabled 1'b1: Disabled
3	R	RESERVED	N/A	Reserved.
2:0	R/W	POFF_SEQ_DELAY2	3'b000	Sets power delay 2. 3'b000: 0ms 3'b001: 1ms 3'b010: 2ms 3'b011: 4ms 3'b100: 6ms Others: Reserved

POFF_SEQ_CONFIG_2 (22h)

Format: Unsigned binary

The POFF_SEQ_CONFIG_2 command sets the Config2 power-off sequence.

Bits	Access	Bit Name	Default	Description
7	R/W	POFF_SEQ_CONFIG2	1'b0	Executes the power-off sequence for Config2. 1'b0: Do not execute Config2 1'b1: Execute Config2
6	R/W	POFF_SEQ_CONFIG2_BUCK_A	1'b1	Disables buck A's output regulator. 1'b0: Enabled 1'b1: Disabled
5	R/W	POFF_SEQ_CONFIG2_BUCK_B	1'b1	Disables buck B's output regulator. 1'b0: Enabled 1'b1: Disabled
4	R/W	POFF_SEQ_CONFIG2_BUCK_C	1'b1	Disables buck C's output regulator. 1'b0: Enabled 1'b1: Disabled
3	R	RESERVED	N/A	Reserved.
2:0	R/W	POFF_SEQ_DELAY3	3'b000	Sets power delay 3. 3'b000: 0ms 3'b001: 1ms 3'b010: 2ms 3'b011: 4ms 3'b100: 6ms Others: Reserved

POFF_SEQ_CONFIG_3 (23h)

Format: Unsigned binary

The POFF_SEQ_CONFIG_3 command sets the Config3 power-off sequence.

Bits	Access	Bit Name	Default	Description
7	R/W	POFF_SEQ_CONFIG3	1'b0	Executes the power-off sequence for Config3. 1'b0: Do Not Execute Config3 1'b1: Execute Config3

6	R/W	POFF_SEQ_CONFIG3_ BUCK_A	1'b1	Disables buck A's output regulator. 1'b0: Enabled 1'b1: Disabled
5	R/W	POFF_SEQ_CONFIG3_ BUCK_B	1'b1	Disables buck B's output regulator. 1'b0: Enabled 1'b1: Disabled
4	R/W	POFF_SEQ_CONFIG3_ BUCK_C	1'b1	Disables buck C's output regulator. 1'b0: Enabled 1'b1: Disabled
3:0	R	RESERVED	N/A	Reserved.

ADC_TEMP (24h)

Format: Unsigned binary

The ADC_TEMP command monitors the IC's junction temperature (T_J).

Bits	Access	Bit Name	Description
7:5	R	ADC_TEMP_READOUT	Measures T_J. 3'b000: <85°C 3'b001: 85°C to 95°C 3'b010: 95°C to 105°C 3'b011: 105°C to 115°C 3'b100: 115°C to 125°C 3'b101: 125°C to 135°C 3'b110: 135°C to 145°C 3'b111: >145°C
4:0	R/W	RESERVED	Reserved.

VOUT_RANGE_SELECT (25h)

Format: Unsigned binary

The VOUT_RANGE_SELECT command sets the output voltage range for buck A, buck B, and buck C.

Bits	Access	Bit Name	Default	Description
7:4	R	RESERVED	N/A	Reserved.
3	R/W	BUCK_A_VOUT_ RANGE_SELECT	1'b1	Sets buck A's output voltage range. 1'b0: 0.4V to 1.2V with 10mV/step 1'b1: 1.2V to 3.6V with 15mV/step
2	R/W	BUCK_B_VOUT_ RANGE_SELECT	1'b1	Sets buck B's output voltage range. 1'b0: 0.4V to 1.2V with 10mV/step 1'b1: 1.2V to 3.6V with 15mV/step
1	R/W	BUCK_C_VOUT_ RANGE_SELECT	1'b1	Sets buck C's output voltage range. 1'b0: 0.4V to 1.2V with 10mV/step 1'b1: 1.2V to 3.6V with 15mV/step
0	R	RESERVED	N/A	Reserved.

OC_STATUS_CLEAR (2Ah)

Format: Unsigned binary

The OC_STATUS_CLEAR command monitors over-current (OC) statuses and clears certain register.

Bits	Access	Bit Name	Default	Description
7	R/W	CLEAR_BUCK_A_OC_STATUS	1'b0	1'b1: Clears OC_STATUS_CLEAR (2Ah), bit[3]
6	R/W	CLEAR_BUCK_B_OC_STATUS	1'b0	1'b1: Clears OC_STATUS_CLEAR (2Ah), bit[2]
5	R/W	CLEAR_BUCK_C_OC_STATUS	1'b0	1'b1: Clears OC_STATUS_CLEAR (2Ah), bit[1]
4	R	RESERVED	N/A	Reserved.
3	R	BUCK_A_OC_STATUS	1'b0	1'b0: No output OC condition on buck A 1'b1: There is an output OC condition on buck A
2	R	BUCK_B_OC_STATUS	1'b0	1'b0: No output OC condition on buck B 1'b1: There is an output OC condition on buck B
1	R	BUCK_C_OC_STATUS	1'b0	1'b0: No output OC condition on buck C 1'b1: There is an output OC condition on buck C
0	R	RESERVED	N/A	Reserved.

MTP_AUTO_REG (30h)

Format: Unsigned binary

The MTP_AUTO_REG command controls the MTP auto-write functions.

Bits	Access	Bit Name	Default	Description
7	R/W	MTP_AUTO_WRITE	1'b0	1'b0 to 1'b1: MTP auto-write bit
6	R	MTP_WRITE_DONE	1'b0	1'b0 to 1'b1: MTP is finished
5:0	R	RESERVED	N/A	Reserved.

Follow the steps below for MTP write operation:

1. Configure all MTP registers.
2. Write PROTECT_REG (14h), bit[6] from 0 to 1. This disables write protection.
3. Ensure that the buck is off before MTP configurations. It is recommended to pull down the external EN pin.
4. Write MTP_AUTO_REG (30h), bit[7] from 0 to 1 for MTP auto-writing.
5. Wait about 2s.
6. Read register MTP_AUTO_REG (30h). If MTP_AUTO_REG (30h) = 0x5A, then MTP configuring is complete.

PART_ID (31h)

Format: Unsigned binary

The PART_ID command sets the part's ID number.

Bits	Access	Bit Name	Default	Description
7:0	R	PART_ID	0x13	Returns the device's ID number.

CODE_ID (35h)

Format: Unsigned binary

The CODE_ID command sets the code ID number.

Bits	Access	Bit Name	Default	Description
7:0	R	CODE ID	0x00	Sets the code ID number.

CODE_VERSION (36h)

Format: Unsigned binary

The CODE_VERSION command sets the code version number.

Bits	Access	Bit Name	Default	Description
7:0	R	CODE_VERSION	0x00	Sets the code version number.

ACTIVE_POSITION_ENABLE_A/B (71h)

Format: Unsigned binary

The ACTIVE_POSITION_ENABLE_A/B command enables active voltage positioning (AVP) for buck A and buck B.

Bits	Access	Bit Name	Default	Description
7	R/W	AVP_EN_A/B	1’b1	Enables AVP for buck A and buck B. 1’b0: Disabled 1’b1: Enabled
6:0	R	RESERVED	N/A	Reserved.

To operate registers 0x71, 0x73, and 0x79, a password should be written to the device by following the steps below:

1. Write register 0xC1 = 95h.
2. Write register 0xC1 = 63h.

To write the register into flash, follow the steps below:

1. Configure registers 0x71, 0x73, and 0x79.
2. Write register 0x87 = 80h.
3. Wait about 1s then read register 0x87. If register 0x87 = 00h, the operation has been successful; otherwise, it has failed.

For more details on the other commands, see the I2C_ADDRESS (73h) section below, as well as the ACTIVE_POSITION_ENABLE_C (79h) section on page 41.

I2C_ADDRESS (73h)

Format: Unsigned binary

The I2C_ADDRESS command sets the I²C address.

Bits	Access	Bit Name	Default	Description
7:4	R	RESERVED	N/A	Reserved.
3:1	R/W	ADDRESS_BITS	3’b 000	Bits[3:1] of this command define bits[6:4] of the I²C address. The I²C address can be modified via the MTP. The I²C address changes after the next power on cycle.
0	R	RESERVED	N/A	Reserved.

ACTIVE_POSITION_ENABLE_C (79h)

Format: Unsigned binary

The ACTIVE_POSITION_ENABLE_C command enables AVP for buck C.

Bits	Access	Bit Name	Default	Description
7	RW	AVP_EN_C	1'b1	Enables AVP for buck C. 1'b0: Disabled 1'b1: Enabled
6:0	R	RESERVED	N/A	Reserved.

VIN_OV_REG (90h)

Format: Unsigned binary

The VIN_OV_REG command sets V_{IN} under-voltage lockout (UVLO) hysteresis and enables V_{IN} over-voltage protection (OVP).

Bits	Access	Bit Name	Default	Description
7:2	R	RESERVED	N/A	Reserved.
1	R/W	VIN_UVLO_ HYSTERESIS	1'b0	Selects V_{IN} UVLO hysteresis. 1'b0: 0.125V 1'b1: 0.25V
0	R/W	VIN_OVP	1'b0	Enables V_{IN} OVP. 1'b0: Disabled 1'b1: Enabled

VIN_UVLO_REG (AFh)

Format: Unsigned binary

The VIN_UVLO_REG command sets the V_{IN} under-voltage lockout (UVLO) threshold.

Bits	Access	Bit Name	Default	Description
7:2	R	RESERVED	N/A	Reserved.
1:0	R/W	VIN_UVLO	2'b00	Selects the V_{IN} UVLO threshold. 00: 3V 01: 3.5V 10: 3.75V 11: 4V

APPLICATION INFORMATION

Setting the Output Voltage (V_{OUT}) with an External Divider

An external resistor divider can set the MPM54313's V_{OUT} (see Figure 11). Consider the tradeoff between stability and dynamics to choose a feedback resistor (R1) that has an appropriate resistance. V_{FB} is determined by VOUT_RANGE_SELECT (25h), BUCK_A_VOUT (15h) for buck A, BUCK_B_VOUT (16h) for buck B, and BUCK_C_VOUT (17h) for buck C.

To enable all channels with an external divider, set VOUT_RANGE_SELECT (25h) = 00h. The ADC reads back V_{FB} rather than the actual voltage.

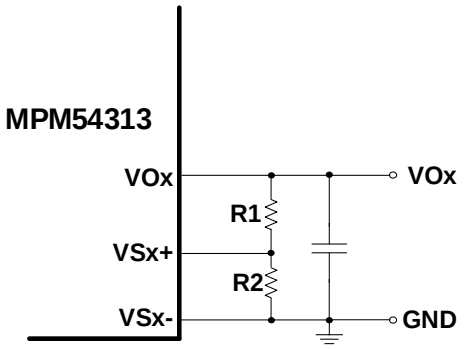


Figure 11: Feedback Network

R2 can be calculated with Equation (3):

$$R2 = \frac{R1}{\frac{V_{OUT}}{V_{REF}} - 1} \quad (3)$$

Table 2 lists the recommended resistor values for common output voltages if VOUT_RANGE_SELECT (25h) = 00h, and BUCK_A_VOUT (15h), BUCK_B_VOUT (16h), or BUCK_C_VOUT (17h) = 14h (0.6V).

Table 2: Resistor Values for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1	10	15
1.2	10	10
1.8	10	5
2.5	10	3.15
3.3	10	2.2
5.5	10	1.23

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and therefore requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. Use low-ESR capacitors for the best performance. Use ceramic capacitors with X5R or X7R dielectrics for the best results because of their low ESR and small temperature coefficients. For most applications, use a 22µF capacitor.

Since C1 absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (4):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (4)$$

The worst-case condition occurs at $V_{IN} = 2 \times V_{OUT}$, calculated with Equation (5):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (5)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1µF), placed as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated with Equation (6):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (6)$$

Selecting the Step-Down Regulator's Output Capacitor

The output capacitor for the step-down regulator maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For the best results, use low-ESR capacitors to keep the output voltage ripple low.

The output voltage ripple can be calculated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C2}\right) \quad (7)$$

Where L_1 is the inductance and R_{ESR} is the output capacitor's equivalent series resistance (ESR).

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be calculated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (9)$$

The characteristics of the output capacitor also affect the stability of the regulation.

PCB Layout Guidelines

For the best results, refer to Figure 12 and follow the guidelines below:

1. Keep the power loop as small as possible.
2. Use a large ground plane to connect directly to PGND.
3. Place a sufficient ceramic input capacitor as close to the device as possible.
4. Place the VCC capacitor as close to the VCC and GND pins as possible.
5. Connect VIN, VOUT, and GND to a large copper area to improve thermal performance and long-term reliability.
6. Separate the input GND area from other GND areas on the top layer.
7. Connect the GND areas together on the internal layers and connect the bottom layer through multiple vias to minimize noise.

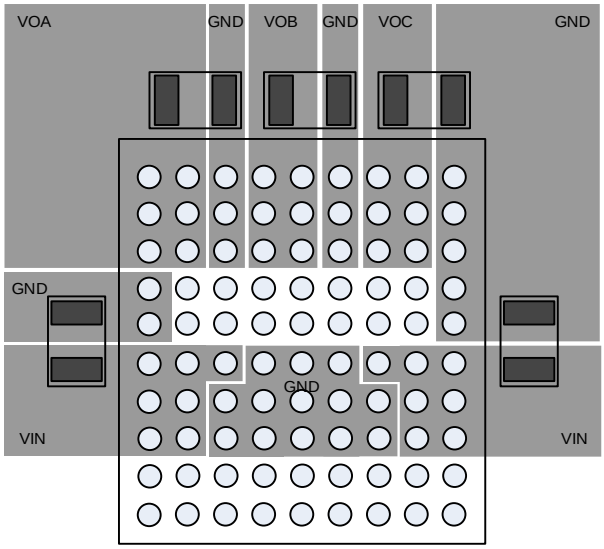


Figure 12: Recommended PCB Layout

MTP CONFIGURATION

Table 3: 0000 Suffix Code Configuration

Items	VOA	VOB	VOC
Output voltage	3.3V	3.3V	3.3V
Mode	FCCM	FCCM	FCCM
I²C address bits[4:6]	000		
Soft start time	1ms	1ms	1ms
Soft-stop time EN/Disable	Disabled	Disabled	Disabled
Soft-stop time	N/A	N/A	N/A
Switching frequency	1000kHz	1000kHz	1000kHz
Buck output discharge enable	Disabled	Disabled	Disabled
Buck output discharge resistor	N/A	N/A	N/A
PG threshold	95%	95%	95%
VOA and VOB active interleaved or not	Disabled		
VOA start-up delay time 0	0ms		
VOB start-up delay time 1	0ms		
VOC start-up delay time 2	0ms		
VOD start-up delay time 3	0ms		
PG start-up delay time 4	0ms		
VOA off delay time 0	0ms		
VOB off delay time 1	0ms		
VOC off delay time 2	0ms		
VOD off delay time 3	0ms		
Load-line function enable	Enabled		
Current monitoring enable	Enabled		
Voltage monitoring enable	Enabled		
Load-line	40mV/A		

Table 4: 0000 Suffix Code Register Value

Register	Hex Value	Register	Hex Value	Register	Hex Value
09h	0x00	14h	0x00	20h	0xF8
0Ah	0x00	15h	0x8C	21h	0x78
0Bh	0xB0	16h	0x8C	22h	0x78
0Ch	0x00	17h	0x8C	23h	0x78
0Dh	0x00	19h	0xF0	25h	0x0E
0Eh	0x1F	1Ah	0x00	35h	0x00
0Fh	0xAA	1Bh	0x00	36h	0x00
10h	0x84	1Ch	0x00	71h	0x80
11h	0x00	1Dh	0x00	73h	0x00
12h	0x55	1Eh	0x00	79h	0x80
13h	0x55	1Fh	0x00	-	-

TYPICAL APPLICATION CIRCUITS

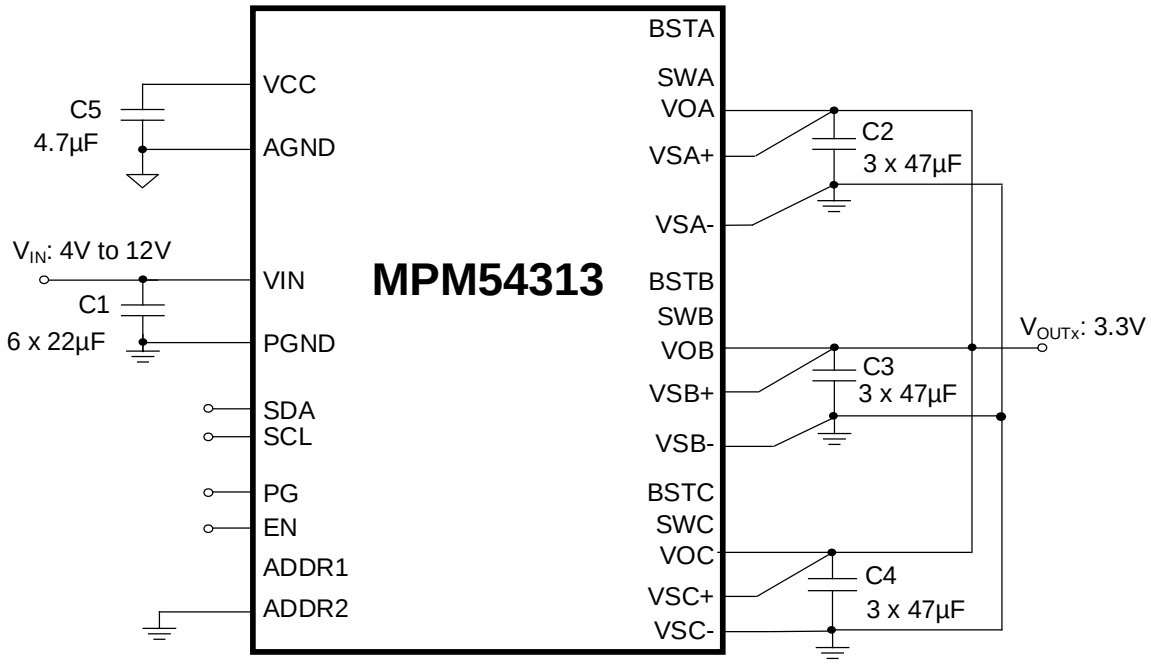


Figure 13: Typical Application Circuit (4V to 16V Input and 3-Phase Paralleled Output with Internal Divider)

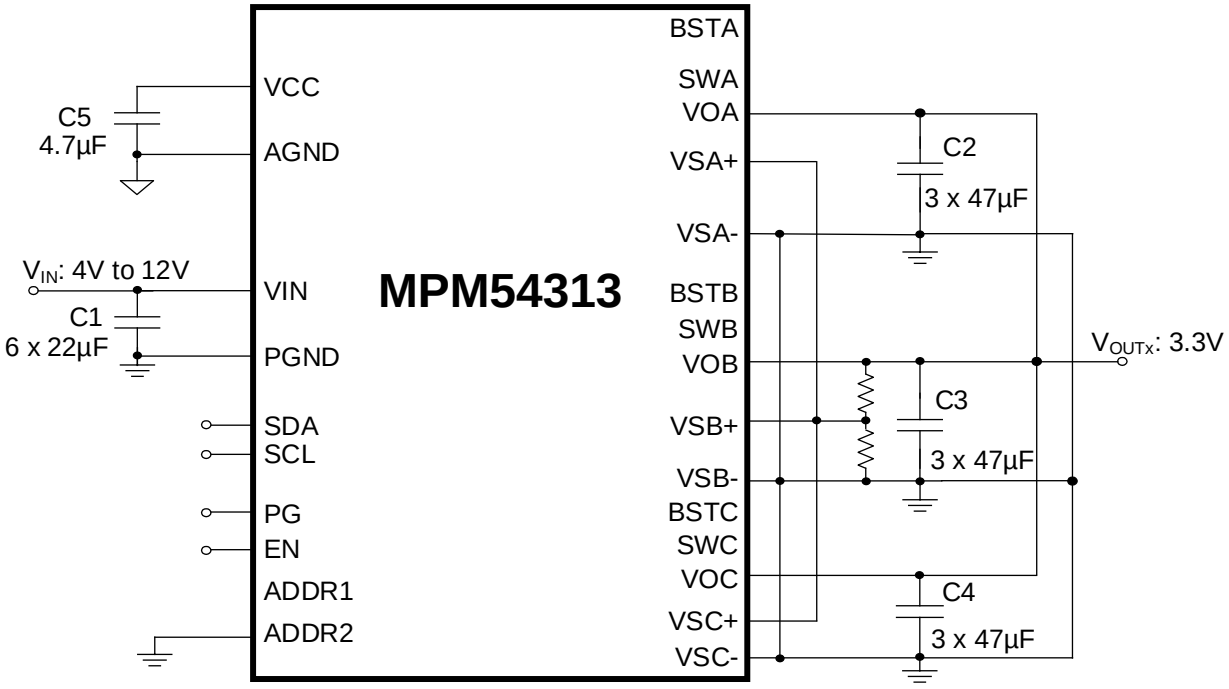


Figure 14: Typical Application Circuit (4V to 16V Input and 3-Phase Paralleled Output with External Divider)

TYPICAL APPLICATION CIRCUITS *(continued)*

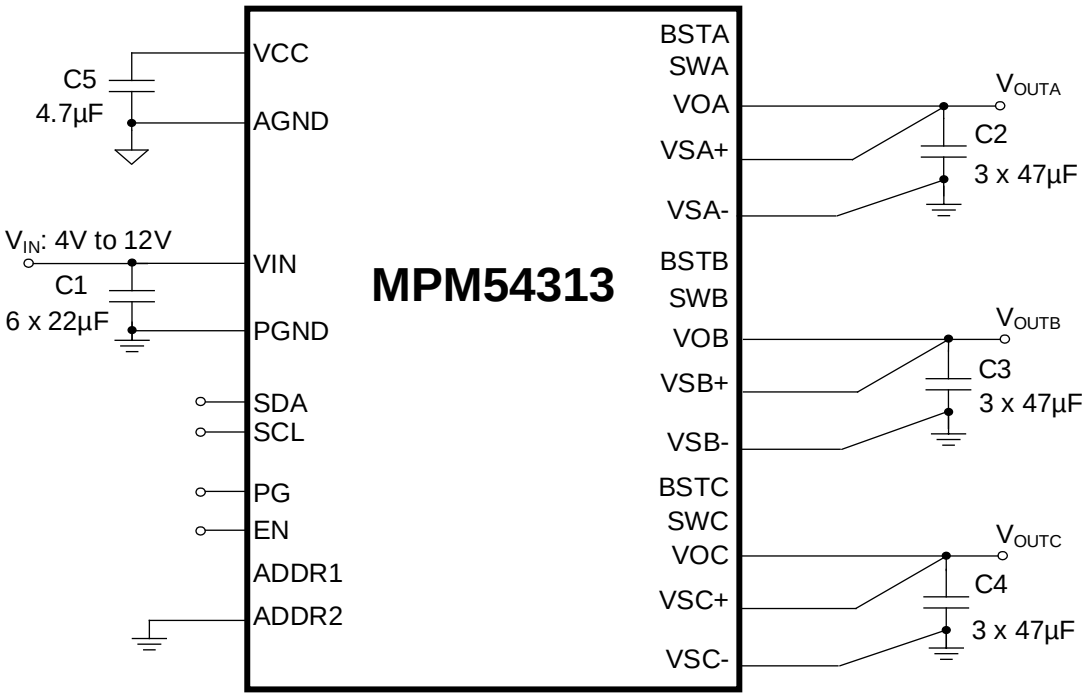


Figure 15: Typical Application Circuit (4V to 16V Input and Triple Outputs with Internal Divider)

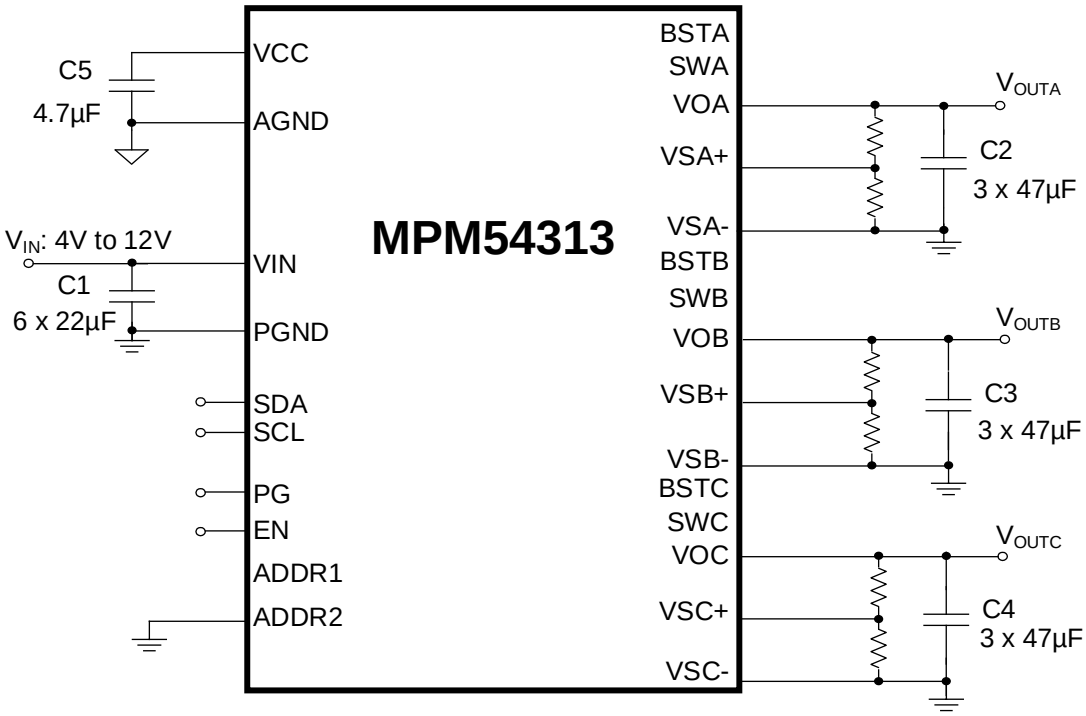
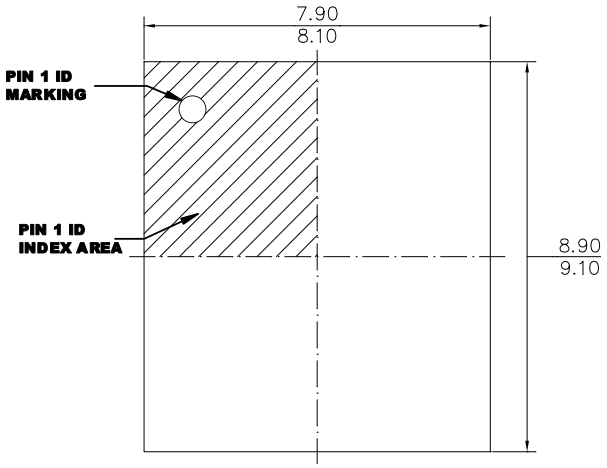


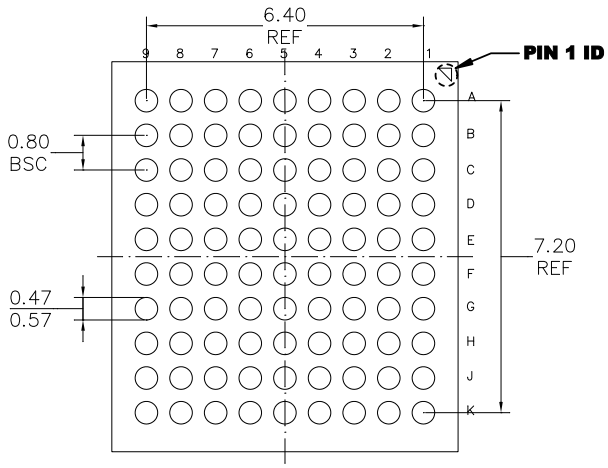
Figure 16: Typical Application Circuit (4V to 16V Input and Triple Outputs with External Divider)

PACKAGE INFORMATION

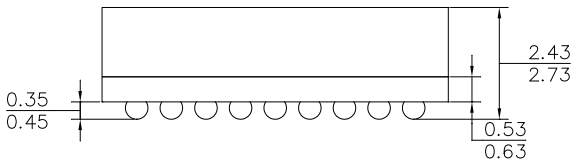
BGA (8mmx9mmx2.58mm)



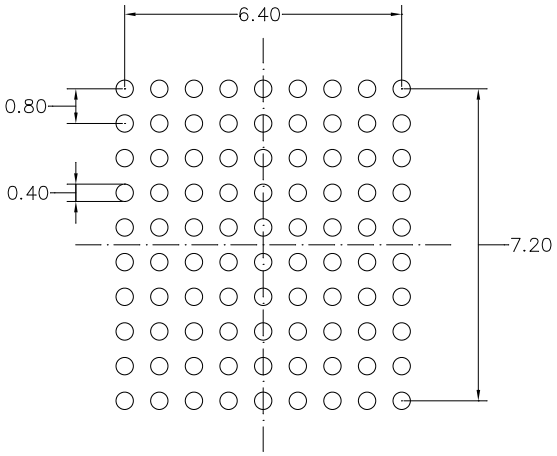
TOP VIEW



BOTTOM VIEW



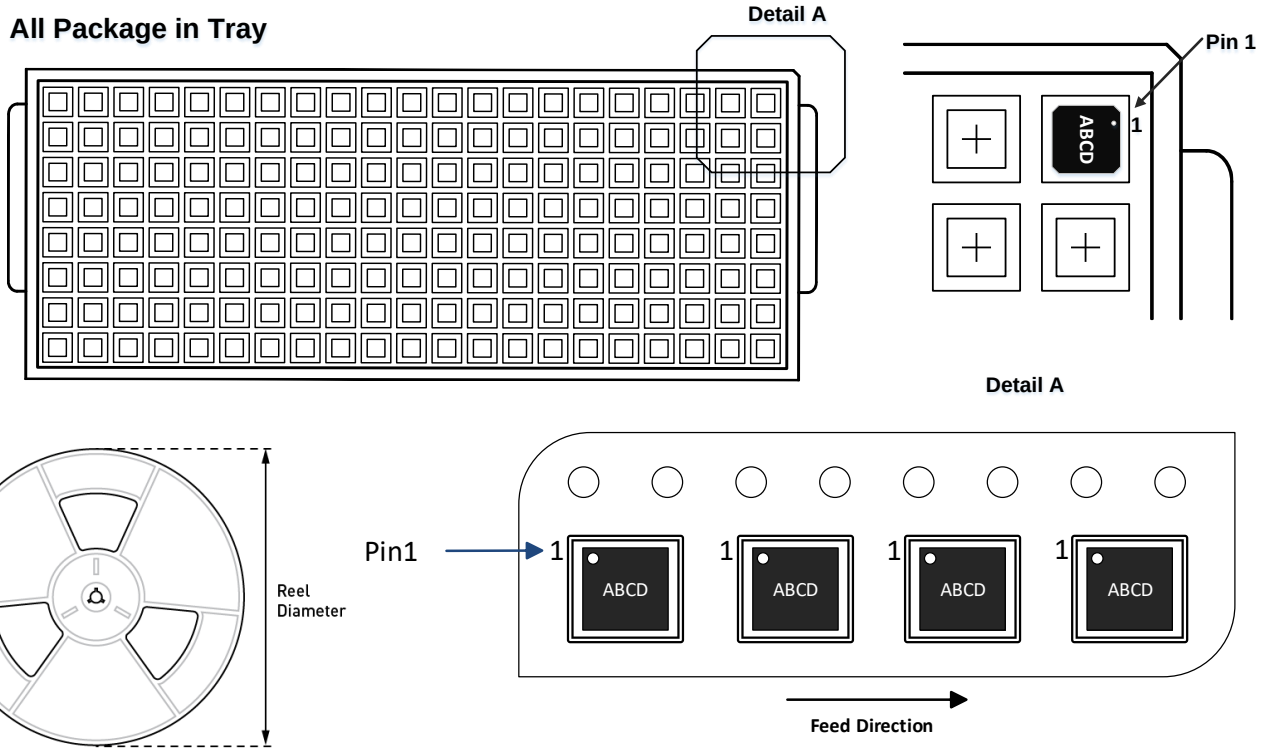
SIDE VIEW



NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-275A.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION (12) (13)



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPM54313GBJ-xxxx-T	BGA (8mmx9mmx 2.58mm)	N/A	N/A	275	N/A	N/A	N/A
MPM54313GBJ-xxxx-Z	BGA (8mmx9mmx 2.58mm)	1000	N/A	N/A	13in	16mm	12mm

Notes:

12) The top image is a schematic diagram of the tray. Different packages correspond to different trays with different lengths, widths and heights.
13) The bottom image is a schematic diagram of a reel. Different packages correspond to different reels with different lengths, widths, and heights.

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	5/7/2024	Initial Release	-