IPS1050LQ

Datasheet

Single channel low side switch with configurable smart overload protection

Features

- Smart overload protection with configurable inrush and limitation levels
- Fast demagnetization of inductive loads
- Junction over-temperature protections
- Over-temperature diagnostic pin
- Designed to drive DC-13 loads according to EN 60947-5-1
- Designed to meet IEC 61000-4-2, IEC 61000-4-4, IEC 61000-4-5
- Package QFN32L 6x6 mm

Typical Applications

- Programmable logic control
- Industrial PC peripheral input/output
- Numerical control machines
- General Low-Side Switch Applications

Product status link

IPS1050LQ

Product label

SUSTAINABLE TECHNOLOGY

Description

The IPS1050LQ is a single low side switch IC, with 65 V absolute maximum rating on the output stage, able to drive capacitive, resistive, or inductive loads with one side connect to supply rail.

The very low $R_{DS\text{-}ON}$ (≤ 50 mΩ) and the smart overload protection based on the configuration of the pins I_{PDX}, make the IC suitable for the for applications requiring high inrush current (up to 25 A) and with different configurable steady state operating current.

The level of inrush current can be modified setting high/low the I_{PDX} pins or automatically reduced by the IC itself when the internal timer (regulated by capacitors on I_{PDX} pins) elapses.

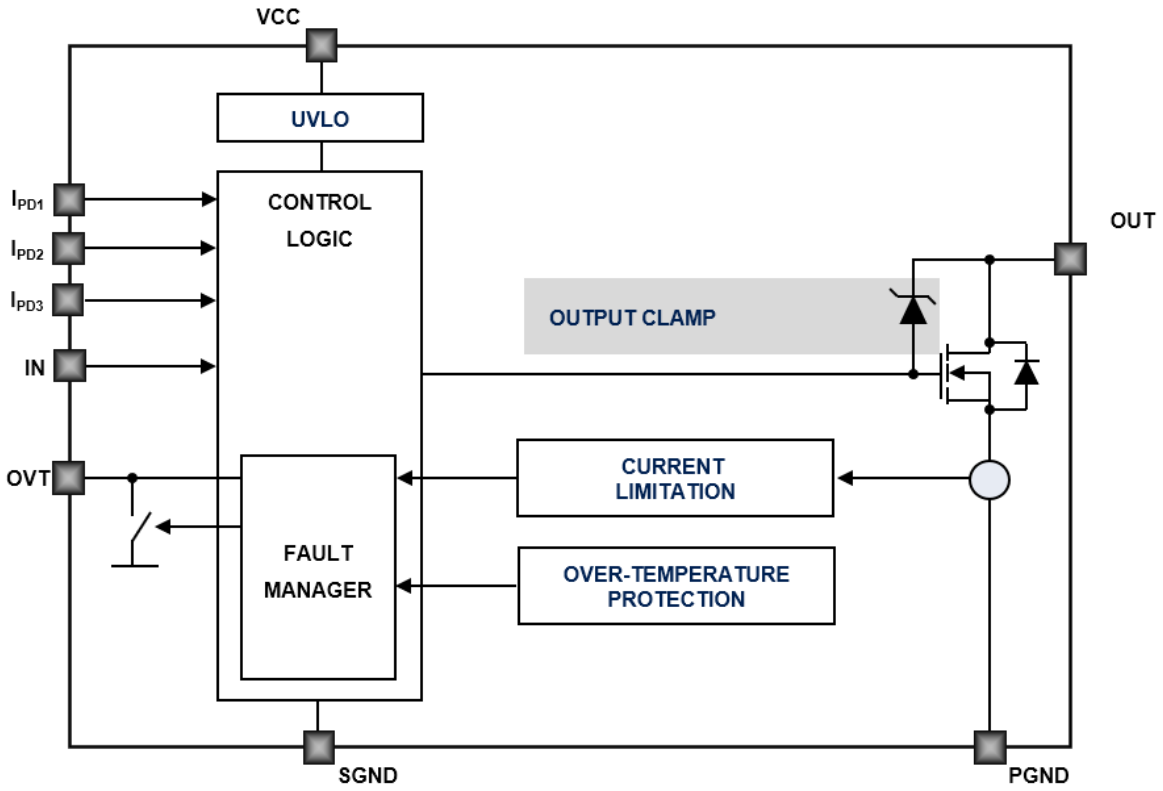
After the inrush current phase, the embedded overload protection can limit the steady state output current to I_{LIM} level featuring both the IC and load protections.

The output channel is protected against junction over-temperature by dedicated temperature sensor.

The diagnostic pin OVT is activated while the over-temperature event persist.

1 Block diagram

Figure 1. **Block diagram**



2 Pin connection

Figure 2. **Pin connections (top through view)**

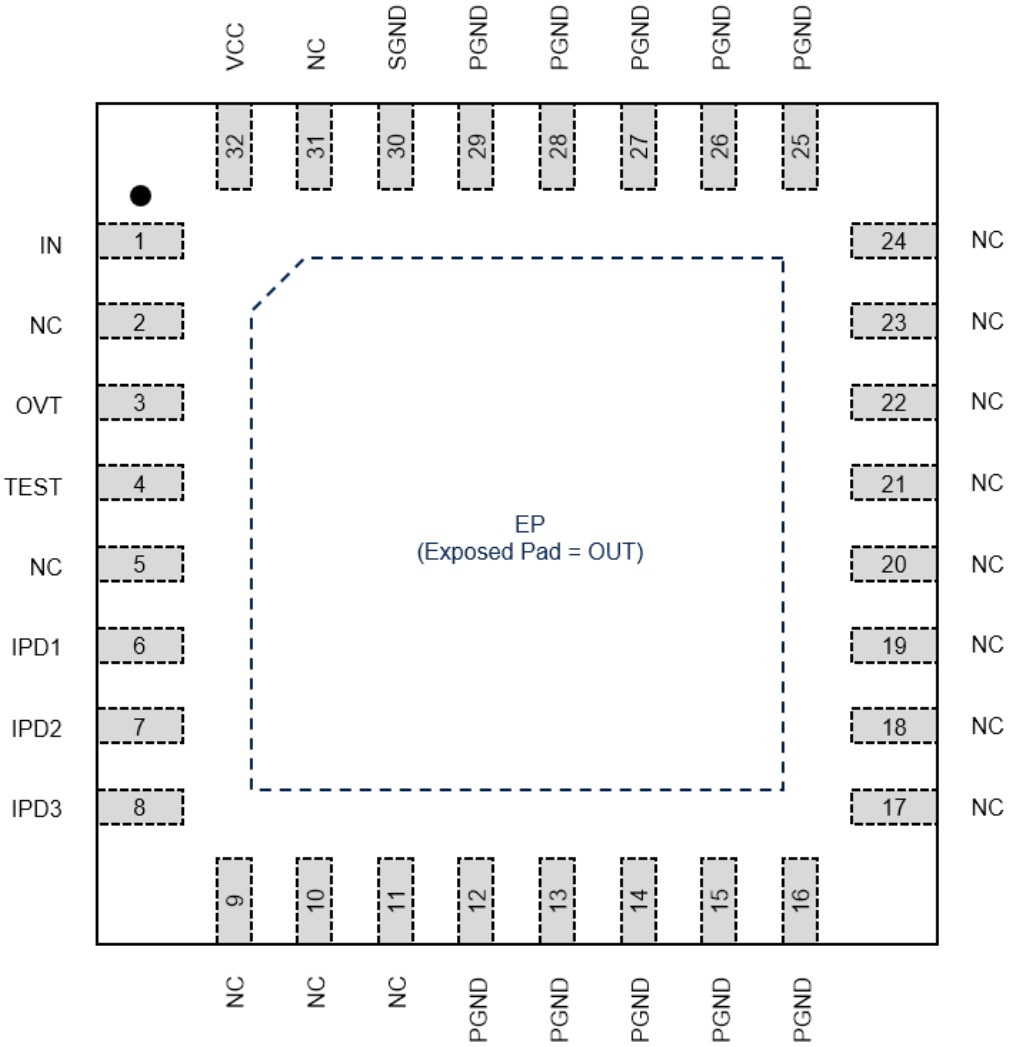


Table 1. Pin descriptions

N.	Name	Function	Type
1	IN	Input signal driving internal power switch and power supply.	Input
2	NC	This lead is not internally connected: it can be used for routing at pcb level.	-
3	OVT	Overtemperature diagnostic pin. This pin is activated when the IC triggers the over-temperature condition.	Output (Open Drain)
4	TEST	Reserved for internal use: leave it floating or connected to SGND by 1 kΩ resistor.	Open Drain
5	NC	This lead is not internally connected: it can be used for routing at pcb level.	-
6	IPD1	Current limitation level and timer selectors. These I_{PDX} pins can be set High or Low by connecting to IN or SGND pins through a 10 kΩ resistor to select the steady state current limitation level, Table 11(1). Smart/dynamic output current limitation can be activated by connecting the pin I_{PDX} pin to SGND by a capacitor (C_{PDX}) defining how long the initial level is active ($I_{LIM(I)}$) before the steady state limitation level ($I_{LIM(S)}$) is activated. The $I_{LIM(S)}$ remains active until next Low-to-High transition of the IN pin, Table 12(1). It is also possible to connect a capacitor between each I_{PDX} pin and SGND. The output current limitation level automatically reduces from highest current limitation level to lowest level across intermediate levels; the values of the C_{PDX} capacitors define how long each level remains active and the sequence of the intermediate levels, Figure 4. Leaving I_{PDX} floating is equivalent to a 1 µs duration for D_{PKX}. *(1): the maximum operating current in steady state condition is anyway limited by the thermal capability of the package and by the ambient temperature. For example, assumed the $R_{TH(JA)}$ reported in* Table 3 *and load current of 6.0 A with $I_{PD1, 2, 3}$ = L-H-H, the maximum ambient temperature is 92 °C.*	Logic / Analog Input
7	IPD2		
8	IPD3		
9,10,11	NC	These leads are not internally connected: they can be used for routing at pcb level.	-
12,13,14,15,16 25,26,27,28,29	PGND	Internal power switch ground. These leads are connected to the source of the embedded N-channel power switch.	Ground
17,18,19,20,21, 22,23,24	NC	These leads are not internally connected: they can be used for routing at pcb level.	-
30	SGND	Internal Logic ground.	Ground
31	NC	This lead is not internally connected: it can be used for routing at pcb level.	-
32	VCC	Logic supply voltage.	Supply
EP	OUT	Power stage output / load connection point. The exposed pad is connected to the drain of the embedded N-channel power mosfet.	Analog Output

3 Absolute maximum ratings

Absolute maximum ratings are the values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All voltages are referenced to GND.

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{OUT}	Voltage at output switch drain	Internally clamped	V
I_{OUT}	Output switch current	Internally limited	A
$-I_{OUT}$	Reverse output current (from PGND to OUT)	30 (1)	A
V_{CC}	Voltage at supply pin	-0.3 to 12	V
V_{IN}	Input pin voltage	-0.3 to 5.5	V
I_{IN}	Input pin current	-1/+10	mA
V_{PDX}	I_{PD1}, I_{PD2}, I_{PD3} pins voltage	-0.3 to 5.5	V
I_{PDX}	I_{PD1}, I_{PD2}, I_{PD3} pins current	-1/+10	mA
V_{DIAG}	OVT pin voltage	-0.3 to 5.5	V
I_{DIAG}	OVT pin current	-1/+10	mA
E_{AS}	Single pulse avalanche energy (T_{AMB} = 125 °C, V_{LOAD} = 24 V, I_{OUT} = 2 A)	1	J
P_{TOT}	Power Dissipation at T_C = 25 °C	Internally limited	W
T_{STG}	Storage Temperature Range	-55 to 150	°C
T_J	Junction Temperature	-40 to 150	°C

1. *The limit is intended with all PGND leads connected to the ground layer of the application board. Also, note that in reverse polarity conditions the internal protections (such as overload and over-temperature) are not active.*

4 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{th(JC)}$ (1)	Thermal resistance junction-case	2	°C/W
$R_{th(JA)}$ (2)	Thermal resistance junction-ambient	32 (3)	°C/W

1. *Rth between the die and the bottom case surface measured by cold plate as per JESD51-12*
2. *JESD51-7.*
3. *Maximum output power =2 W (at T_J < 150 °C and T_{AMB} = 85 °C).*

5 Electrical characteristics

(V_{CC} = 9 V; -40 °C < T_J < 125 °C, unless otherwise specified)

Table 4. Output stage

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating range	-	5.8		10	V
$V_{CC(ON)}$	VCC activation threshold	VCC rising		5.3	5.8	V
$V_{CC(OFF)}$	VCC deactivation threshold	VCC falling	4.5	5.2		V
$V_{CC(HYST)}$	VCC deactivation hysteresis	-		0.2		V
$I_{CC(ON)}$	Supply current in ON state	V_{IN} = 3.3 V		1	1.4	mA
$I_{CC(OFF)}$	Supply current in inactive status	V_{IN} = SGND		1	1.5	mA
R_{DSON}	On-state resistance	V_{CC} = 6 V, V_{IN} = 3.3 V, I_{LOAD} = 2 A, @ T_J = 25 °C		25		mΩ
		V_{CC} = 6 V, V_{IN} = 3.3 V, I_{LOAD} = 2 A, @ T_J = 125 °C			50	mΩ
V_{DEMAG}	Output Clamp Voltage	IOUT ≥ 50 mA	65	70	75	V
$I_{OUT(OFF)}$	OFF state output current	V_{IN} = 0 V, V_{OUT} = 7 V			3	µA
		V_{IN} = 0 V, V_{OUT} = 24 V			4	
		V_{IN} = 0 V, V_{OUT} = 36 V			6	
		V_{IN} = 0 V, V_{OUT} = 60 V			25	
Body diode of output switch						
$V_{OUT(REV)}$	Forward voltage of output switch	V_{IN} = 0V, I_{OUT} = -5 A			1.5	V
t_{rr} (1)	Reverse recovery time	I_{OUT} = -5 A, di/dt = 25 A/µs, V_{OUT} = 24 V, T_J = 25 °C		250		ns
Q_{rr}(1)	Reverse recovery charge			1		µC
I_{RRM}(1)	Reverse recovery current			8		A

1. *Not tested at final test*

Table 5. Input and I_{PDx} pins

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IH}	Input pin high level voltage	IN pin voltage rising	2.2			V
V_{IL}	Input pin low level voltage	IN pin voltage falling			0.75	V
$V_{I(HYST)}$	Input pin hysteresis voltage			0.3		V
I_{IN}	Input pin current	VCC = 6 V, V_{IN} = 3.3 V, OUT = open load		45	110	µA
$V_{IPD(T)}$	V_{IPDX} pins transition voltage (L-H or H-L)	I_{PDX} voltage rising or falling		2.4		V

Table 6. Switching

(VCC = 6 V, V_{IN} = 3.3 V, V_{LOAD} = 24 V, R_{LOAD} = 12 Ω)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_f	Output voltage fall time	Power switch activation, see Figure 3		20	40	µs
$t_{PD(H-L)}$	Propagation delay time IN to OUT (V_{OUT} level high to low)			10	20	µs
t_r	Output voltage rise time	Power switch deactivation, see Figure 3		15	25	µs
$t_{PD(L-H)}$	Propagation delay time IN to OUT (V_{OUT} level low to high)			25	50	µs

Figure 3. Timing

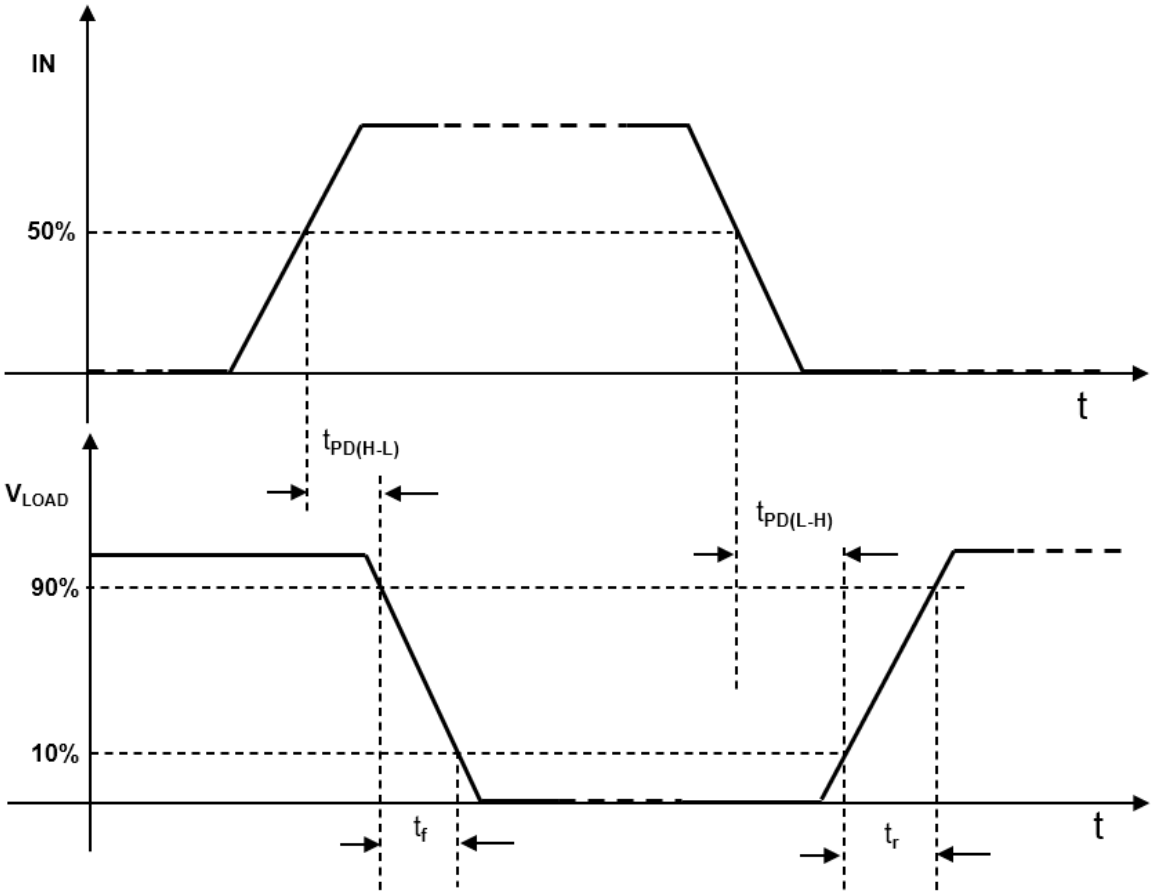


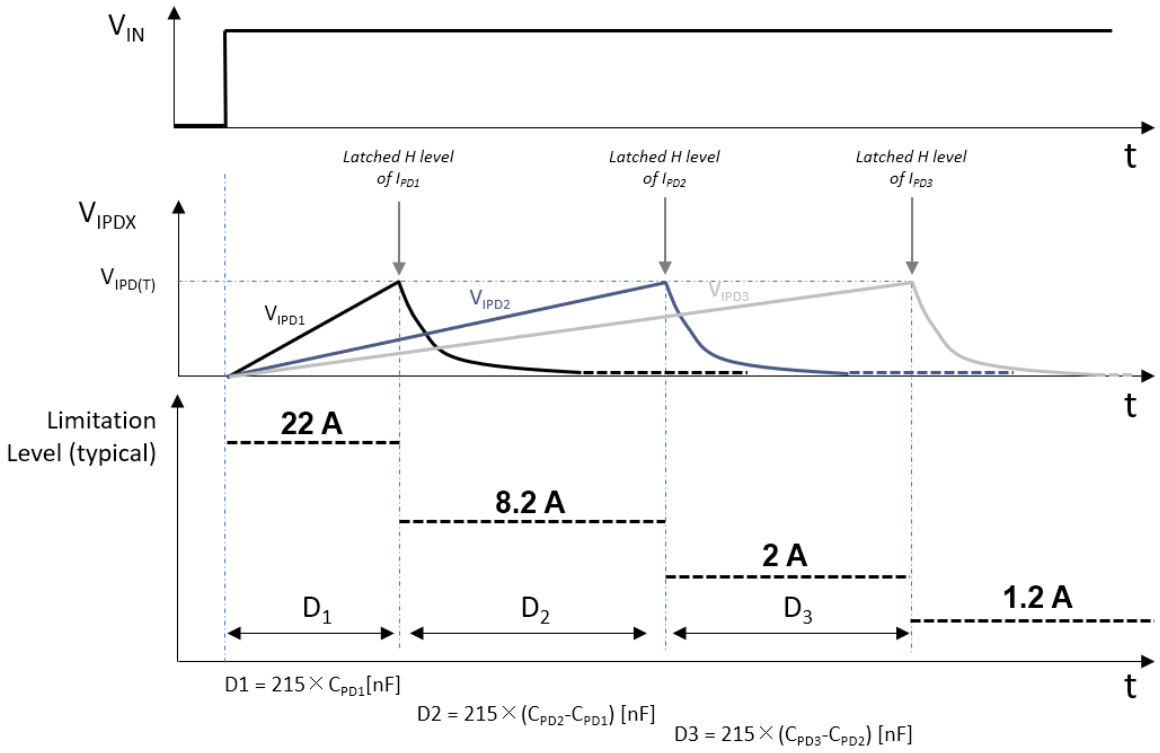
Table 7. Diagnostic pin (OVT)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{DIAG}	Voltage drop on OVT pin	I_{DIAG} = 4 mA Fault condition active		0.85	1	V
I_{DIAG}	Leakage current on OVT pin	V_{DIAG} = 3.3 V Fault condition not active			5	µA

Table 8. Protections and Diagnostic

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Static Overload detection and output current limitation: I_{PDX} pins set High (= 3.3 V) or Low (= SGND)						
$I_{PK(S)}$	Overcurrent activation threshold			$I_{LIM(S)}$ + 20%		A
$I_{LIM(S)}$	Overcurrent limitation level	I_{PD1} = L, I_{PD2} = L, I_{PD3} = L	21	25	39	A
		I_{PD1} = L, I_{PD2} = L, I_{PD3} = H	15.8	22	27.5	A
		I_{PD1} = L, I_{PD2} = H, I_{PD3} = L	11	16.5	22	A
		I_{PD1} = L, I_{PD2} = H, I_{PD3} = H	7.9	12	16	A
		I_{PD1} = H, I_{PD2} = L, I_{PD3} = L	4.5	8.2	12	A
		I_{PD1} = H, I_{PD2} = L, I_{PD3} = H	2.4	4	5.6	A
		I_{PD1} = H, I_{PD2} = H, I_{PD3} = L	1	2	3	A
		I_{PD1} = H, I_{PD2} = H, I_{PD3} = H	0.7	1.2	1.8	A
Dynamic Output Overload detection limitation: example with I_{PD1} connected to SGND by capacitor C_{PD1}, I_{PD2} and I_{PD3} pins set High (= 3.3 V) or Low (= SGND). Other configurations with capacitor on I_{PD1}, and/or on I_{PD2} and/or I_{PD3} are allowed: see Figure 4						
$I_{PK(I)}$	Initial overcurrent activation threshold			$I_{LIM(S)}$ + 20%		A
$I_{LIM(I)}$	Initial overcurrent limitation level	I_{PD1} = to SGND by C_{PD1} I_{PD2} = L, I_{PD3} = L	21	25	39	A
$D_{PK(I)}$	Initial overcurrent time			215 × C_{PD1}[nF]		µs
$I_{LIM(S)}$	Steady state overcurrent limitation level		4.5	8.2	12	A
$I_{LIM(I)}$	Initial overcurrent limitation level	I_{PD1} = to SGND by C_{PD1} I_{PD2} = L, I_{PD3} = H	15.8	22	27.5	A
$D_{PK(I)}$	Initial overcurrent time			215 × C_{PD1}[nF]		µs
$I_{LIM(S)}$	Steady state overcurrent limitation level		2.4	4	5.6	A
$I_{LIM(I)}$	Initial overcurrent limitation level	I_{PD1} = to SGND by C_{PD1} I_{PD2} = H, I_{PD3} = L	11	16.5	22	A
$D_{PK(I)}$	Initial overcurrent time			215 × C_{PD1}[nF]		µs
$I_{LIM(S)}$	Steady state overcurrent limitation level		1	2	3	A
$I_{LIM(I)}$	Initial overcurrent limitation level	I_{PD1} = to SGND by C_{PD1} I_{PD2} = H, I_{PD3} = H	7.9	12	16	A
$D_{PK(I)}$	Initial overcurrent time			215 × C_{PD1}[nF]		µs
$I_{LIM(S)}$	Steady state overcurrent limitation level		0.7	1.2	1.8	A

Figure 4. **Dynamic current limitation (C_{PD1} < C_{PD2} < C_{PD3})**



6 Output Logic

Table 9. Output stage truth table

(L = pin voltage Low, H = pin voltage High, X = not determined)

Condition	$V_{IN(MCU)}$	IN	OUT	OVT
Normal Operation	L H	L H	H L	H H
Overload	L H	L H	L X(1)	H H
Junction over-temperature protection (2)	L H	L H	H H	L L

1. *Pin voltage = $V_{SUPPLY} – (I_{OUT} * R_{LOAD})$*
2. *When $T_J > T_{JSD}$ OUT is forced OFF, OVT is activated*

7 Application Schematics Examples

Figure 5. **Application schematic: example of static setting of current limitation**

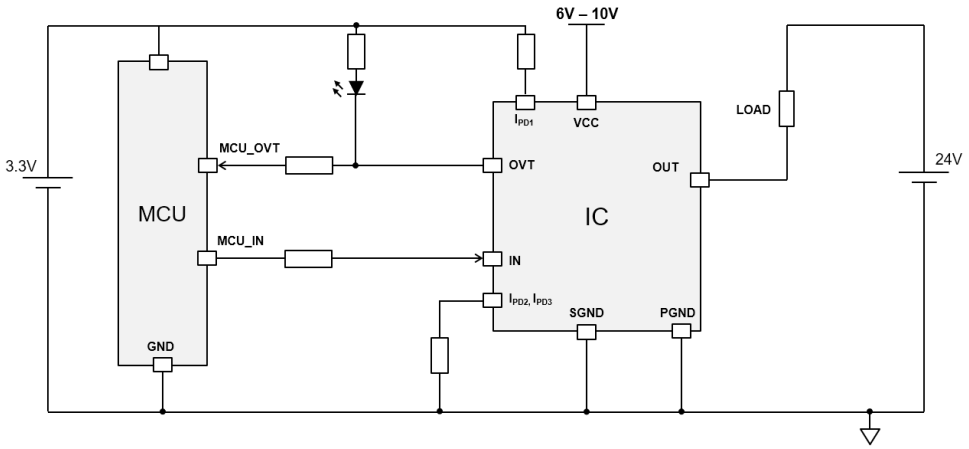


Figure 6. **Application schematic: example of dynamic control of current limitation by GPIOs**

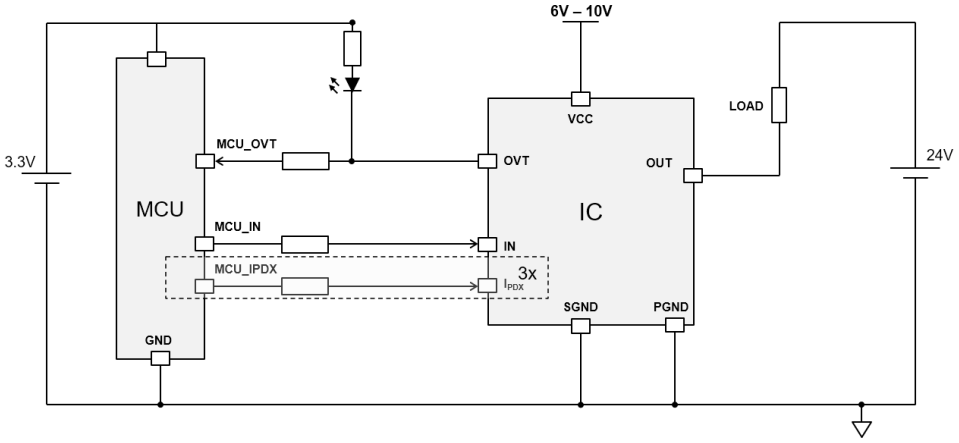


Figure 7. **Application schematic: example of dynamic control of current limitation with single capacitor**

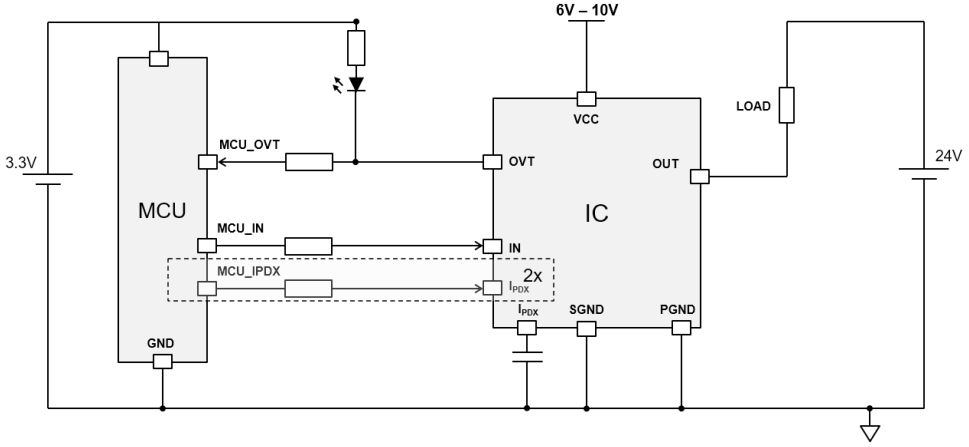


Figure 8. **Application schematic: example of dynamic control of current limitation with two capacitors**

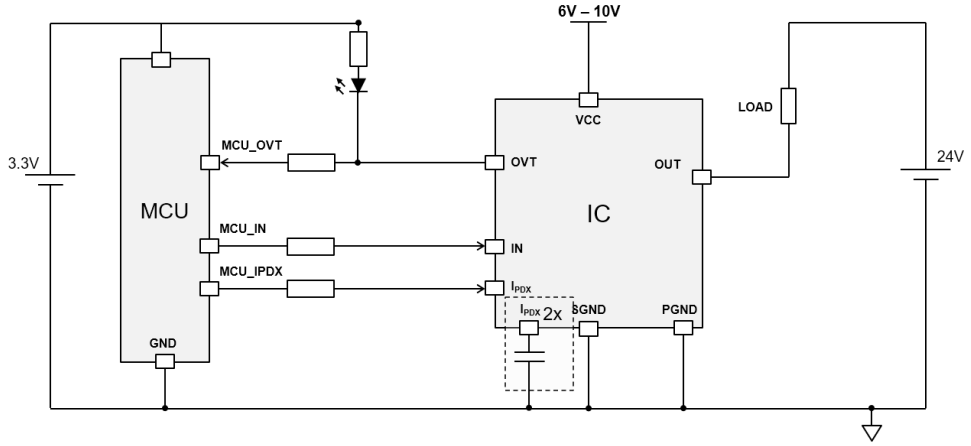
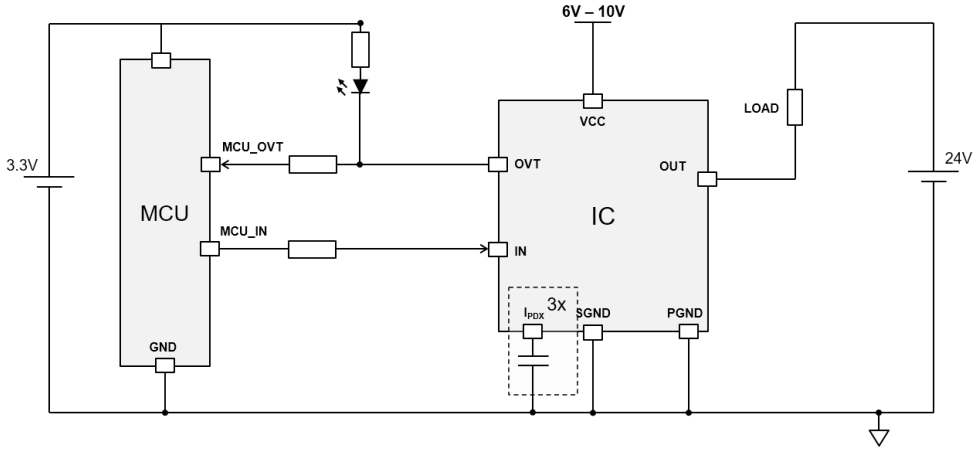


Figure 9. **Application schematic: example of dynamic control of current limitation with three capacitors**



8 Protections and diagnostic

The IC integrates several protections to help the design of robust applications.

8.1 Over-temperature

The device is protected against overheating in case of overload conditions. During the driving period (by means when the MCU is forcing high the IN pin), if the output is overloaded, then the device suffers huge thermal stress.

In thermal stress conditions the junction thermal shutdown protection is activated: the output channel (OUT) is turned off when its junction temperature (T_J) is higher than the activation threshold (T_{JSD}) and turned back on when it goes below the reset threshold (T_{JR}).

This behavior continues until the fault on the output is present. When the thermal protection is active for OUT, the OVT pin is activated accordingly.

Figure 10 shows the thermal protection behavior, while Figure 11 reports typical temperature trends and output vs input state.

Figure 10. Thermal protection flowchart

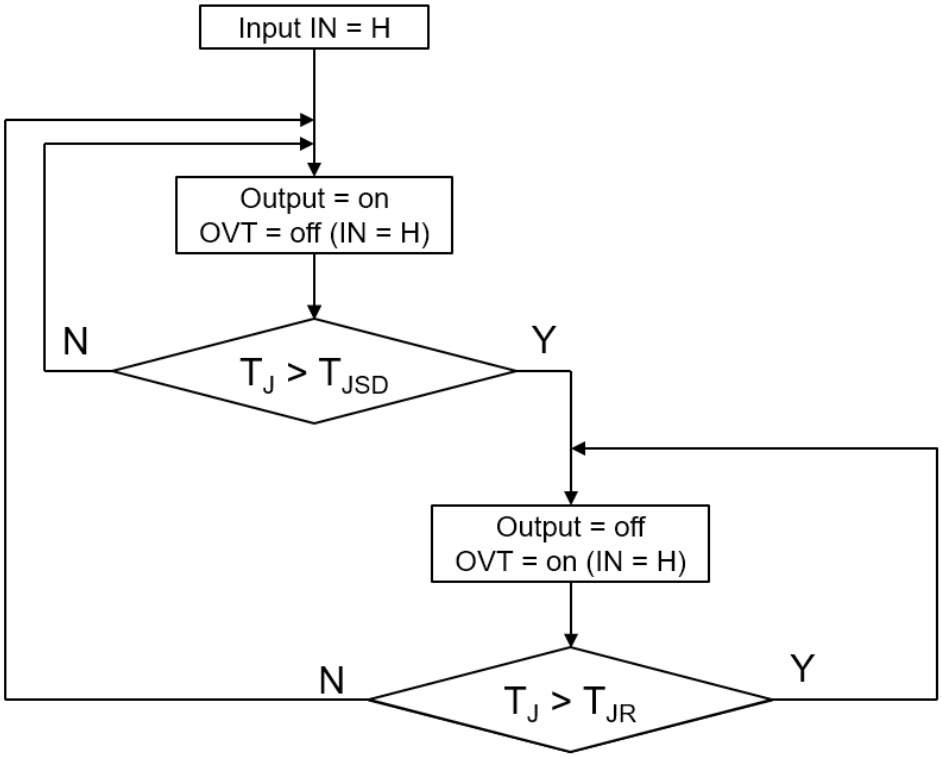


Figure 11. **Thermal protection plot**

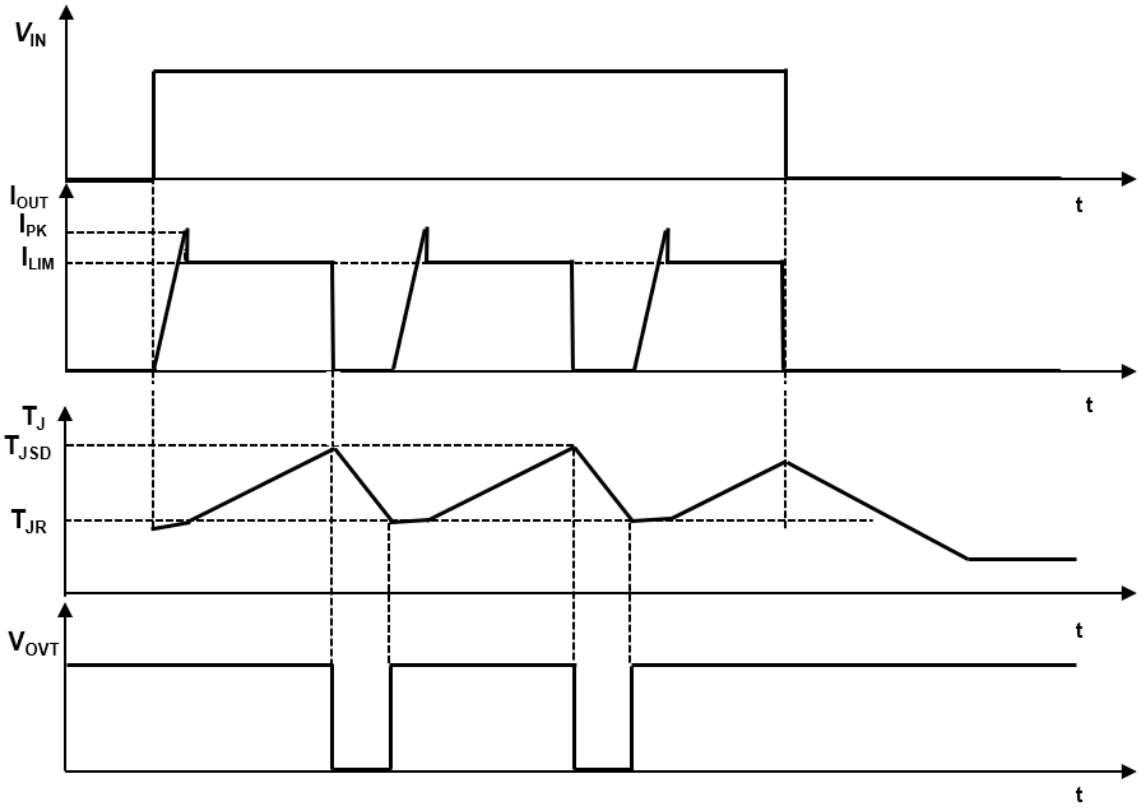


Table 10. **Thermal protection temperatures**

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{JSD}	Junction temperature shutdown	150	170	190	°C
T_{JR}	Junction temperature reset		150		°C
T_{JHYS}	Junction temperature hysteresis		20		°C

8.2 Overload

The IC integrates an output current control circuitry, activated when the IN pin goes High, guaranteeing the load and IC functionalities in case of overload or short circuit event.

If the sensing part of the control circuitry triggers the overcurrent activation threshold, then the same circuitry activates the output current limitation protection, by means that the current supplied to the load will be limited by a proper regulation of the V_{GS} on the integrated power switch.

The output current control circuit can work with static and dynamic thresholds, according to the settings of the pins I_{PD1} and I_{PD2}.

In the static current limitation, the I_{PDX} pins are set “High” or “Low”. The activation thresholds and limitation levels are reported in the section “**Static Overload detection and output current limitation: I_{PDX} pins set High or Low**” of Section 5.

Note that the I_{PDX} pins can be driven by the GPIO ports of an MCU or ASIC: in this case the system can switch between different thresholds and levels.

The dynamic current limitation becomes active if at least one of the I_{PDX} pins is connected to GND by a C_{PDx} capacitor. An internal circuitry supplies the C_{PDX} capacitor so that the related I_{PDX} pin goes from 0 V to “high level” in D_{PK} [µs]= 215 × C_{PDx} [nF].

Also, the internal circuitry on each I_{PDX} pin feature the reset of the I_{PDX} high voltage level so that the system is ready to restart at next transition of the IN pin.

The current limitation activation thresholds and current limitation levels with one I_{PDX} pin fixed high or low and other I_{PDX} pin connected to C_{PDX} are reported in the section "**Dynamic Output Overload detection limitation and output current limitation**" of Section 5.

If the final application requires same C_{PDX} capacitor for two or three I_{PDX} pins, then it is recommended to short the pins to share a single capacitor.

For convenience Table 11 and Table 12 summarize the possible current limitation levels.

Table 11. Static current limitation setting

I_{PD1}	I_{PD2}	I_{PD3}	I_{LIM} [A]		
			Min.	Typ.	Max.
L	L	L	21	25	39
L	L	H	15.8	22	27.5
L	H	L	11	16.5	22
L	H	H	7.9	12	16
H	L	L	4.5	8.2	12
H	L	H	2.4	4	5.6
H	H	L	1	2	3
H	H	H	0.7	1.2	1.8

Table 12. Mixed mode current limitation setting

I_{PD1}	I_{PD2}	I_{PD3}	$I_{LIM(I)}$ [A]	$I_{LIM(S)}$ [A]	$D_{PK(I)}$ [µs]
L	L	C_{PD}	25	22	215 × C_{PD} [nF]
L	H		16.5	12	
H	L		8.2	4	
H	H		2	1.2	
L	C_{PD}	L	25	16.5	
L		H	22	12	
H		L	8.2	2	
H		H	4	1.2	
C_{PD}	L	L	25	8.2	
	L	H	22	4	
	H	L	16.5	2	
	H	H	12	1.2	

9 Active clamp

Active clamp is also known as Fast Demagnetization of inductive loads or *Fast Current Decay*.

When a high-side driver turns off an inductance, an under-voltage on output is detected.

The OUT pin is pulled-down to V_{DEMAG}. The conduction state is modulated by an internal circuitry in order to keep the OUT pin voltage at ~V_{DEMAG} until the energy in the inductive load has been dissipated.

The energy is dissipated in both IC internal switch and load resistance.

Figure 12. Active clamp behavior

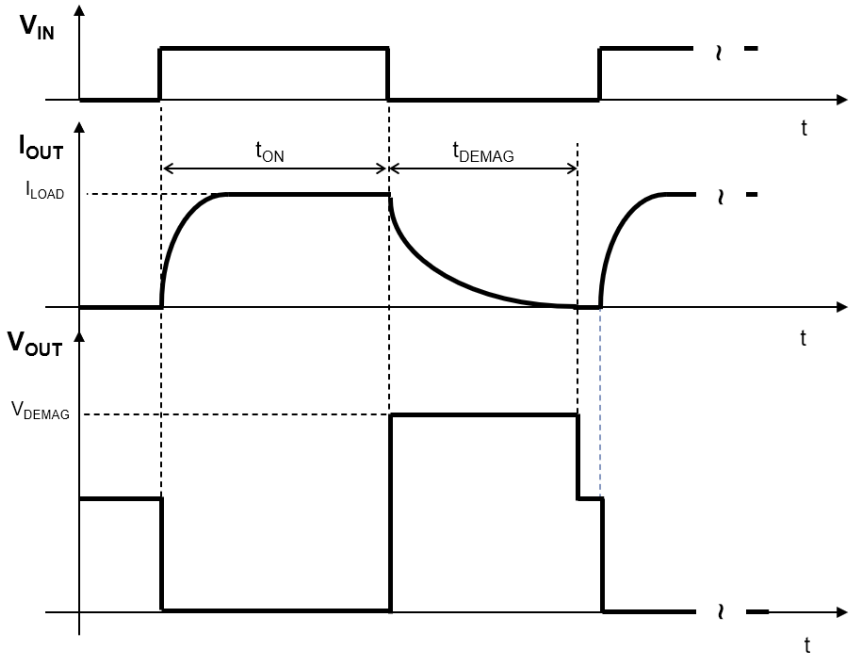


Figure 13. Typical demagnetization: E vs I (single pulse) at V_{LOAD} = 24 V and T_{AMB} = 125 °C

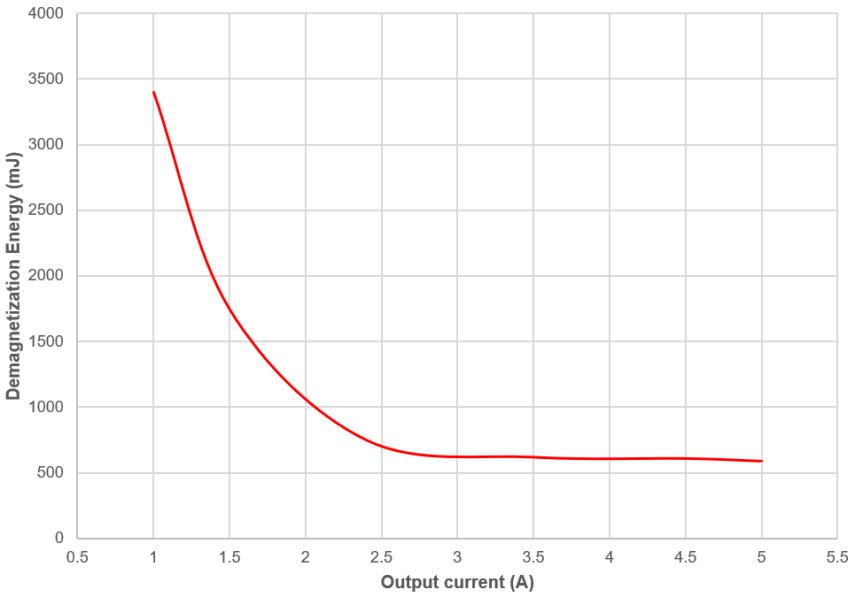
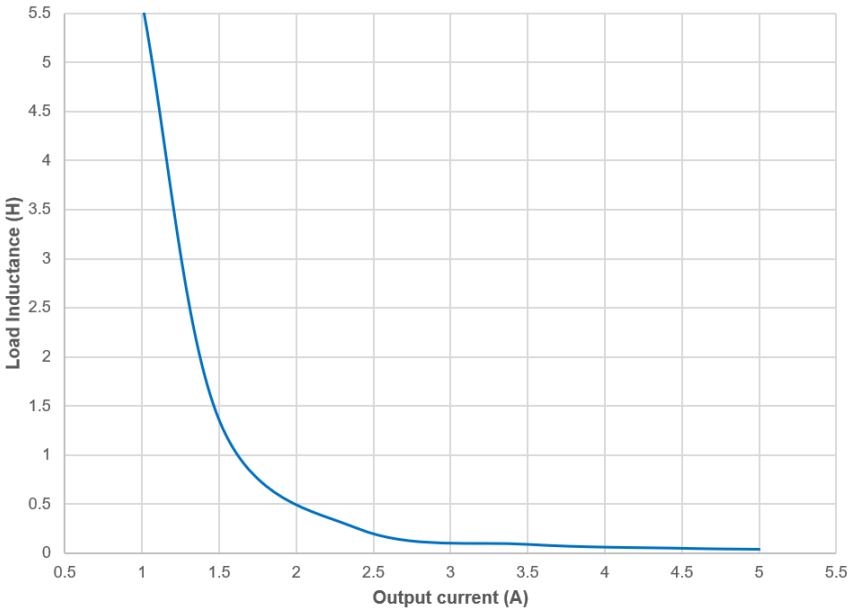


Figure 14. Typical demagnetization: L vs I (single pulse) at V_{LOAD} = 24 V and T_{AMB} = 125 °C



10 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com

ECOPACK is an ST trademark.

10.1 Package mechanical data

Figure 15. **QFN32L 6x6 package dimensions**

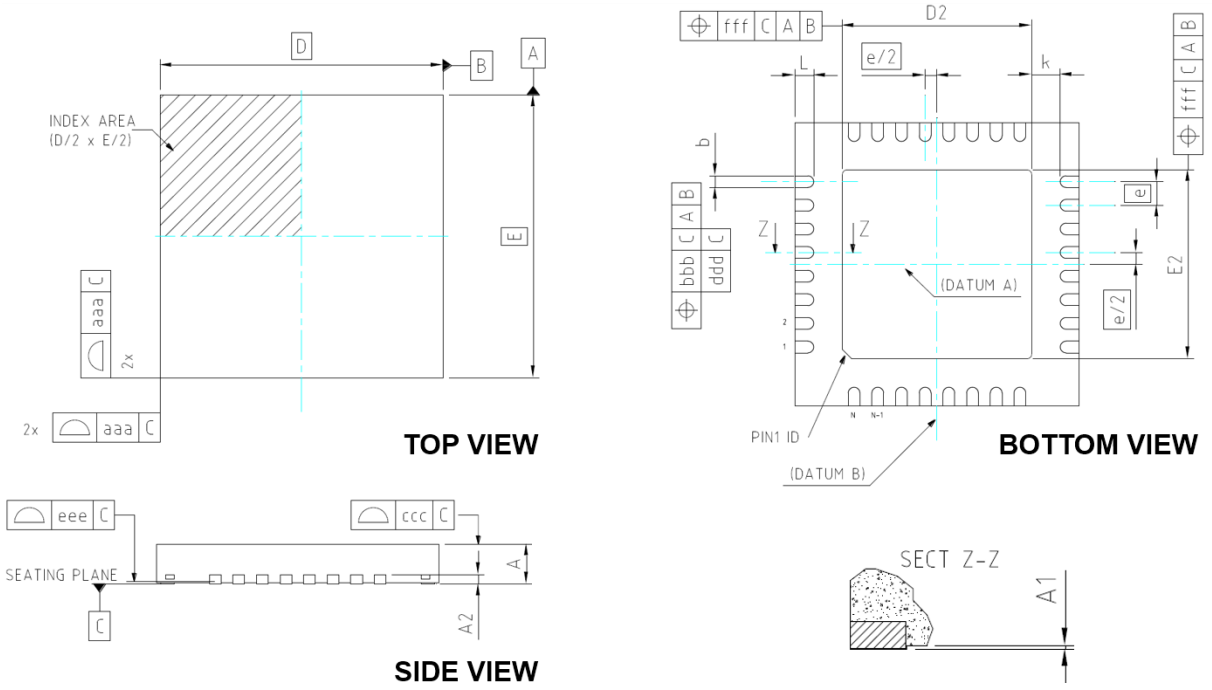


Table 13. **QFN32L 6x6 mechanical data**

Symbol	[mm]			Notes
	Min.	Nom.	Max.	
A	0.80	0.90	1.00	11
A1	0.00	0.02	0.05	8, 11
A2		0.2 REF		
L	0.35	0.40	0.45	11
b	0.20	0.25	0.30	7, 11
D		6.00		11
D2	3.90	4.00	4.10	11
E		6.00		11
E2	3.90	4.00	4.10	11
e		0.5		
k	0.55			
N		32		9

Table 14. Tolerance of forms and positions

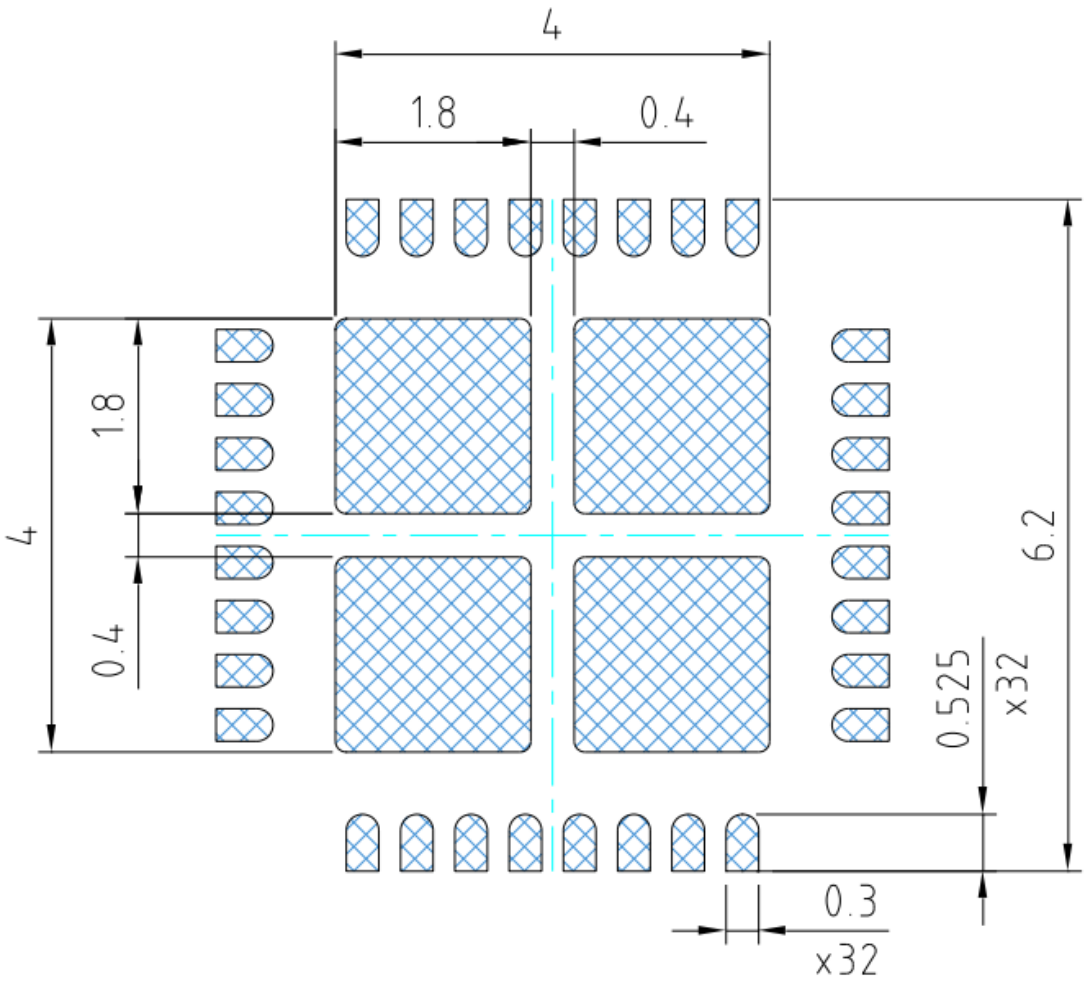
Symbol	Tolerance of forms and position	Notes
aaa	0.15	10
bbb	0.10	
ccc	0.10	
ddd	0.05	
eee	0.08	
fff	0.10	

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. Datum A-B to be determined at datum plane C.
3. To be determined at setting datum plane C.
4. Detail of pin 1 identifier are optional but must be located within the zone indicated.
5. All Dimensions are in millimeters.
6. Exact shape of each corner of the exposed die pad is optional.
7. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
8. A1 is defined as the distance from the seating plane to the lowest point on the package body.
9. “N” is the max number of terminal positions for the specified body size.
10. For Tolerance of Form and Position see Table.
11. Critical dimensions:
    - A
    - A1
    - A3
    - D & E
    - b & L
    - D2 & E2
12. Component cross reference: *OPTIONAL*.
13. For Symbols, Recommended Values and Tolerances see Table below: (ACCORDING TO JEDEC SPEC IF REGISTERED OR JEDEC DESIGN GUIDE).

Table 15. Definitions

Symbol	Definition	Notes
aaa	The bilateral profile tolerance that controls the position of the plastic body sides. The centers of the profile zones are defined by the basic dimensions D and E	For flange-molded packages, this tolerance also applies for basic dimensions D1 and E1. For packages tooled with intentional terminal tip protusion, aaa does not apply to those protusions.
bbb	The tolerance that controls the position of the entire terminal pattern with respect to Datum's A and B. The center of the tolerance zone for each terminal is defined by basic dimension "e" as related to Datum's A and B	
ccc	The tolerance located parallel to the seating plane in which the top surface of the package must be located	
ddd	The tolerance that controls the position of the terminals to each other. The centers of the profile zones are defined by basic dimension "e"	This tolerance is normally compounded with tolerance zone defined by bbb
eee	The unilateral tolerance located above the seating plane where in the bottom surface of all terminals must be located	This tolerance is commonly known as the "coplanarity" of the package terminals
fff	The tolerance that controls the position of the exposed metal heat feature. The center of the tolerance zone is the datum's defined by the center lines of the package body	This tolerance applies to an optional package feature

Figure 16. QFN32L 6x6 Suggested footprint



11 Packing mechanical data

Figure 17. **QFN32L 6x6 mm reel shipment**

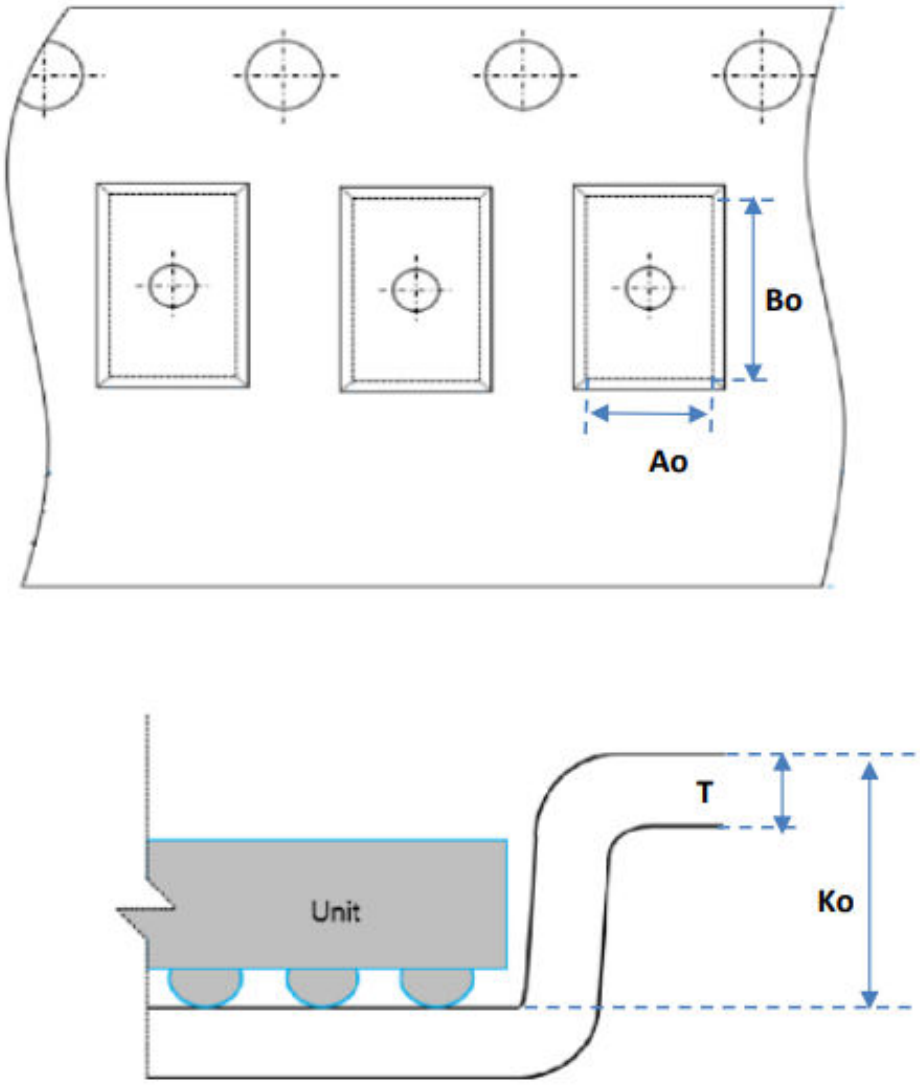


Table 16. **Standard SPC parameters**

Item	Description
Ao	Pocket Length
Bo	Pocket Width
Ko	Pocket Depth
T	Tape Thickness

Figure 18. **QFN32L 6x6 mm carrier tape dimensions**

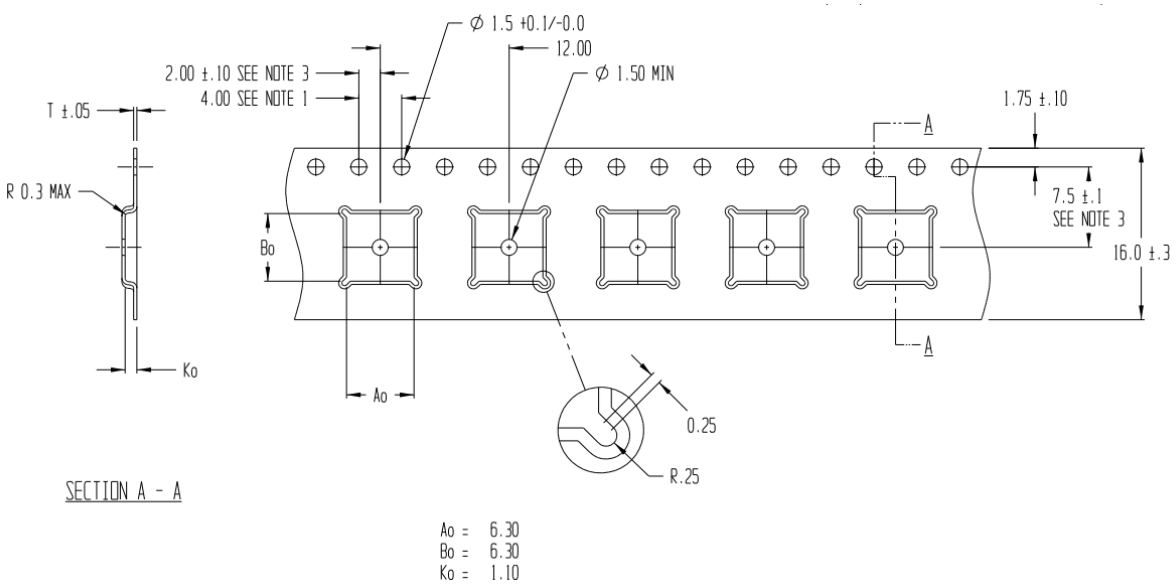
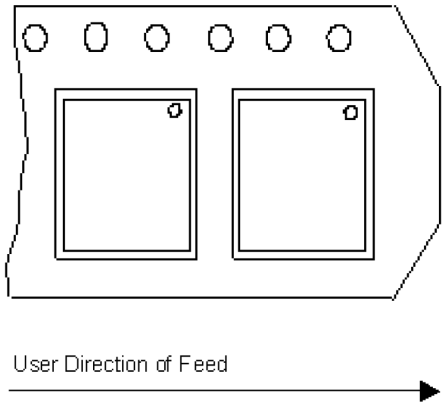


Figure 19. **QFN32L 6x6 mm carrier tape, Pin 1 indication**



12 Ordering information

Table 17. **Ordering information**

Part number	Package	Packaging
IPS1050LQ	QFN32L 6x6 mm	Tape and reel

Revision history

Table 18. **Document revision history**

Date	Version	Changes
29-Sep-2025	1	Initial release.
06-Oct-2025	2	Corrected test conditions in the Figure 13 and Figure 14; some minor changes.

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