Description

The OB1203 Sensor Module integrates a multi-channel light sensor (LS/CS), a proximity sensor (PS), and a photoplethysmography sensor (PPG).

The light sensor can be configured as ambient light sensor (LS) to measure ambient light similar to the human eye experience or as an RGB color sensor (CS). The module has a fully integrated biosensor for reflective photoplethysmography. With the appropriate algorithm, it can determine human heart rate (HR), oxygen saturation (SpO2), respiration rate, and heart rate variability (a measure of stress). The OB1203 integrates light sources and drivers in a single optically optimized package.

A major LS application of the device is in smart phones or other mobile devices to enable brightness control of display panels. The OB1203 can also determine proximity of nearby objects in order to support the activation of touch screen displays or system functions. The sensor combines optical sensing features (CS, LS, and PS) and bio-sensing functionality (PPG) without needing a visible optical opening. The unique implementation of the OB1203 enables SpO_2 measurements behind ink that is IR transmissive, but visibly dark, allowing implementation in aesthetic industrial designs.

Biosensor Features

- SpO_2 measurement behind visibly dark, IR transmissive ink
- Industry's smallest optical biosensor module
- Fully integrated and trimmed module, including two LEDs, 250mA maximum drive current, and photodetectors
- Output resolution PPG: 16 to 18 bits
- Data stored in 18-bit wide, 32-sample FIFO memory
- Integrated averaging function for higher signal-to-noise ratio (SNR) and data rate reduction
- Programmable measurement rate: up to 3200 samples per second
- High SNR

Ambient Light Sensor Features

- High lux accuracy over different light sources
- Absolute sensitivity: 0.06 lux to > 150000 lux
- Output resolution LS/CS: 13 to 20 bits
- Three LS/CS gain modes: x1 to x6
- Highly linear output, 50Hz/60Hz light and fluorescent light flicker immunity

Color Sensor Features

- Four parallel channels (red, green, blue, clear)
- Accurate Correlated Color Temperature (CCT)
- Accurate CIE 1931 XYZ (RGB) color measurement
- Very stable spectral response over angle of light incidence
- Output resolution CS: 13 to 20 bits

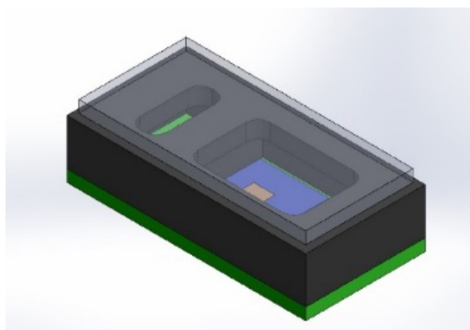
Proximity Sensor Features

- Integrated and trimmed LED source, driver, and photodetector
- Programmable pulsed LED up to 250mA output current
- High resolution (12 to 16 bits)
- Object movement detection (in/out)
- Ambient light suppression > 100klx sun light
- Crosstalk cancelation (analog and digital)

Physical Characteristics

- Highly reliable and industry-proven OSIP package with integrated cover glass for hypoallergenic products
- Wide operation temperature: - 40°C to +85°C
- Wide supply voltage: 1.7V to 3.6V
- Typical active current at minimum duty cycle:
  - LS/CS:110µA
  - PS: 90µA + LED current (typical ~300µA average)
- Low standby current: 2µA typical
- I2C interface capable of Standard Mode (100kHz) or Fast Mode (400kHz) communication; 1.8V to 3.3V logic compatible
- Programmable level-based interrupt functions with upper and lower thresholds for extending battery life
- Industry's smallest package: 4.2 × 2 × 1.2 mm^3 14-OSIP module

Figure 1. 3D Package Rendering



Biosensor, LS and PS Applications

- Mobile devices such as smartphones, smart accessories, touch screen disable, display brightness and color adjust, smartwatches, secondary sensor for blood pressure
- Head phones
- Hearables
- Fitness and wellness
- Occupancy
- Gesture detection
- Industrial applications such as proximity and light detection in less than 1ms, fast light barriers, lighting control, robotics, agriculture and hydroponic light sensing, daylighting

Application Circuit

Figure 2. Typical Circuit – Only 6 Connections

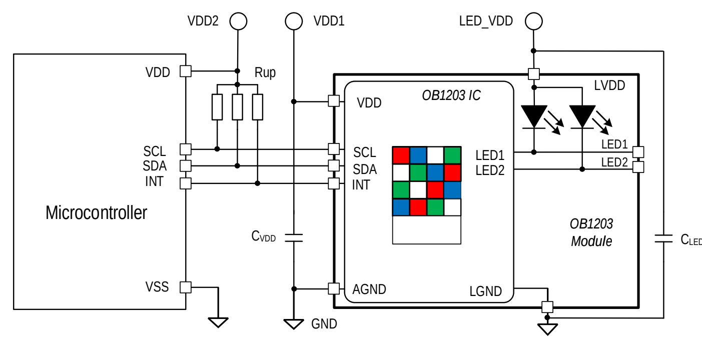


Figure 3. Block Diagram

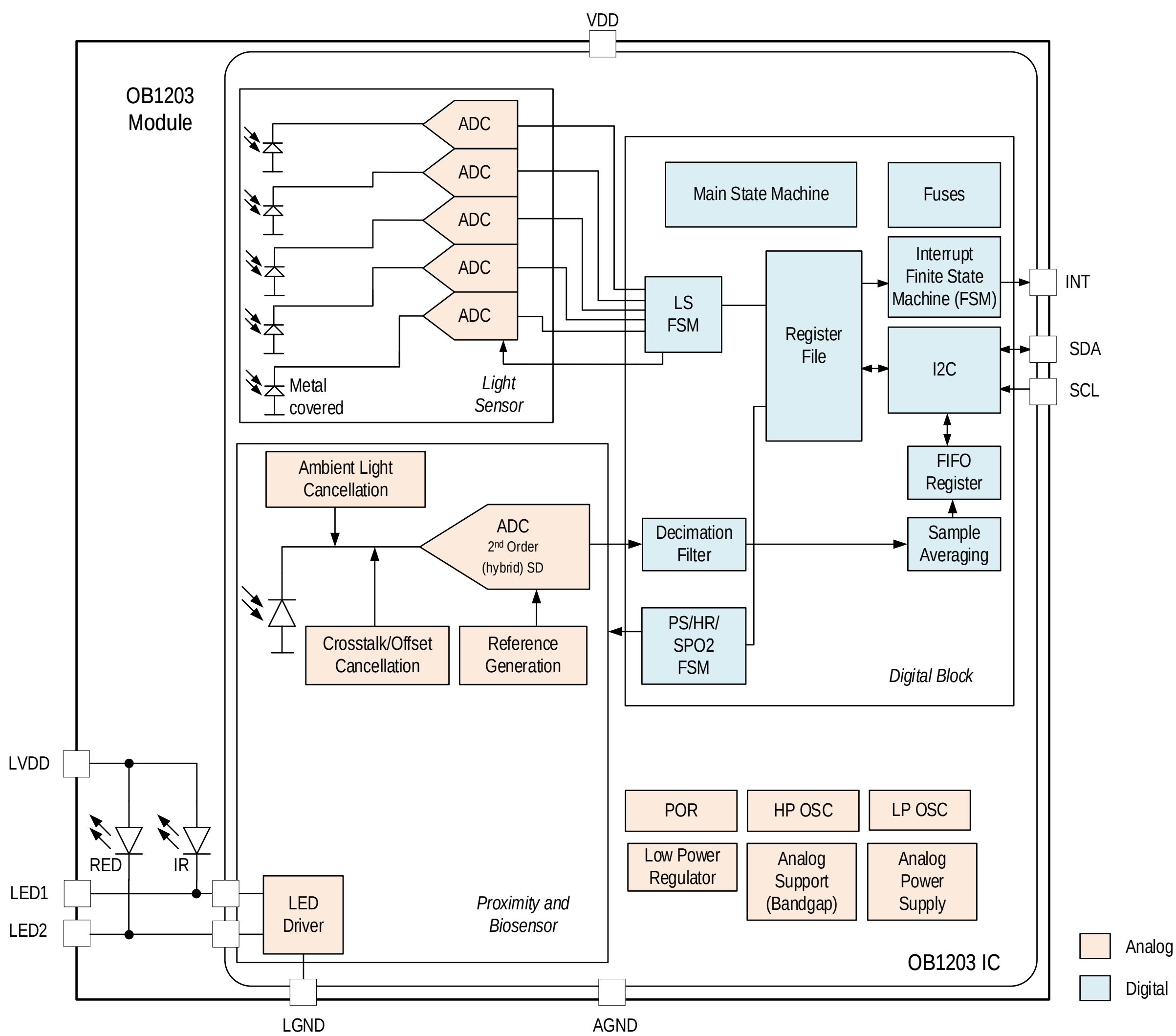


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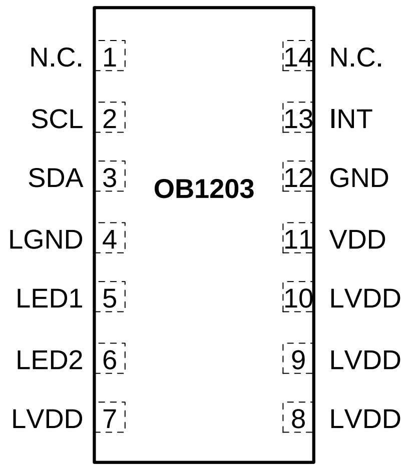
Figure 4. Pin Assignments for 2 × 4.2 × 1.2 mm 14-OSIP Package – Top View



2. Pin Descriptions

Table 1. Pin Descriptions

Pin Number	Name	I/O Type	Description
1	N.C.	–	Not connected internally. Can be connected to ground.
2	SCL	IN	I2C serial clock line.
3	SDA	IN/OUT	I2C serial data line.
4	LGND	GROUND	LED/digital ground (required).
5	LED1	–	IR LED driver test pin (LED cathode / driver output).
6	LED2	–	Red LED driver test pin (LED cathode / driver output).
7, 8, 9, 10	LVDD	SUPPLY	LED power supply.
11	VDD	SUPPLY	Digital/analog power supply.
12	GND	GROUND	Analog ground.
13	INT	OUT	Interrupt pin.
14	N.C.	–	Not connected internally. Can be connected to ground.

3. Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. The device might not function or be operable above the recommended operating conditions given in this section. Stresses exceeding the absolute maximum ratings might damage the device. In addition, extended exposure to stresses above the recommended operating conditions might affect device reliability. Renesas does not recommend designing to the "Absolute Maximum Ratings."

Global measurement conditions V_{DD} = 2.8V, T_{AMB} = 25ºC unless otherwise noted.

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{DD-GND}	Maximum input supply voltage (VDD pin)			3.6	V
V_{I2C}	Maximum voltage on SCL, SDA and INT pins		-0.5	3.6	V
V_{LED}	Maximum voltage on LVDD pins	VDD supplied in operation range	-0.5	5.0 [a]	V
T_{AMB_MAX}	Maximum operating temperature range		-40	85	°C
T_{STOR}	Storage temperature		-45	90	°C
I_{IN}	Maximum input current into any pin except supply / LED pins (latch-up)		-100	100	mA
V_{HBM}	Electrostatic discharge protection [b]	Human Body Model, JESD22-A114	2000		V
V_{CDM}	Charge Device Model		1000		V

[a] If V_{DD} = 0V, then maximum V_{LED} = 3.6V.

[b] HBM: C = 100pF charged to V_{HBM} with resistor R = 1.5kΩ in series; valid for all pins.

4. Recommended Operating Conditions

Global measurement conditions V_{DD} = 2.8V, T_{AMB} = 25ºC unless otherwise noted.

Table 3. Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{DD}	Voltage supply on VDD pin	1.7		3.6	V
T_{AMB}	Ambient operating temperature range	-40		85	°C
V_{LED}	LED power supply (VDD supplied in operating range)	3.3		4.5 [a]	V

[a] If V_{DD} = 0V, then maximum V_{LED} = 3.6V.

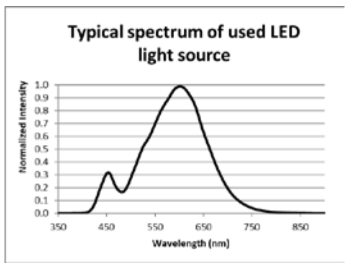
5. Electrical and Optical Characteristics

Global measurement conditions V_{DD} = 2.8V, T_{AMB} = 25ºC unless otherwise noted.

Table 4. Electrical and Optical Characteristics

Note: See important table notes at the end of the table.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
Power On Reset						
POR_{LH} POR_{HL}	DC power-on reset level	Slow variation of VDD (< 1ms), T_A = 25°C		1.2		V
Current Consumption						
I_{LS}	LS/CS (clear and color sensor) active mode current [a]	Default setting; 100% duty cycle; VDD = 2.8V; Gain Mode 3		110		µA
I_{PS_pk}	PS (proximity sensor) active mode peak current [b]	Default setting; 100ms period; VDD = 2.8V		750		µA
I_{PS_avg}	PS (proximity sensor) active mode average current [b]	Default setting; 100ms period; VDD = 2.8V		80		µA
I_{PPG1_VDD}	PPG1 active mode VDD average current	Default measurement period and pulse width		730		µA
I_{PPG2_VDD}	PPG2 active mode VDD average current	Minimum PPG pulse width and period setting (maximum rate)		780		µA
I_{PPG1_LED}	PPG1 active mode LED average current	125mA LED current setting, default PPG pulse width and period settings		30		mA
		125mA LED current setting, minimum PPG pulse width and period settings (maximum rate)		50		mA
I_{PPG2_LED}	PPG2 active mode LED average current	125mA LED current setting, default PPG pulse width and period settings		48		mA
		125mA LED current setting, minimum PPG pulse width and period settings (maximum rate)		43		mA
I_{SBY}	Standby VDD current [c]	The OB1203 is in Standby Mode; no active I2C communication		< 2	5	µA
I2C Interface						
$V_{I2Chigh}$	I2C signal input high		1.26		VDD	V
V_{I2Clow}	I2C signal input low		0		0.54	V

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
LS Light Sensor Characteristics						
	Spectral response		See Figure 12.			
RES_{LS}	LS output resolution	Programmable to 13, 16, 17, 18, 19, 20 bit	13	18	20	bit
	Dark level count	0 lx, 18-bit range		0		count
t_{LS}	Measurement repetition period [d]	Programmable in 8 steps	25		2000	ms
t_{INT}	Measurement integration time [d]	Programmable in 6 steps	50		400	ms
G_1	Sensitivity at gain 1	Example for 3050 K, 5 klx LED light, 18-bit sensor resolution. Specification changes with the resolution setting as shown in Table 7.		C: 9160 R: 3160 G: 4280 B: 1470		counts
G_3	Sensitivity at gain 3			C: 27480 R: 9480 G: 12840 B: 4410		counts
G_6	Sensitivity at gain 6			C: 54960 R: 18960 G: 25680 B: 8820		counts
PS Proximity Sensor Characteristics						
RES_{PS_bit}	Measurement resolution	Depends on pulse width and number of LED pulses; see sections 7.9.12 and 7.9.13	10	15	16	bit
RES_{PS_irr}	Signal strength IR	125mA LED current; 8 pulse average; gain mode 1; 4.6cm round white reflective target [e] in 4.6cm distance	2830	3300	4030	counts
RES_{PS_red}	Signal strength Red		2300	2660	3200	counts
ALC_{max}	Ambient light cancellation			>100000		lx
N_{PULSE}	Number of LED pulses		1	8	32	
t_{PS}	Measurement period	Programmable in 8 steps		3.125 to 400		ms
t_{PS_pw}	Pulse width	Three possible settings; configur-able via register setting; see section 7.9.13		26		µs
				42		µs
				71		µs
	Analog crosstalk cancellation	Programmable 0 or 50% FS		50%		Full scale
	Digital crosstalk cancellation	Programmable: 0 to full signal level. For 16-bit resolution.	0		65535	count

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
PPG Characteristics						
RES_{PPG}	Measurement resolution		16	18	18	bit
A_{PPG}	Digital averaging factor		1		32	
t_{PPG}	Measurement period	Programmable in 8 steps		0.3125 to 20		ms
t_{PPG_pw}	Pulse width	Configurable via register setting; see section 7.9.32		130 247 481 949		µs
	IR counts	18% grey card reflector (6mm from top of package); sample under clear cover glass; 125mA LED current; 130µs LED on time; average over 100 samples per second.		28000		count
	Red counts			28000		count
	Analog crosstalk cancellation	Programmable 0 or 50% FS		50%		Full scale
	Sample rate accuracy vs. nominal		-2		2	%
Measurement Timing						
$t_{WAKE\text{-}STB}$	Wake-up time from Standby Mode	From Standby to Active Mode (measurement can start)		1.5		ms
t_{Start}	Start time from VDD apply to Standby Mode			10		ms
IR LED (LED1 Pin) Characteristics						
λ_{Peak}	Peak wavelength	I_{LED} = 100mA, T_A = 25°C		940		nm
$I_{IR\_LED\ (Max)}$	IR LED current	Programmable in 1024 steps		250		mA
Red LED (LED2 Pin) Characteristics						
λ_{Peak}	Peak wavelength	I_{LED} = 20mA, T_A = 25°C		700		nm
$I_{RED\_LED\ (Max)}$	Red LED current	Programmable in 512 steps		125		mA

[a] For the LS, the maximum duty cycle is selected with 100ms measurement time (default) and 100ms period at an illumination of 1000 lux.

[b] For the PS, 100ms measurement period, 42µs pulse width, 8 pulses, 15-bit resolution, and Gain Mode 1 are selected.

[c] Refer to Figure 16 for typical temperature dependence.

[d] Typical timing accuracy applied.

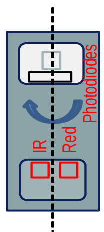
[e] 90 % reflective Kodak R-27.

6. Typical Performance Characteristics

Global measurement conditions V_{DD} = 2.8V, T_{AMB} = 25ºC, and default power-up settings, unless otherwise noted.

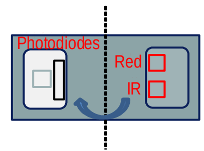
Figure 5. Package Rotation Axes for Field of View

Package Width



Applies to Figures
Figure 6
Figure 7
Figure 10

Package Length



Applies to Figures
Figure 8
Figure 9
Figure 11

Note: For Figure 6 through Figure 11, positive angle values apply to rotations where the respective right side of the package as shown in Figure 5 rotates upwards.

Figure 6. Typical FOV of R, G, B and Clear Photodiode along Width of Package

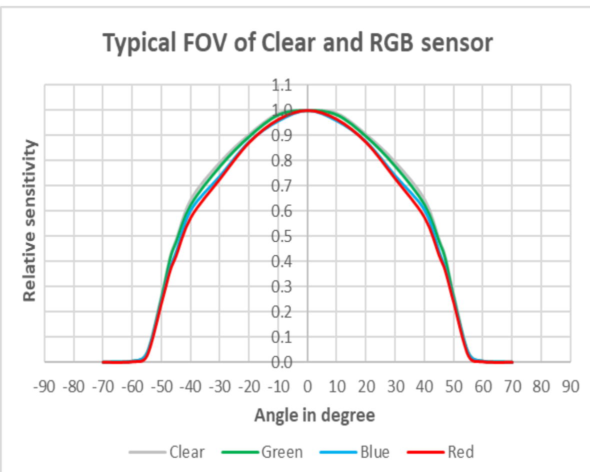


Figure 7. Typical FOV of PPG and Proximity Photodiode along Width of Package

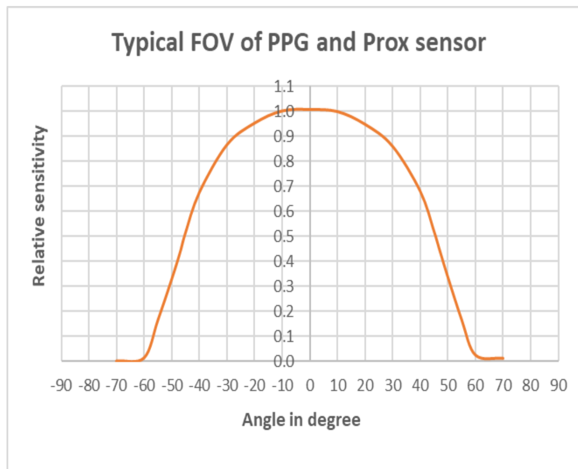


Figure 8. Typical FOV of R, G, B and Clear Photodiode along Length of Package

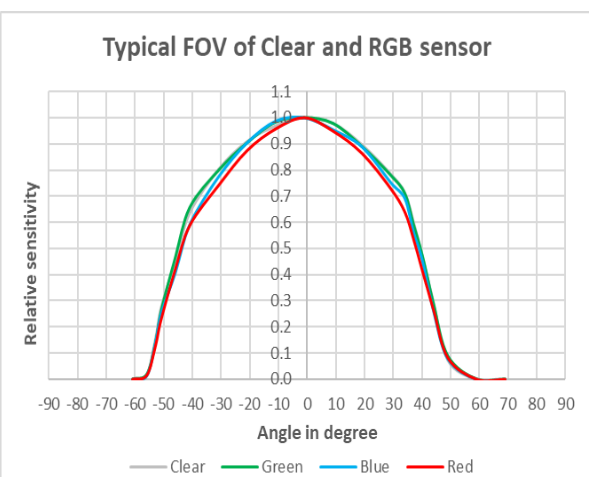


Figure 9. Typical FOV of PPG and Proximity Photodiode along Length of Package

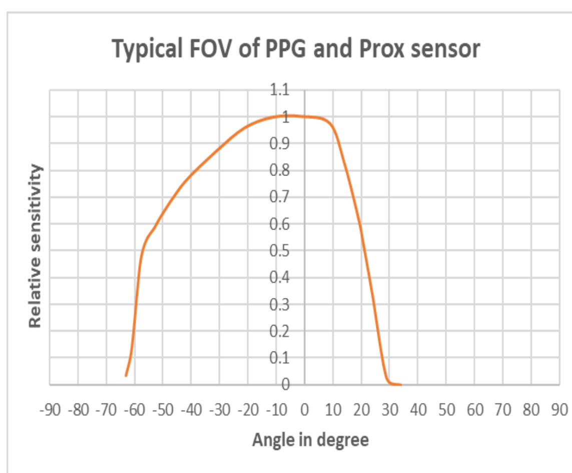


Figure 10. Typical Radiation Characteristic of the LEDs along Width of Package

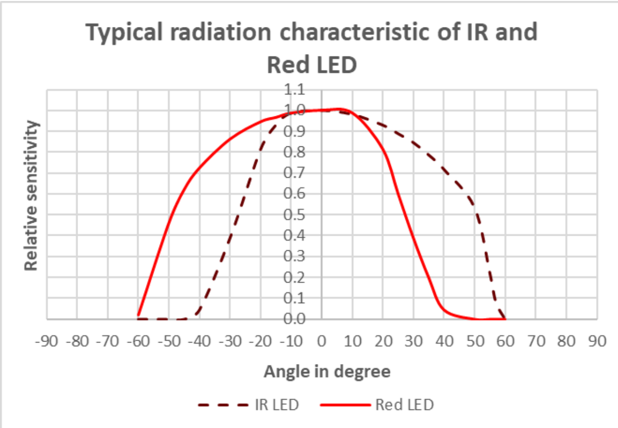


Figure 11. Typical Radiation Characteristic of the LEDs along Length of Package

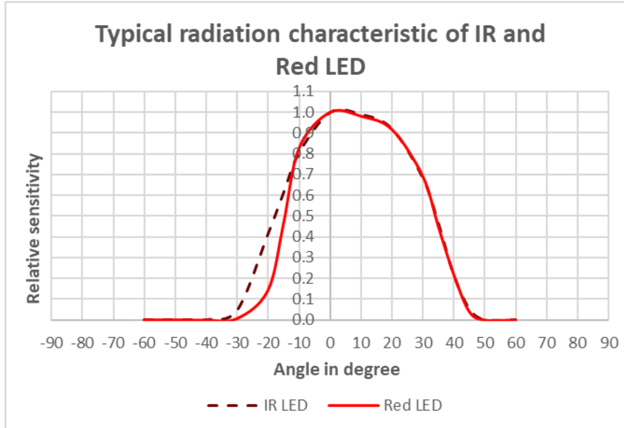


Figure 12. Typical Normalized Spectral Response of R, G, B and Clear Sensors

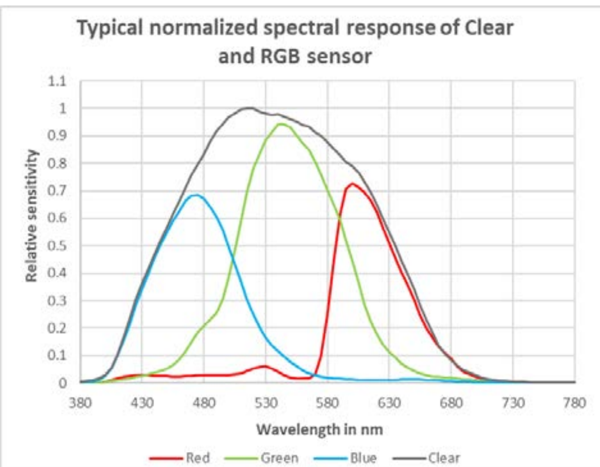


Figure 13. Typical Linearity of R, G, B and Clear Sensors

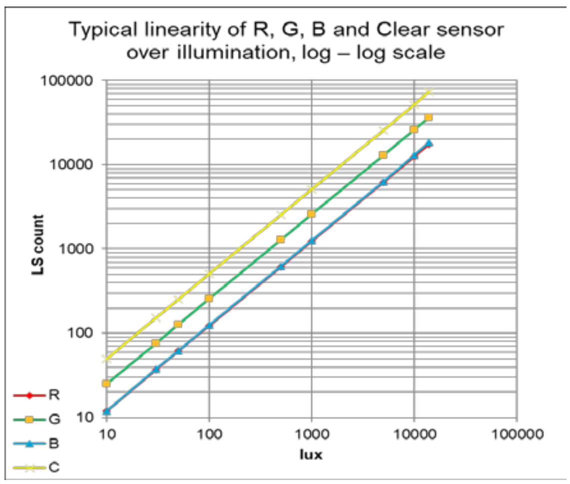


Figure 14. Typical PS Count over Distance

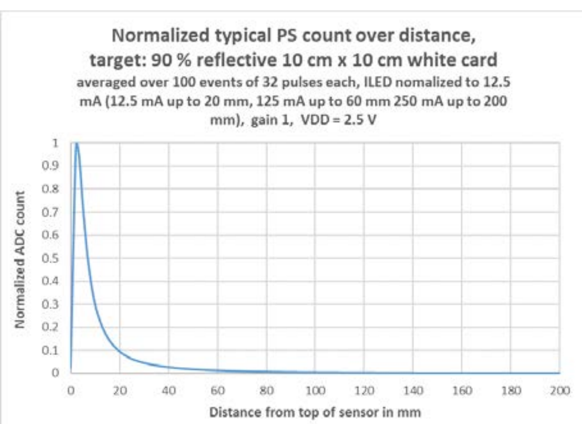


Figure 15. Log of Typical PS Count

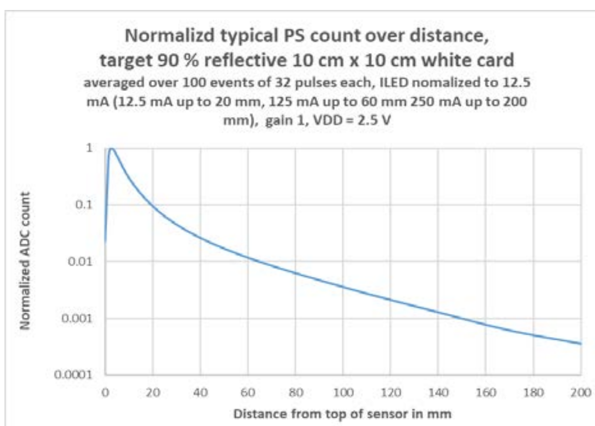


Figure 16. Typical Normalized Standby Current over Temperature

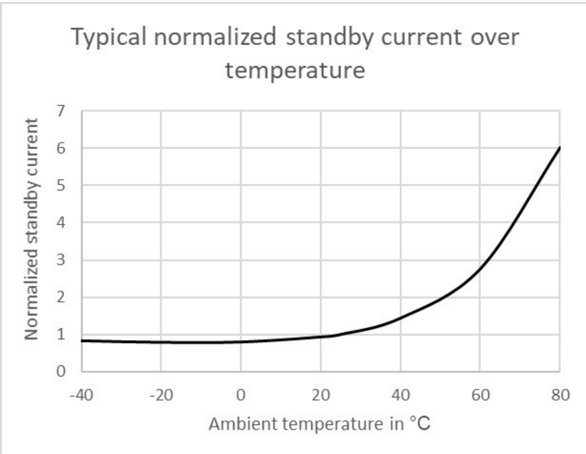


Figure 17. Typical Normalized LED Light Output Linearity with LED Current Register Settings

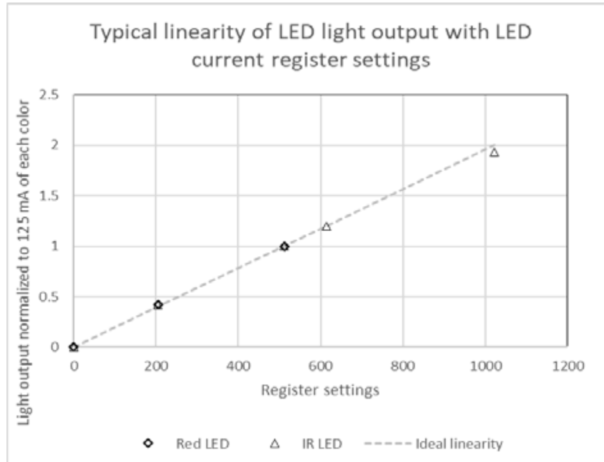


Figure 18. Typical LED Driver Current vs. Current Register Setting

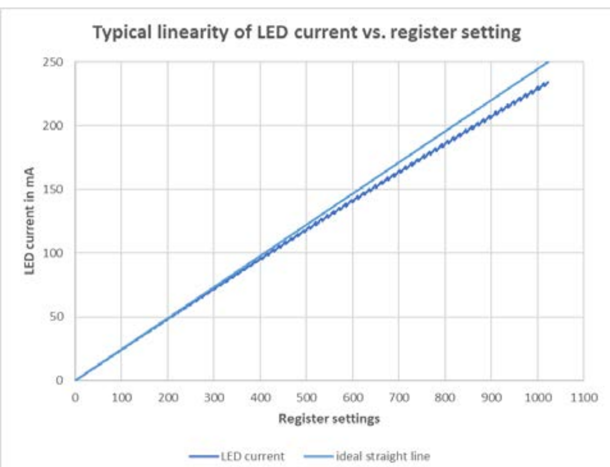
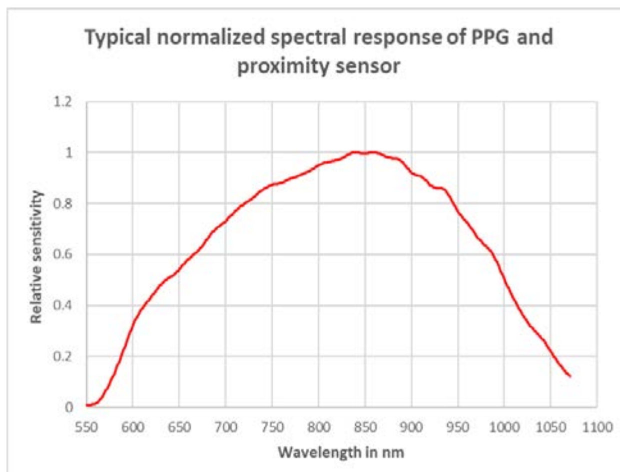


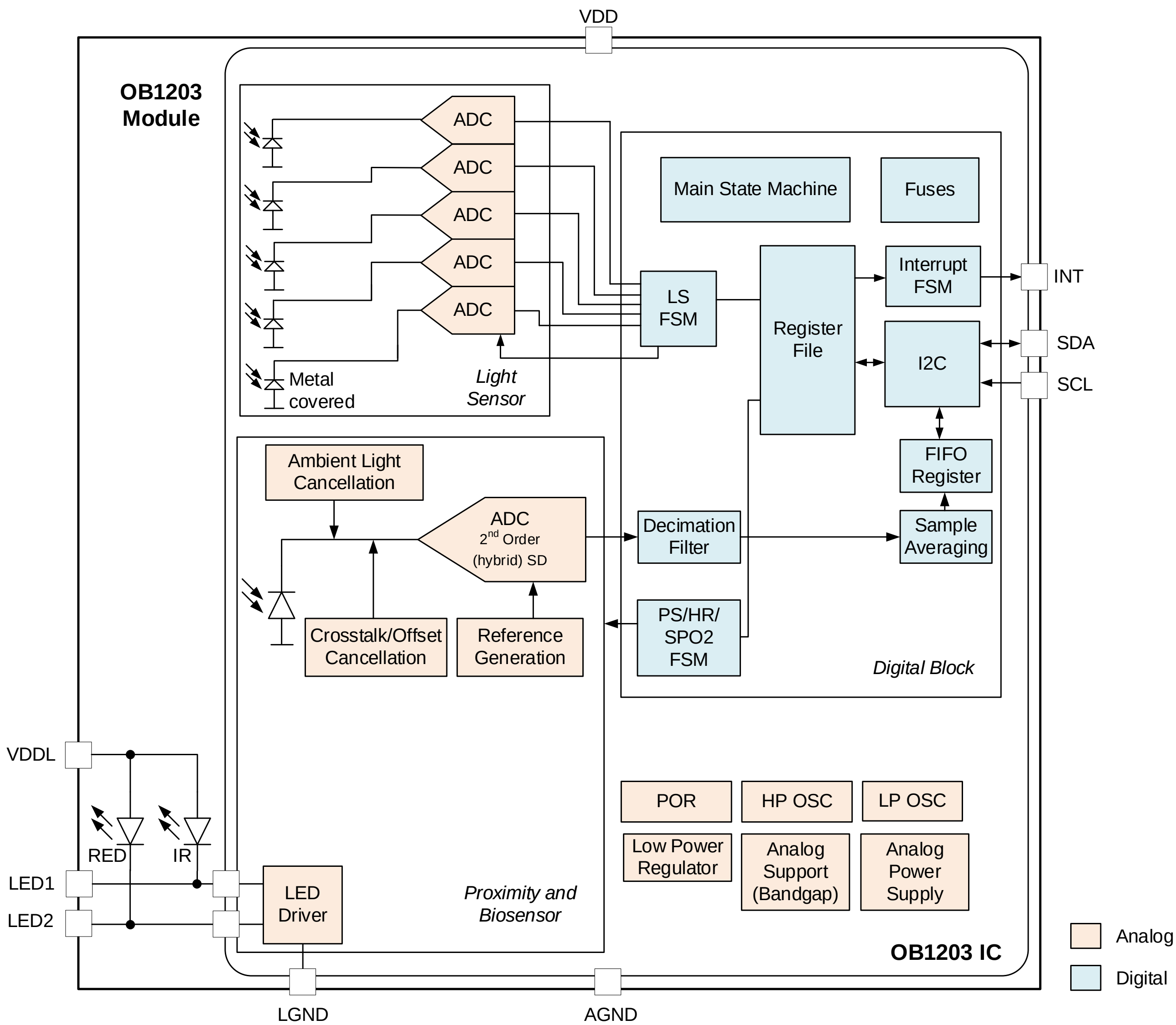
Figure 19. Typical Normalized Spectral Response of PPG and Proximity Sensor



7. Detailed Description

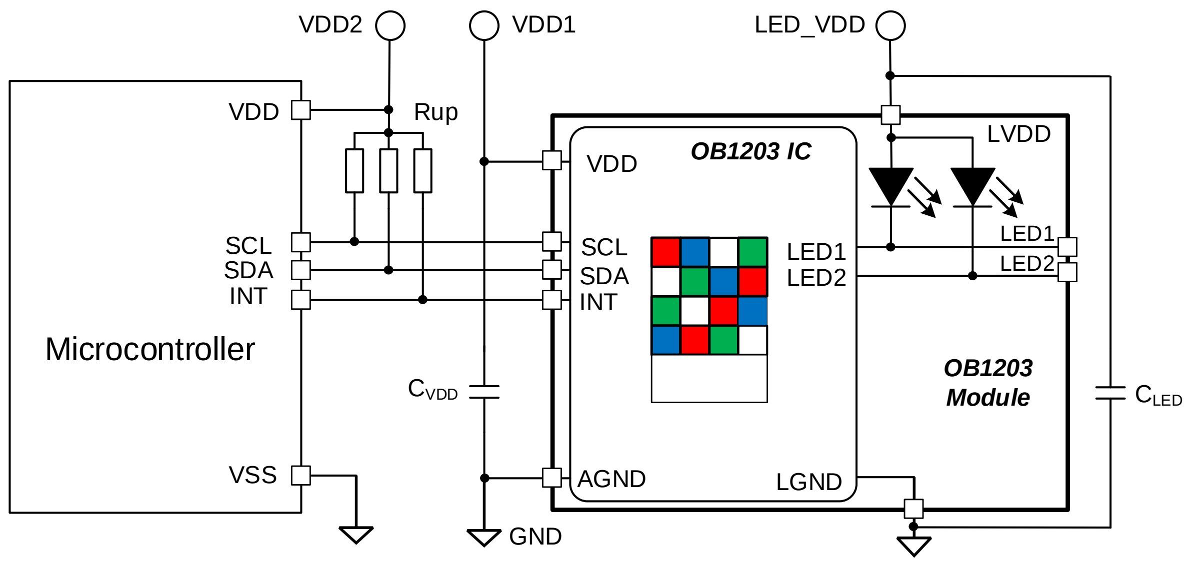
The OB1203 incorporates a sensor IC and two LEDs for excitation in the optical red and infrared range. The IC contains different photodiodes for light (R, G, B, and Clear channels) and proximity measurements as well as photoplethysmography. It also has photodiodes for temperature compensation of the light sensor. The sensor diodes are arranged in a matrix array while the single diode for PS/PPG measurement is located below the matrix. The photodiode current is converted to digital values by an analog-to-digital converter (ADC). The OB1203 also includes a current driver for the LEDs as well as some peripheral circuits, such as two internal oscillators, a current source, and voltage reference. It is trimmed and calibrated at final test using settings in nonvolatile memory (NVM).

Figure 20. Simplified Block Diagram



7.1 Application Circuit

Figure 21. Typical Application Circuit



7.2 Modes of Operation

Table 5. Channel Activation during Operation Modes

Mode Name[a]	LS		PS		IR PPG		Red PPG	
	Standby	Active	Standby	Active	Standby	Active	Standby	Active
Standby	✓		✓		✓		✓	
LS only		✓	✓		✓		✓	
PS only	✓			✓	✓		✓	
LS+PS		✓		✓	✓		✓	
PPG1	✓		✓			✓	✓	
PPG2	✓		✓			✓		✓

[a] All other mode combinations are prohibited and should not be used. Otherwise proper operation is not guaranteed.

7.3 Main State Machine

The main state machine is set to "Start State" during a power-on or software reset. As soon as the reset is released, the internal low power (LP) oscillator is started and the programmed I2C address and the trim values are read from the internal NVM trimming data block. The OB1203 enters Standby Mode as soon as the Idle State is reached (see Figure 22).

NOTE: If the I2C address has yet not been read, the device will respond with NACK to any I2C command and ignore any request in order to avoid responding to an incorrect I2C address.

The sensor mode is selected with the respective bits in the *MAIN_CTRL_0* (see section 7.9.9) or *MAIN_CTRL_1* register (see section 7.9.10; e.g., the LS_EN bit is set to 1. If any of the sensor operation modes are activated through an I2C command, the internal support blocks are immediately powered on. Once the voltages and currents are settled (typically after 1.5ms), the state machine checks for trigger events from a measurement scheduler to start conversions according to the selected measurement periods (see sections 7.9.13, 7.9.18, and 7.9.32).

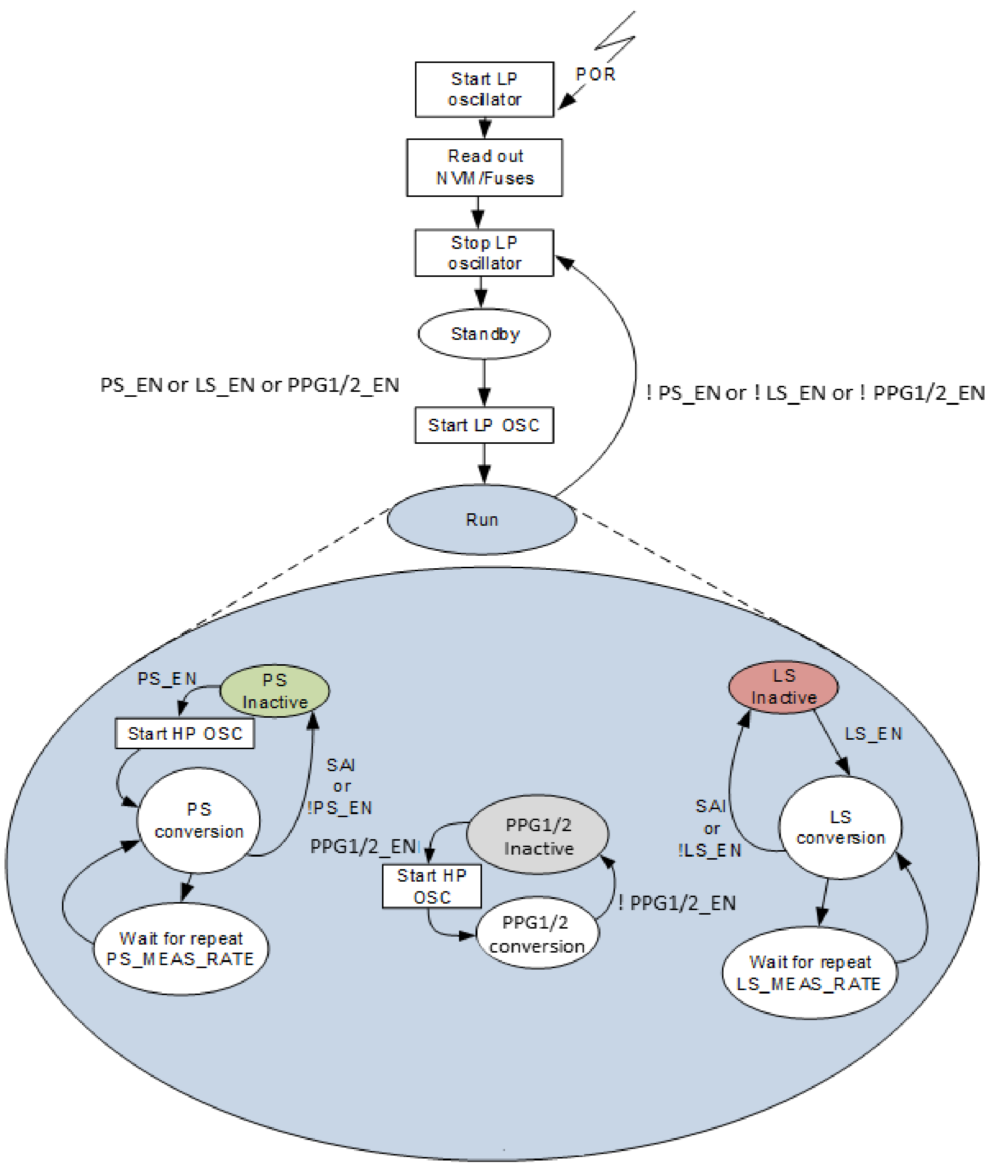
When the user resets the LS_EN bit (or the PPG_PS_EN bit) to '0,' a running conversion will be completed and the relevant ADCs will move to Standby Mode thereafter. The support blocks will only move to Standby Mode if all sensors are inactive.

If any of the sensors are programmed to "Sleep After Interrupt" (SAI) with the SAI bits in the *MAIN_CTRL_0* or *MAIN_CTRL_1* register, the relevant ADCs will move to Standby Mode after the interrupt condition occurs. Also the sensor enable bits LS_EN or PPG_PS _EN will be set following a read out of the corresponding status register *STATUS_0* or *STATUS_1*.

The deactivation of either LS or PPG/PS in the *MAIN_CTRL_0* or *MAIN_CTRL_1* registers will not clear the related status bits in the *STATUS_0* or *STATUS_1* register. They will always be reset upon activation of the respective sensor.

If no measurements are enabled, as on power-up, the OB1203 is automatically in Low-Power Standby Mode.

Figure 22. Simplified Main State Machine



7.4 Light Sensor Description

The light sensor (LS) can be operated independently and in parallel to the proximity sensor (PS). It can be configured to run in LS Mode (Green, Clear and Comp) or in CS mode (Red, Green, Blue, Clear, and Comp) (see Table 6). If the full CS functionality is not needed, LS Mode can be selected in the MAIN_CTRL_0 (15_{HEX}) register (see section 7.9.9).

The Comp channel receives data from a metal-covered photodiode used to measure dark current and compensate the readings of the light sensors for temperature changes.

Table 6. LS Channel Activation in LS and CS Mode

LS Mode	Red	Green	Blue	Clear	Comp
LS (LS_Mode = 0)		✓		✓	✓
CS (LS_Mode = 1)	✓	✓	✓	✓	✓

The OB1203 light sensor range and sensitivity are configured by the LS_RES_PERIOD register (22_{HEX}; see section 7.9.18) and LS_GAIN register (23_{HEX}; see section 7.9.19). The same gain and resolution (measurement time) settings are applied to the LS/CS channels. If different gain or resolution settings are required for different channels, conversions must be performed consecutively with modified settings.

Gain (i.e., 1x, 3x, 6x) sets the maximum light level that will saturate the sensor. Higher gain means a smaller maximum and minimum detectable signal.

Resolution sets the dynamic range, namely the number of counts that corresponds to the highest signal. Higher resolutions have a higher maximum number of counts and a correspondingly smaller least significant bit (higher sensitivity). Higher resolution is obtained by a longer integration (measurement) time.

For automatic gain control methods, if a channel is saturated or close to saturation, e.g. above 80% of max counts, the user application can decrease the gain. If the light level is less than about 20% for all sensors' readings, the user's application can increase the gain.

In order to make measurements at different resolutions and gains equivalent, appropriate scaling should be performed. An example calculation of lux given in Equation 1, Equation 2, and Equation 3 scales all measurements to the highest gain and highest resolution.

$$Lux = Gain_{scale}\, Res_{scale}\, (C_1R + C_2G + C_3B)$$ Equation 1

$$Gain_{scale} = \frac{6}{gain}$$ Equation 2

$$Res_{scale} = 2^{(20 - res)}$$ Equation 3

Where *gain* is 1, 3, or 6, *res* is 13, 16, 17, 18, 19, or 20 and C_1, C_2, and C_3 are application-specific color correction coefficients.

Table 7. LS Detection Ranges and Sensitivity Calculation Example

			Gain[a] 1		Gain 3		Gain 6	
Resolution [bits]	Measurement Time [ms]	Maximum Counts	Sensitivity	Range (Detectable Light Levels)	Sensitivity	Range	Sensitivity	Range
13	3.125	8191	1x	6x	3x	3x	6x	1x
16	25	65535	8x	6x	24x	3x	48x	1x
17	50	131071	16x	6x	48x	3x	96x	1x
18 (default)	100	262143	32x	6x	96x	3x	192x	1x
19	200	524,288	64x	6x	192x	3x	384x	1x
20	400	1,048,575	128x	6x	384x	3x	768x	1x

7.5 Proximity and PPG Sensor Description

The proximity and PPG sensor measures the amount of reflected energy in the red and infrared range from a target object using the LED cathode/driver outputs on the LED2 and LED1 pins, respectively. The transmitter is realized with an infrared LED (peak wavelength of approximately 940nm) and a red LED (peak wavelength of approximately 700nm) that are integrated in the OB1203 module.

The photodiode is integrated on-chip. Its analog output signal is converted to a digital value by an integrated ADC. The conversion result is stored in an output register that can be read via the I2C bus. There are four gain modes to adjust the PS/PPG sensitivity of the OB1203 to the needs of the application.

Ambient light influence is suppressed by default (ambient light cancellation). To reduce the influence of crosstalk of reflected LED light behind a cover glass or from the skin surface, the OB1203 has an analog crosstalk cancellation built in. This function can subtract a DC offset signal before the analog-to-digital conversion and therefore avoids reduction in the sensor's dynamic range by optical crosstalk or unwanted optical back scatter. For further details, see the *OB1203 Application Note – PS/PPG Crosstalk Cancelation*. The value of the DC offset signal is accessible via a register each for the PPG and PS measurements. The external application must determine the appropriate cancelation values prior to the start of the measurement. After AD conversion but before the interrupt threshold comparison, the PS Mode allows an additional digital crosstalk reduction (see 7.5.2).

7.5.1 LEDs and Integrated LED Driver

The built-in LEDs are controlled via the integrated LED driver of the OB1203. The LED intensity can be adjusted by the LED current (refer to Table 4). The LED currents are adjustable in register *PS_LED_CURR* for PS and *PPG_IRLED_CURR*/*PPG_RLED_CURR* for PPG independently (sections 7.9.11, 7.9.28, and 7.9.29).

7.5.2 Principles of Proximity Sensor Operation

The proximity sensor can be operated independently and in parallel with the light sensor. By default, the IR LED (LED1 pin) is used as the transmitter. The PS gain is adjustable in four steps with the *PPG_PS_GAIN* register (see section 7.9.26).

The timing is programmable by defining the number of LED pulses N_{PULSES}, the pulse width t_{PS_pw}, and the measurement period t_{PS} (refer to Figure 23 and Table 8) in the *PS_PWIDTH_PERIOD* register; see section 7.9.13. The pulse repetition period t_{PS_pr} depends on the pulse width t_{PS_pw}.

An analog cancellation that allows a rough adjustment without loss of dynamic range for the PS is accessible with the *PS_CAN_PULSES* register; see section 7.9.30. A digital crosstalk cancellation can be used for fine adjustments (see sections 7.5 and 7.9.12). The digital cancellation value is automatically subtracted from the PS conversion result.

To improve PS data noise, the moving average and hysteresis features can be activated in the *PS_MOV_AVG_HYS* register; refer to section 7.9.15.

Figure 23. PS Timing Characteristic

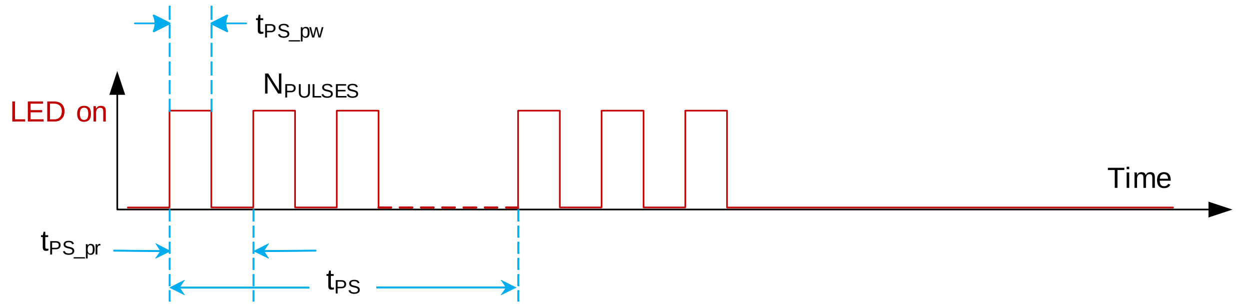


Table 8. PS Parameter

Setting	Symbol	Range of settings
Number of LED pulses [a]	N_{PULSES}	1 to 32
Measurement period	t_{PS}	3.125ms to 400ms
Pulse width	t_{PS_pw}	26µs | 42µs | 71µs
Pulse repetition period	t_{PS_pr}	89µs | 118µs | 176µs

[a] For measurement periods of 3.125ms and pulse widths above 26µs, the number of LED pulses is limited to 16.

7.5.3 Principles of PPG Sensor Operation

The PPG sensor can operate with two modes: PPG1 and PPG2. For PPG1 Mode, only LED1 (the IR LED) is used by default. This mode allows determination of parameters related to heart rate with an appropriate algorithm. The PPG2 Mode also uses LED2 (the Red LED) as a transmitter. This mode supports further analysis, such as SpO_2 and respiration rate determination. By (temporarily) enabling the LED_FLIP bit during the measurement, it is possible to use the red LED for PPG1 Mode; see section 7.9.27. Hence, an optical feedback on the correct positioning of the person's finger can be provided. Furthermore HR determination with the red LED instead of the IR LED is supported.

The timing is programmable by defining the pulse width t_{PPG_pw} and the measurement period T_{PPG} (see Figure 24 and Table 9) via changing register *PPG_PWIDTH_PERIOD*; see section 7.9.32. The pulse repetition period t_{PPG_pr} depends on the pulse width t_{PPG_pw}.

The influence of reflected light from the skin surface may be reduced by using the analog crosstalk cancellation. This modification is available via a setting in the register *PPG_CAN_ANA*, see section 7.9.30.

An averaging function can be applied to improve the signal to noise ratio and to reduce the data rate of the PPG data obtained. The number of samples averaged is programmable via the *PPG_AVG* register (see section 7.9.31).

Figure 24. PPG Timing Characteristic (without Averaging)

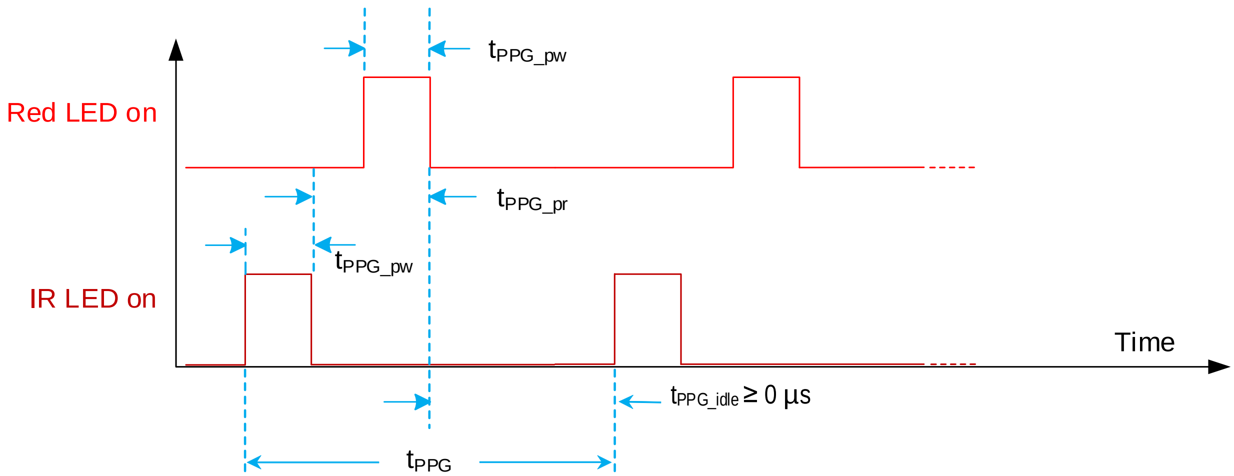


Table 9. PPG Parameters

Note: Not all combinations of settings are valid. For details, see section 7.9.32.

Setting	Symbol	Range of Settings
Measurement period	t_{PPG}	0.3125ms to 20ms
Pulse width	t_{PPG_pw}	130µs to 949µs
Pulse repetition period	t_{PPG_pr}	294µs to 1934µs

The PPG data is stored in a FIFO register. The FIFO consists of 32 words of 3 bytes each, so the FIFO can hold up to 32 samples of PPG1 measurement data or 16 sample pairs of PPG2 measurement data. In PPG2 Mode, the IR LED (LED1) data is written to the FIFO first followed by the result of the red LED (LED2) by default. The FIFO register read out via the I2C register *FIFO_DATA* has special features to enable reliable, time-resolved PPG measurements; see section 7.7.2.

The FIFO Write Pointer, FIFO Read Pointer, and FIFO Overflow Counter help to control the readout without losing samples. The FIFO Write Pointer contains the FIFO index where the next sample of PPG data will be written in the FIFO (see section 7.9.34). The FIFO Read Pointer contains the FIFO index of the FIFO register (of the first data which has not been read) (section 7.9.35). The FIFO Overflow Counter (see section 7.9.36) counts the number of lost or overwritten samples if the FIFO Rollover Enable is set (see section 7.9.33).

The FIFO_DATA ($3B_{HEX}$; see section 7.9.37) data register is special, providing access to an internal RAM that stores the biosensor data. Successive reads of the FIFO_DATA register are indexed through the RAM, not the register map. To access registers beyond $3B_{HEX}$, a write operation to a register beyond $3B_{HEX}$ must be performed.

It is necessary for the FIFO_DATA register to be read in a single burst (a.k.a. “block”) read. To read one data word (of 18 bits), a 3-byte block read at the address $3B_{HEX}$ must be performed. For the read of *n* words a 3*n* byte block read can be performed.

Several readout scenarios depending on the demands of the application are supported by using the “FIFO almost full interrupt” and “PPG data interrupt” settings; see section 7.6.3.

By default, in the event of a full FIFO, no further samples of PPG data are written into the FIFO. If the FIFO Rollover Enable bit (refer to section 7.9.33) is set to 1, when the FIFO is full, new PPG data will overwrite old data in the FIFO.

7.6 Interrupt Features

The OB1203 can generate independent LS, PS, and PPG interrupt signals. LS and PS interrupts will be triggered if the upper or lower threshold values are crossed. The PPG interrupts notify on the availability of new PPG data and on an adjustable number of free FIFO registers remaining during a PPG measurement.

Another feature is the option to deactivate a sensor after an interrupt event occurs by setting the *Sleep After Interrupt* bit in the respective *MAIN_CTRL_0* or *MAIN_CTRL_1* register (*SAI_LS* and *SAI_PS* for light and proximity sensors respectively). This feature is independently available for both the PS and LS/CS sensors.

The LS and PS persistence settings determine the number of consecutive samples that must be measured before the interrupt is asserted.

For LS, an interrupt can also be triggered if the output count variation of consecutive conversions has exceeded a defined limit.

The PS Logic Output Mode allows the interrupt pin to show whether objects are near or far. If the PS Logic Output Mode is set, then no other interrupts will be asserted.

All interrupt signals as well as *ps_logic_mode* are active low at the INT pin.

Clearing the interrupt status flag by reading the status register will also clear the interrupt signal on the INT pin except in the PS Logic Output Mode.

7.6.1 LS Interrupt

The LS interrupt functionality is configured by the bits in the *INT_CFG_0* register (see section 7.9.23). It can function as either threshold triggered (LS_VAR_MODE = 0) or variance trigged (LS_VAR_MODE = 1).

The LS_INT_SEL bits in the *INT_CFG_0* register configure which of the LS/CS channels (Clear, Green, Red or Blue) will be compared with the interrupt thresholds.

The threshold interrupt is enabled with LS_INT_EN = 1 and LS_VAR_MODE = 0. The interrupt is set when the respective **_DATA* register of the selected interrupt source channel is above the upper or below the lower threshold configured in the *LS_THRES_UP* and *LS_THRES_LOW* registers (see sections 7.9.20 and 7.9.21 respectively) for a specified number of consecutive measurements as configured in the *INT_PST* register (1 + LS_PERSIST) (see section 7.9.25).

The variance interrupt is enabled with LS_INT_EN = 1 and LS_VAR_MODE = 1. It is set when the absolute value difference between the preceding and the current output data of the selected interrupt source channel is above the variance threshold.

In Variance Mode if LS_PERSIST > 0 (see section 7.9.25), each measurement must differ from the previous by the specified variance (any combination of up and down changes). LS_PERSTIST > 0 is not recommended in Variance Mode.

7.6.2 PS Interrupt

The interrupt is configured by the bits in the *INT_CFG_1* register (see section 7.9.24) and enabled with *PS_INT_EN = 1*.

The bit *PS_LOGIC_MODE* in the *INT_CFG_1* register further defines the behavior of the interrupt.

PS_LOGIC_MODE = 0: The interrupt is set (interrupt pin to ground and the status bits to 1) after each measurement when the *PS_DATA* is above the upper threshold configured in the *PS_THRES_UP* register (see section 7.9.16).

The interrupt is also set (interrupt pin to ground and the status bits to 1) after each measurement when the *PS_DATA* is below the lower threshold configured in the *PS_THRES_LOW* (see section 7.9.17).

The interrupt is cleared (interrupt pin to high; status bit to zero) when the STATUS or PS DATA registers are read or the data measurement is between the two thresholds.

For *PS_PERSIST* > 0, the interrupts occur only after a specified number of consecutive measurements above or below the respective thresholds, as configured in the *INT_PST* register (1 + PS_PERSIST) (see section 7.9.25).

To obtain interrupts whenever new data is available, set the upper threshold below the lower threshold and PS_PERSIST = 0.

Interrupt pin and *PS_interrupt_status* bit:	Reset by *STATUS_1* register read (see section 7.9.2)
PS_data_status bit:	Reset by data register read
PS_logic_signal_status bit:	Reset by interrupt condition (signal below lower threshold)

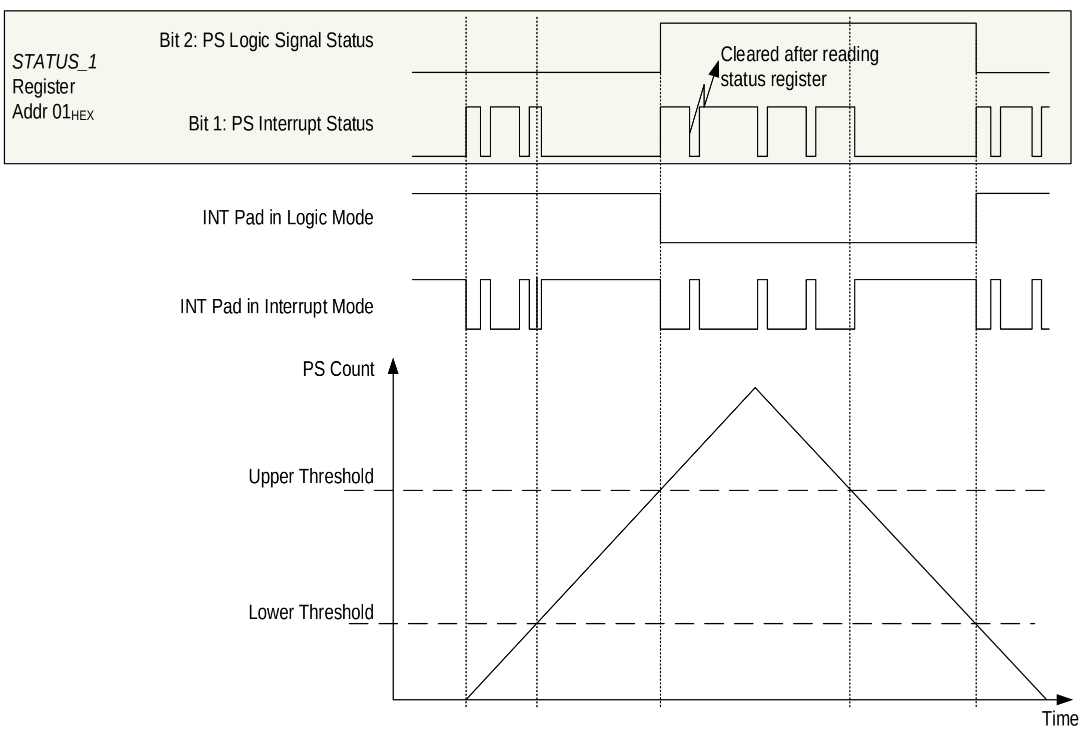
PS_LOGIC_MODE = 1: The interrupt and the status bits in the *STATUS_1* register are set (interrupt pin to ground) when the *PS_DATA* content is above the upper threshold configured in the *PS_THRES_UP* register and held until the *PS_DATA* drops below the lower threshold configured in the *PS_THRES_LOW* register. For the PS logic status bit, a set interrupt is equal to the Near Mode (strong reflective signal, object close), while a weak signal (no interrupt) is the Far Mode (object far away).

For PS_PERSIST > 0, the interrupt changes only after a specified number of consecutive measurements above or below the respective thresholds, as configured in the *INT_PST* register (1 + PS_PERSIST) (see section 7.9.25).

PS_interrupt_status bit:	Reset by *STATUS_1* register read
PS data status bit:	Reset by data register read
Interrupt pin and *PS logic status* bit:	Reset by interrupt condition (signal below lower threshold)

The PS interrupt generator is shown in the upper part of Figure 25. An example of the interrupt behavior is shown in Figure 25.

Figure 25. PS Interrupt Behavior Examples



Note: The *STATUS_0* and *STATUS_1* registers should be read out immediately after an interrupt transition has occurred on the INT pin. As the interrupts are not reset automatically, an interrupt event caused by crossing the opposite threshold could be missed.

7.6.3 PPG Interrupt

The *FIFO_almost_full* interrupt is enabled by setting the *A_FULL_INT_EN* bit in register *INT_CFG_1* to '1' (see section 7.9.24). It is triggered when a certain number of free FIFO registers are remaining. This number can be configured in register *FIFO_CFG* (see section 7.9.33). The status bit of the *FIFO almost full* interrupt in the *STATUS_1* register is set even if the interrupt pin is disabled. The status bit *FIFO almost full interrupt* is cleared by reading the *STATUS_1* register or reading the *FIFO_DATA* register.

The PPG data interrupt is enabled by setting the *PPG_INT_EN* bit in register *INT_CFG_1* to '1' (see section 7.9.24). It is triggered when a new sample of PPG measurement data is available in the FIFO. The *PPG data status* bit is set even if the interrupt pin is disabled. The *PPG data status* bit is cleared by reading the *STATUS_1* register or reading the *FIFO_DATA* register.

7.7 I2C Interface

The OB1203 is equipped with an I2C interface for control and data communication. The chip always operates as a slave. A read/write bit must be appended to the slave address by the master device to properly communicate with the device.

The interface is compatible with Standard Mode (100kHz) and Fast Mode (400kHz) I2C communication.

Table 10. Supported I2C clock Frequencies

Mode	Frequency	Transient Noise Filter
Standard	100kHz	50ns
Fast	400kHz	50ns

The I2C circuitry is always active (Standby or Active Mode of the OB1203). If the I2C address is not yet read from the memory block, the device will respond with "NACK" to any request and ignore the possible commands. An attempt to read or write to non-existing addresses will be answered with "NACK."

7.7.1 I2C Address Decoding

The 7 bit I2C address of the device is 53_{HEX}. Appending the write / read bit yields $A6_{HEX}$ for write and $A7_{HEX}$ for read in the I2C address command.

7.7.2 I2C Register Read

The OB1203 registers can be read individually or in Block Read Mode. If the last valid address (51_{HEX}) has been reached, but the master continues with the block read, the address counter in the OB1203 will not roll over and the OB1203 returns 00_{HEX} for every subsequent byte read.

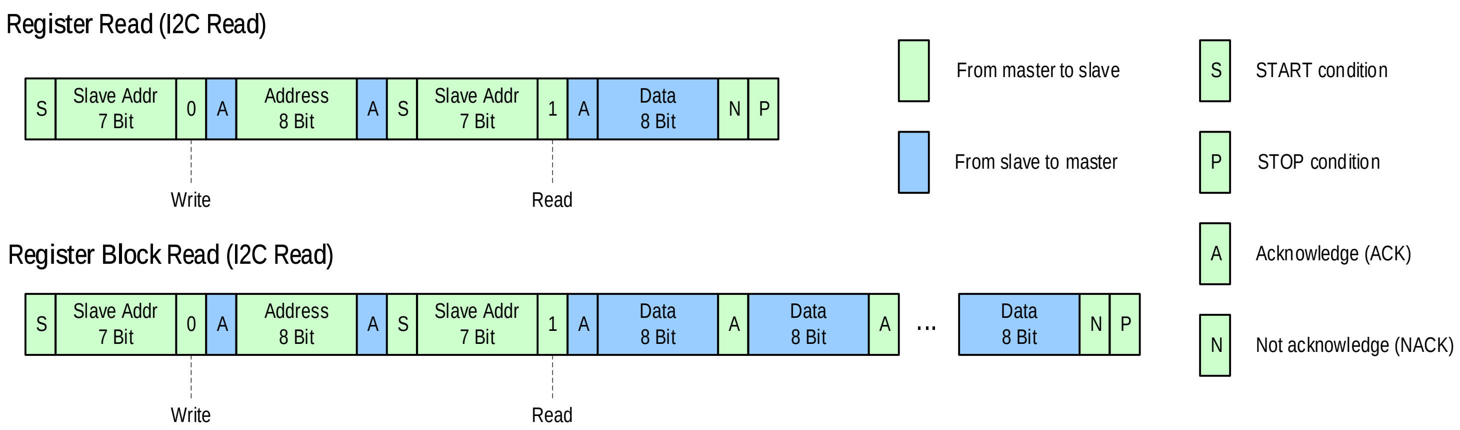
The block read operation is the only way to ensure correct data read out of multi-byte data registers and to avoid splitting of results with HIGH and LOW bytes originating from different conversions. If an I2C read operation is active, all registers are locked until the I2C read operation is completed. This guarantees that the data in the LS/PS data and status registers come from the same measurement even if an additional measurement cycle ends during the read operation. New measurement data is stored into temporary registers and the I2C **_DATA* registers are updated as soon as there is no on-going I2C read operation.

The *FIFO_DATA* register (see section 7.9.37) behaves differently from all other readable registers. Reading the *FIFO_DATA* register does not increment the register address. A block read from this register reads this address again and again. However the *FIFO_RD_PTR* register is incremented after reading a sample consisting of 3 bytes and so the FIFO can be read byte-by-byte. To continue I2C register reads after *FIFO_DATA*, a new command with the address of this register must be sent before the data from this and the following registers can be read. See section 7.9.37 for more details.

If a read access is started on an address outside the valid address range, the OB1203 will return NACK until the I2C operation is ended.

Read operations must follow the timing diagram in Figure 26.

Figure 26. I2C Register Read



7.7.3 I2C Register Write

The OB1203 registers can be written to individually or in Block Write Mode. If a register includes read (R) and read/write (RW) bits, data written to read-only bits are ignored.

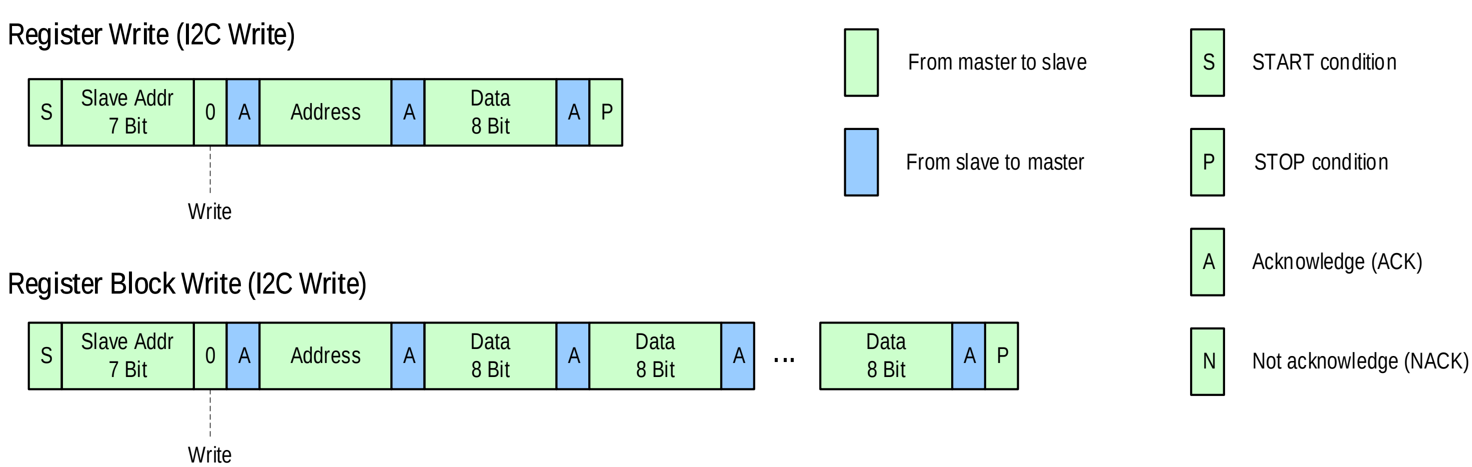
If the last valid address (51_{HEX}) of the OB1203 address range is reached but the master attempts to continue the block write operation, the address counter of the OB1203 will not roll over. The OB1203 will return NACK for every following byte sent by the master until the I2C operation is ended.

If a write access is started on an address outside the valid address range, the OB1203 will return NACK until the I2C operation is ended.

Some register bits are R/W and must be set to a specific value 0 or 1 as indicated in the register map.

Write operations must follow the timing diagram in Figure 27.

Figure 27. I2C Register Write



7.7.4 I2C Interface Bus Timing

Figure 28. Bus Timing

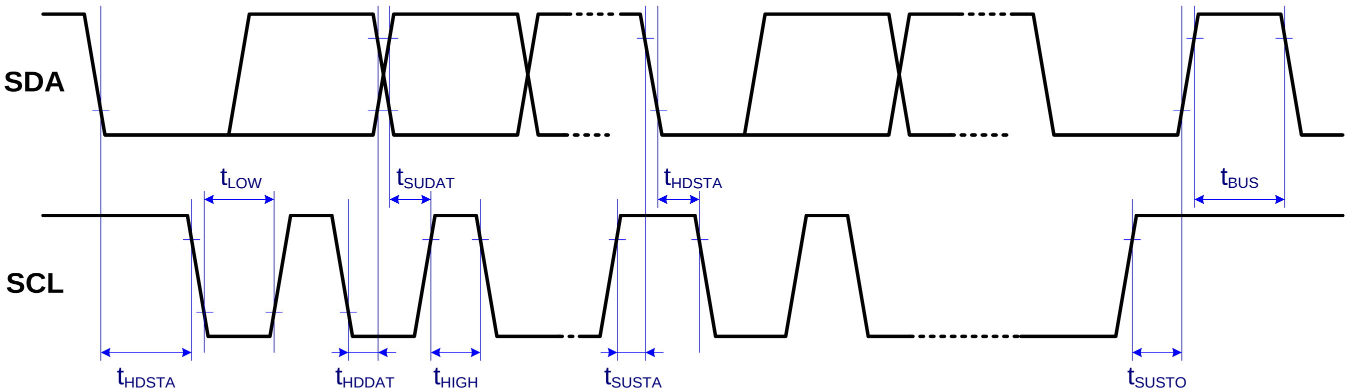


Table 11. Bus Timing Characteristic

Parameter	Symbol	Standard Mode	Fast Mode	Units
Maximum SCL clock frequency	f_{SCL}	100	400	kHz
Minimum START condition hold time relative to SCL edge	t_{HDSTA}	4		µs
Minimum SCL clock low width	t_{LOW}	4.7		µs
Minimum SCL clock high width	t_{HIGH}	4		µs
Minimum START condition setup time relative to SCL edge	t_{SUSTA}	4.7		µs
Minimum data hold time on SDA relative to SCL edge	t_{HDDAT}	0		µs
Minimum data setup time on SDA relative to SCL edge	t_{SUDAT}	0.1	0.1	µs
Minimum STOP condition setup time on SCL	t_{SUSTO}	4		µs
Minimum bus free time between stop condition and start condition	t_{BUS}	4.7		µs

7.8 Summary of Internal Registers

Table 12. Register Map

Address	Type	Name	Default Value	Description
00_{HEX}	R	STATUS_0	80_{HEX}	Power-on status, LS interrupt, and LS data status
01_{HEX}	R	STATUS_1	00_{HEX}	PPG/PS data status, PS/PPG interrupt status
02_{HEX}	R	PS_DATA_0	00_{HEX}	PS measurement data, LSB
03_{HEX}	R	PS_DATA_1	00_{HEX}	PS measurement data, MSB
04_{HEX}	R	LS_CLEAR_DATA_0	00_{HEX}	LS Clear measurement data, LSB
05_{HEX}	R	LS_CLEAR_DATA_1	00_{HEX}	LS Clear measurement data intervening bits
06_{HEX}	R	LS_CLEAR_DATA_2	00_{HEX}	LS Clear measurement data, MSB

Address	Type	Name	Default Value	Description
07HEX	R	LS_GREEN_DATA_0	00HEX	LS Green/LS measurement data, LSB
08HEX	R	LS_GREEN_DATA_1	00HEX	LS Green/LS measurement data intervening bits
09HEX	R	LS_GREEN_DATA_2	00HEX	LS Green/LS measurement data, MSB
0AHEX	R	LS_BLUE_DATA_0	00HEX	LS Blue measurement data, LSB
0BHEX	R	LS_BLUE_DATA_1	00HEX	LS Blue measurement data intervening bits
0CHEX	R	LS_BLUE_DATA_2	00HEX	LS Blue measurement data, MSB
0DHEX	R	LS_RED_DATA_0	00HEX	LS Red measurement data, LSB
0EHEX	R	LS_RED_DATA_1	00HEX	LS Red measurement data intervening bits
0FHEX	R	LS_RED_DATA_2	00HEX	LS Red measurement data, MSB
10HEX	R	COMP_DATA_0	00HEX	LS Comp measurement data, LSB
11HEX	R	COMP_DATA_1	00HEX	LS Comp measurement data intervening bits
12HEX	R	COMP_DATA_2	00HEX	LS Comp measurement data, MSB
15HEX	R/W	MAIN_CTRL_0	00HEX	LS operation mode control, software (SW) reset
16HEX	R/W	MAIN_CTRL_1	00HEX	PPG/PS operation mode control
17HEX	R/W	PS_LED_CURR_0	FFHEX	PS LED current, LSB
18HEX	R/W	PS_LED_CURR_1	01HEX	PS LED current, MSB
19HEX	R/W	PS_CAN_PULSES	1AHEX	PS analog cancellation level and pulse setting
1AHEX	R/W	PS_PWIDTH_PERIOD	15HEX	PS pulse width and measurement period
1BHEX	R/W	PS_CAN_DIG_0	00HEX	PS digital cancellation level setting, LSB
1CHEX	R/W	PS_CAN_DIG_1	00HEX	PS digital cancellation level setting, MSB
1DHEX	R/W	PS_MOV_AVG_HYS	00HEX	PS moving average and hysteresis configuration
1EHEX	R/W	PS_THRES_UP_0	FFHEX	PS interrupt upper threshold, LSB
1FHEX	R/W	PS_THRES_UP_1	FFHEX	PS interrupt upper threshold, MSB
20HEX	R/W	PS_THRES_LOW_0	00HEX	PS interrupt lower threshold, LSB
21HEX	R/W	PS_THRES_LOW_1	00HEX	PS interrupt lower threshold, MSB
22HEX	R/W	LS_RES_PERIOD	22HEX	LS resolution and measurement period setting
23HEX	R/W	LS_GAIN	01HEX	LS analog gain range setting
24HEX	R/W	LS_THRES_UP_0	FFHEX	LS interrupt upper threshold, LSB
25HEX	R/W	LS_THRES_UP_1	FFHEX	LS interrupt upper threshold, intervening bits
26HEX	R/W	LS_THRES_UP_2	0FHEX	LS interrupt upper threshold, MSB
27HEX	R/W	LS_THRES_LOW_0	00HEX	LS interrupt lower threshold, LSB
28HEX	R/W	LS_THRES_LOW_1	00HEX	LS interrupt lower threshold, intervening bits
29HEX	R/W	LS_THRES_LOW_2	00HEX	LS interrupt lower threshold, MSB
2AHEX	R/W	LS_THRES_VAR	00HEX	LS interrupt variance threshold

Address	Type	Name	Default Value	Description
$2B_{HEX}$	R/W	INT_CFG_0	10_{HEX}	LS interrupt configuration
$2C_{HEX}$	R/W	INT_CFG_1	00_{HEX}	PS/PPG interrupt configuration
$2D_{HEX}$	R/W	INT_PST	00_{HEX}	LS/PS interrupt persist setting
$2E_{HEX}$	R/W	PPG_PS_GAIN	09_{HEX}	PPG/PS gain setting
$2F_{HEX}$	R/W	PPG_PS_CFG	40_{HEX}	PPG power save and LED flip setting
30_{HEX}	R/W	PPG_IRLED_CURR_0	00_{HEX}	PPG IR LED (LED1) current, LSB
31_{HEX}	R/W	PPG_IRLED_CURR_1	00_{HEX}	PPG IR LED current, MSB
32_{HEX}	R/W	PPG_RLED_CURR_0	00_{HEX}	PPG Red LED (LED2) current, LSB
33_{HEX}	R/W	PPG_RLED_CURR_1	00_{HEX}	PPG Red LED current, MSB
34_{HEX}	R/W	PPG_CAN_ANA	00_{HEX}	PPG analog cancellation value
35_{HEX}	R/W	PPG_AVG	$0A_{HEX}$	Number of averaged PPG samples
36_{HEX}	R/W	PPG_PWIDTH_PERIOD	42_{HEX}	PPG pulse width and measurement period
37_{HEX}	R/W	FIFO_CFG	00_{HEX}	FIFO rollover and almost full configuration
38_{HEX}	R/(W)	FIFO_WR_PTR	00_{HEX}	FIFO write pointer
39_{HEX}	R/(W)	FIFO_RD_PTR	00_{HEX}	FIFO read pointer
$3A_{HEX}$	R/(W)	FIFO_OVF_CNT	00_{HEX}	FIFO overflow counter
$3B_{HEX}$	R	FIFO_DATA	00_{HEX}	FIFO mirrored PPG data
$3D_{HEX}$	R	PART_ID	TBD	Part number ID

7.9 Detailed Description of Registers

7.9.1 STATUS_0

Address	00_{HEX}
Default value	80_{HEX}
Register access	R

Bit	7	6	5	4	3	2	1	0
00_{HEX}	Power-On_ status	0	0	0	0	0	LS_interrupt_ status	LS_data_ status

Bit[7] *Power-On_ status:*
If set to 1, the part has had a power-up event, either because the part was turned on or because there was a power-supply voltage disturbance

A value of 1 is the default for the first register read after power-on reset.

Note: All interrupt threshold settings in the registers have been reset to power-on default states and should be examined if the *Power-On status* flag is set.

The flag is cleared after the register is read.

Bit[1] *LS_ interrupt_status:* (updated even if the interrupt pin is disabled)

0	Interrupt condition has not occurred (**default**)
1	Interrupt condition has occurred (cleared after read)

Bit[0] *LS_data_status:*

0	Old data, already read (**default**)
1	New data, not yet read (cleared after read)

7.9.2 STATUS_1

Address 01HEX

Default value 00HEX

Register access R

Bit	7	6	5	4	3	2	1	0
01HEX	TS_data_status	X	FIFO_almost_ full_interrupt	PPG_data_ status	0	PS_logic_signal _status	PS_interrupt_ status	PS_data_status

Bit[7] *TS_data_status:*

	0	Old data, already read (**default**)
	1	New data, not yet read (cleared after read)

Bit[6] *reserved*

Bit[5] *FIFO_almost_full_interrupt* (updated even when the interrupt pin is disabled)

	0	Interrupt condition has not occurred (**default**)
	1	Interrupt condition has occurred (cleared after read, also cleared by reading *FIFO_DATA*)

Bit[4] *PPG_data_status*:

	0	Old data, already read (**default**)
	1	New data, not yet read (cleared after read, also cleared by reading *FIFO_DATA*)

Bit[2] *PS_logic_signal_status*:

	0	Object is far (**default**)
	1	Object is close

Bit[1] *PS_interrupt_status*: (updated even when the interrupt pin is disabled)

	0	Interrupt condition has not occurred (**default**)
	1	Interrupt condition has occurred (cleared after read)

Bit[0] *PS_data_status:*

	0	Old data, already read (**default**)
	1	New data, not yet read (cleared after read)

7.9.3 PS_DATA

Address	02_{HEX} and 03_{HEX}
Default value	00_{HEX} and 00_{HEX}
Register access	R

Bit	7	6	5	4	3	2	1	0
02_{HEX}	PS_DATA_0							
03_{HEX}	PS_DATA_1							

The PS conversion result is automatically corrected by the value of the PS cancellation register (*PS_CAN_DIG,* see section 7.9.14):

PS_ DATA = PS_meas – PS_CAN_DIG

PS_meas is the internal raw value obtained from the PS ADC. If the operations PS moving average and/or PS hysteresis are enabled, they will affect the PS data before they are written in the *PS_DATA* register.

The PS conversion result is written MSB-aligned into the PS_DATA registers. The result must always be treated as a 16-bit value regardless of the measurement resolution resulting from the pulse width setting selected in the *PS_PWIDTH_PERIOD* register (see section 7.9.13). For example, in 10-bit resolution, bits 0 to 5 in *PS_DATA_0* are always zero. The smallest value above zero is therefore 64 counts.

Reg 02_{HEX}	Bit[7:0]	PS measurement least significant data byte, bit 0 is always the LSB of the data word
Reg 03_{HEX}	Bit[7:0]	PS measurement most significant data byte, bit 7 is always the MSB of the data word

7.9.4 LS_CLEAR_DATA

Address	04_{HEX}, 05_{HEX}, and 06_{HEX}
Default value	00_{HEX}, 00_{HEX}, and 00_{HEX}
Register access	R

Bit	7	6	5	4	3	2	1	0
04_{HEX}	LS_CLEAR_DATA_0							
05_{HEX}	LS_CLEAR_DATA_1							
06_{HEX}	0	0	0	0	LS_CLEAR_DATA_2			

Light sensor Clear channel digital output data:

The LS conversion results are automatically compensated by the value of *COMP_DATA*:

$LS\_CLEAR\_DATA = (LS\_CLEAR_{int} – COMP\_DATA)$

LS_CLEAR_{int} is the internal raw value obtained from the Clear LS ADC. If LS_CLEAR_{int} is already full-scale, then the value of *LS_CLEAR_DATA* is set to its maximum value without subtracting *COMP_DATA*.

LS_CLEAR_DATA is clipped at ($2^{Resolution}$ – 1) and always written as unsigned integer values LSB-aligned into the *LS_CLEAR_DATA* registers, regardless of the resolution selected in the *LS_RES_PERIOD* register. *LS_CLEAR_DATA_2* and *LS_CLEAR_DATA_1* are filled with '0' for resolutions lower than 20 bit and 16 bit, respectively.

Reg 04_{HEX}	Bit[7:0]	Clear diode data least significant data byte
Reg 05_{HEX}	Bit[7:0]	Clear diode data middle data byte
Reg 06_{HEX}	Bit[3:0]	Clear diode data most significant data byte

7.9.5 LS_GREEN_DATA

Address	07_{HEX}, 08_{HEX}, and 09_{HEX}
Default value	00_{HEX}, 00_{HEX}, and 00_{HEX}
Register access	R

Bit	7	6	5	4	3	2	1	0
07_{HEX}	LS_GREEN_DATA_0							
08_{HEX}	LS_GREEN_DATA_1							
09_{HEX}	0	0	0	0	LS_GREEN_DATA_2			

Light sensor Green channel digital output data:

The LS conversion results are automatically compensated by the value of *COMP_DATA*:

LS_GREEN_DATA = (LS_GREEN_{int} – *COMP_DATA*)

LS_GREEN_{int} is the internal raw value obtained from the Green LS ADC. If LS_GREEN_{int} is already full-scale, then the value of *LS_GREEN_DATA* is set to its maximum value without subtracting *COMP_DATA*.

LS_GREEN_DATA is clipped at ($2^{Resolution}$ – 1) and always written as unsigned integer values LSB-aligned into the *LS_GREEN_DATA* registers, regardless of the resolution selected in the *LS_RES_PERIOD* register. *LS_GREEN_DATA_2* and *LS_GREEN_DATA_1* are filled with '0' for resolutions lower than 20 bit and 16 bit, respectively.

Reg 07_{HEX}	Bit[7:0]	Green diode data least significant data byte
Reg 08_{HEX}	Bit[7:0]	Green diode data middle data byte
Reg 09_{HEX}	Bit[3:0]	Green diode data most significant data byte

7.9.6 LS_BLUE_DATA

Address	$0A_{HEX}$, $0B_{HEX}$, and $0C_{HEX}$
Default value	00_{HEX}, 00_{HEX}, and 00_{HEX}
Register access	R

Bit	7	6	5	4	3	2	1	0
$0A_{HEX}$	LS_BLUE_DATA_0							
$0B_{HEX}$	LS_BLUE_DATA_1							
$0C_{HEX}$	0	0	0	0	LS_BLUE_DATA_2			

Light sensor Blue channel digital output data:

The LS conversion results are automatically compensated by the value of *COMP_DATA*:

LS_BLUE_DATA = (LS_BLUE_{int} – *COMP_DATA*)

LS_BLUE_{int} is the internal raw value obtained from the Blue LS ADC. If LS_BLUE_{int} is already full-scale, then the value of *LS_BLUE_DATA* is set to its maximum value without subtracting *COMP_DATA*.

LS_BLUE_DATA is clipped at ($2^{Resolution}$ – 1) and always written as unsigned integer values LSB-aligned into the *LS_BLUE_DATA* registers, regardless of the resolution selected in the *LS_RES_PERIOD* register. *LS_BLUE_DATA_2* and *LS_BLUE_DATA_1* are filled with '0' for resolutions lower than 20 bit and 16 bit, respectively.

Reg $0A_{HEX}$	Bit[7:0]	Blue diode data least significant data byte
Reg $0B_{HEX}$	Bit[7:0]	Blue diode data middle data byte
Reg $0C_{HEX}$	Bit[3:0]	Blue diode data most significant data byte

7.9.7 LS_RED_DATA

Address	$0D_{HEX}$, $0E_{HEX}$, and $0F_{HEX}$
Default value	00_{HEX}, 00_{HEX}, and 00_{HEX}
Register access	R

Bit	7	6	5	4	3	2	1	0
$0D_{HEX}$	LS_RED_DATA_0							
$0E_{HEX}$	LS_RED_DATA_1							
$0F_{HEX}$	0	0	0	0	LS_RED_DATA_2			

Light sensor Red channel digital output data:

The LS conversion results are automatically compensated by the value of *COMP_DATA*:

LS_RED_DATA = (LS_RED_{int} – *COMP_DATA*)

LS_RED_{int} is the internal raw value obtained from the Red LS ADC. If LS_RED_{int} is already full-scale then the value of *LS_RED_DATA* is set to its maximum value without subtracting *COMP_DATA*.

LS_RED_DATA is clipped at ($2^{Resolution}$ – 1) and always written as unsigned integer values LSB-aligned into the *LS_RED_DATA* registers, regardless of the resolution selected in the *LS_RES_PERIOD* register. *LS_RED_DATA_2* and *LS_RED_DATA_1* are filled with '0' for resolutions lower than 20 bit and 16 bit, respectively.

Reg $0D_{HEX}$	Bit[7:0]	Red diode data least significant data byte
Reg $0E_{HEX}$	Bit[7:0]	Red diode data middle data byte
Reg $0F_{HEX}$	Bit[3:0]	Red diode data most significant data byte

7.9.8 COMP_DATA

Address	10_{HEX} and 11_{HEX} and 12_{HEX}
Default value	00_{HEX} and 00_{HEX} and 00_{HEX}
Register access	R

Bit	7	6	5	4	3	2	1	0
10_{HEX}	COMP_DATA_0							
11_{HEX}	COMP_DATA_1							
12_{HEX}	0	0	0	0	COMP_DATA_2			

Light sensor temperature compensation (Comp) channel digital output data:

COMP_DATA is clipped at ($2^{Resolution}$ – 1) and always written as unsigned integer values LSB-aligned into the *COMP_DATA* registers, regardless of the resolution selected in the *LS_RES_PERIOD* register. *COMP_DATA_2* and *COMP_DATA_1* are filled with '0' for lower resolutions than 20 bit and 16 bit, respectively.

Reg 10_{HEX}	Bit[7:0]	Temperature compensation channel least significant data byte
Reg 11_{HEX}	Bit[7:0]	Temperature compensation channel middle data byte
Reg 12_{HEX}	Bit[3:0]	Temperature compensation channel most significant data byte

7.9.9 MAIN_CTRL_0

Address	15_{HEX}
Default value	00_{HEX}
Register access	R/W

Bit	7	6	5	4	3	2	1	0
15_{HEX}	SW reset	0	0	0	SAI_LS	0	LS_MODE	LS_EN

Note: Bits shown as '0' or '1' must be programmed as shown

Bit[7] *Software reset*:

- 0: No software reset triggered (**default**).
- 1: A software reset will be triggered immediately, and therefore the I2C bus command is NOT answered with "ACK." The part is operational after a typical delay of 10ms. However, the power-on reset bit in *STATUS_0* is NOT set.

Bit[3] *Sleep after interrupt for LS:*
This bit reacts on the "LS interrupt status" bit in the *STATUS_0* register.

- 0: The light sensor will stay active after an interrupt occurs (**default**).
- 1: The light sensor will return to standby (LS_EN will be cleared when the measurement is finished and the *STATUS_0* register is read) after an interrupt occurs. After *STATUS_0* is read, the sensor is re-enabled.

Bit[1] *Light sensor mode*:
This bit is only checked if *LS_EN* is active.

- 0: LS Mode (Green, Clear and Comp) channels activated (**default**).
- 1: CS Mode: All light sensor channels activated (Red, Green, Blue, Clear, and Comp).

Bit[0] *Light sensor enable:*

- 0: Light sensor inactive (**default**).
- 1: Light sensor active.

7.9.10 MAIN_CTRL_1

Address	16_{HEX}
Default value	00_{HEX}
Register access	R/W

Bit	7	6	5	4	3	2	1	0
16_{HEX}	0	0	0	0	SAI_PS	PPG_PS_MODE		PPG_PS_EN

Note: Bits shown as ‘0’ or ‘1’ must be programmed as shown.

Bit[3] *Sleep after interrupt for PS:*
This bit reacts on the “PS interrupt status” bit in the *STATUS_1* register.

0	The proximity sensor will stay active after an interrupt occurs (**default**).
1	The proximity sensor will return to standby (*PPG_PS_EN* will be cleared when the measurement is finished and the *STATUS_1* register is read) after an interrupt occurs.

Bit[2:1] *PPG proximity mode*

00_{BIN}	PS Mode (**default**)
01_{BIN}	PPG1 Mode. Measures PPG with IR LED (LED1 pin) unless the *LED_Flip* bit in the *PPG_PS_CFG* is set, in which case the red LED (LED2 pin) is used.
10_{BIN}	PPG2 Mode. Measures PPG with IR and red light interleaved. The first samples are with IR, the second samples with red, and then the pattern repeats, filling in alternate slots in the FIFO. If the *LED_Flip* bit (see section 7.9.27) is set the order is reversed.
11_{BIN}	Reserved.

Bit[0] *PPG or proximity sensor enable:*

0	PPG/PS inactive (**default**).
1	PPG/PS active.

7.9.11 PS_LED_CURR

Address	17_{HEX} and 18_{HEX}
Default value	FF_{HEX} and 01_{HEX}
Register access	R/W

Bit	7	6	5	4	3	2	1	0
17_{HEX}	PS_LED_CURR_0							
18_{HEX}	0	0	0	0	0	0	PS_LED_CURR_1	

Note: Bits shown as '0' or '1' must be programmed as shown.

PS LED current:

The PS LED current is adjustable in 1024 steps between 0 and 250mA nominal.

BIN Code	HEX Code	State
0000000000_{BIN}	000_{HEX}	LED off (0 mA)
0000000001_{BIN}	001_{HEX}	LED pulsed nominal current level = 0.24mA
0000000010_{BIN}	002_{HEX}	LED pulsed nominal current level = 0.49mA
…	…	…
0111111111_{BIN}	$1FF_{HEX}$	LED pulsed nominal current level = 125mA (**default**)
…		…
1111111111_{BIN}	$3FF_{HEX}$	LED pulsed nominal current level = 250mA

Reg 17_{HEX}	Bit[7:0]	PS LED current least significant data byte, bit 0 is the LSB of the data word
Reg 18_{HEX}	Bit[1:0]	PS LED current most significant data byte, bit 1 is MSB

Note: Writing to this register resets the PS state machine and starts new measurements.

7.9.12 PS_CAN_PULSES

Address 19HEX

Default value 1AHEX

Register access R/W

Bit	7	6	5	4	3	2	1	0
19HEX	0	PS_CAN_ANA	Number_of_LED_pulses			0	1	0

Note: Bits shown as '0' or '1' must be programmed as shown.

Bit[6] *PS analog cancellation level:*
PS_CAN_ANA determines the amount of analog photocurrent cancellation that is applied during the integration phase of the PS measurement. The PS analog cancellation level is expected to be written by the MCU during system startup.

0BIN	No offset cancellation (**default**)
1BIN	50% offset of the full scale value

Bit[5:3] *Number_of_LED_pulses in each PS measurement:*
This register controls the number of emitted PS LED pulses (1 to 32).

For example, for the pulse width of 42µs, the number of emitted LED pulses is limited to 16 at the pulse period of 3.125ms.

For the pulse width of 71µs the number of emitted LED pulses is limited to 8 at the pulse period of 3.125, and 16 at the pulse period of 6.25ms.

The number of LED pulses influences the measurement resolution; see Table 13.

000BIN	1 pulse
001BIN	2 pulses
010BIN	4 pulses
011BIN	8 pulses (**default**)
100BIN	16 pulses
101BIN	32 pulses
110BIN	32 pulses
111BIN	32 pulses

Note: Writing to this register resets the PS state machine and starts new measurements.

7.9.13 PS_PWIDTH_PERIOD

Address 1A$_{HEX}$

Default value 15$_{HEX}$

Register access R/W

Bit	7	6	5	4	3	2	1	0
1A$_{HEX}$	0	0	PS_pulse_width		0	PS_measurement_period		

Note: Bits shown as ‘0’ or ‘1’ must be programmed as shown.

Bit[5:4] *P_ pulse_width:*

This is the duration of each LED pulse in the PS measurement. The pulse width affects the measurement time and together with the number of LED pulses, it affects the measurement resolution; see Table 13.

00$_{BIN}$ 26µs

01$_{BIN}$ 42µs (default)

10$_{BIN}$ 71µs

11$_{BIN}$ Reserved

Bit[2:0] *PS_measurement_period:*

This is the nominal time between PS measurements.

000$_{BIN}$ 3.125ms

001$_{BIN}$ 6.25ms

010$_{BIN}$ 12.5ms

011$_{BIN}$ 25ms

100$_{BIN}$ 50ms

101$_{BIN}$ 100ms (default)

110$_{BIN}$ 200ms

111$_{BIN}$ 400ms

Note: Writing to this register resets the PS state machine and starts new measurements.

Table 13. PS Measurement Output Resolution

Pulse Width in µs	Number of Pulses					
	1	2	4	8	16	32
26	10 bit	11 bit	12 bit	13 bit	14 bit	15 bit
42	12 bit	13 bit	14 bit	15 bit	16 bit	16 bit
71	14 bit	15 bit	16 bit	16 bit	16 bit	16 bit

7.9.14 PS_CAN_DIG

Address 1B$_{HEX}$ and 1C$_{HEX}$

Default value 00$_{HEX}$ and 00$_{HEX}$

Register access R/W

Bit	7	6	5	4	3	2	1	0
1B$_{HEX}$	PS_CAN_DIG_0							
1C$_{HEX}$	PS_CAN_DIG_1							

PS digital cancellation level:
The digital cancellation value is subtracted from the measured PS data before the data is transferred to the *PS_DATA* registers and compared with the Interrupt thresholds. The PS digital cancellation level is expected to be written by the MCU host controller.

Reg 1B$_{HEX}$	Bit[7:0]	PS digital cancellation level least significant data byte; bit 0 is the LSB of the data word.
Reg 1C$_{HEX}$	Bit[7:0]	PS digital cancellation level most significant data byte; bit 7 is the MSB.

Note: Writing to this register resets the PS state machine and starts new measurements.

7.9.15 PS_MOV_AVG_HYS

Address	$1D_{HEX}$
Default value	00_{HEX}
Register access	R/W

Bit	7	6	5	4	3	2	1	0
$1D_{HEX}$	PS_moving_average_enable	PS_hysteresis_level						

Bit[7] *PS_moving_average_enable:*

If set, the *PS_DATA* is the average of the current and previous measurement The moving average is applied after digital offset cancellation.

0	PS moving average not applied (**default**).
1	PS moving average applied.

Bit[6:0] *PS_hysteresis_threshold:*

PS hysteresis mode tracks and holds the peak PS count level when objects are approaching, and it tracks and holds the baseline level when objects are moving away from the sensor.

This may be useful for capturing baseline or peak signal levels for determining thresholds when the controller might not be polling fast enough to capture every measurement. It also has the effect of reducing data variation as PS count fluctuations within the specified hysteresis are masked.

When the PS hysteresis level is set to a value larger than 00_{HEX}, the PS_DATA register displays the highest recorded PS count measurement (peak track and hold). When a signal arrives that is smaller than the peak signal minus the programmed hysteresis, PS_DATA switches to track and hold the lowest PS count measurement (baseline). Similarly, in baseline tracking mode, when a PS measurement is greater than the baseline plus the hysteresis, the PS_DATA switches to track and hold the subsequent peak values.

BIN Code	HEX Code	Value
0000000_{BIN}	00_{HEX}	0 (no hysteresis function applied) (**default**)
0000001_{BIN}	01_{HEX}	2
0000010_{BIN}	02_{HEX}	4
…	…	…
1111110_{BIN}	$7E_{HEX}$	252
1111111_{BIN}	$7F_{HEX}$	254

Note: Writing to this register resets the PS state machine and starts new measurements.

7.9.16 PS_THRES_UP

Address	$1E_{HEX}$ and $1F_{HEX}$
Default value	FF_{HEX} and FF_{HEX}
Register access	R/W

Bit	7	6	5	4	3	2	1	0
$1E_{HEX}$	PS_THRES_UP_0							
$1F_{HEX}$	PS_THRES_UP_1							

PS_THRES_UP sets the upper threshold value for the PS interrupt. The Interrupt Controller compares the value in *PS_THRES_UP* against the measured data in the *PS_DATA* registers. It generates an interrupt event if *PS_DATA* exceeds the upper threshold level.

The data format for *PS_THRES_UP* matches that of the *PS_DATA* registers.

Reg $1E_{HEX}$	Bit[7:0]	Upper threshold of PS interrupt least significant data byte; bit 0 is the LSB of the data word.
Reg $1F_{HEX}$	Bit[7:0]	Upper threshold of PS interrupt most significant data byte; bit 7 is MSB.

Note: Writing to this register resets the PS state machine and starts new measurements.

7.9.17 PS_THRES_LOW

Address	20_{HEX} and 21_{HEX}
Default value	00_{HEX} and 00_{HEX}
Register access	R/W

Bit	7	6	5	4	3	2	1	0
20_{HEX}	PS_THRES_LOW_0							
21_{HEX}	PS_THRES_LOW_1							

PS_THRES_LOW sets the lower threshold value for the PS interrupt. The Interrupt Controller compares the value in *PS_THRES_LOW* against measured data in the *PS_DATA* registers. It generates an interrupt event if *PS_DATA* is lower than the lower threshold level.

The data format for *PS_THRES_LOW* matches that of the *PS_DATA* registers.

Reg 20_{HEX}	Bit[7:0]	Upper threshold of PS interrupt least significant data byte; bit 0 is the LSB of the data word.
Reg 21_{HEX}	Bit[7:0]	Upper threshold of PS interrupt most significant data byte; bit 7 is the MSB.

Note: Writing to this register resets the PS state machine and starts new measurements.

7.9.18 LS_RES_PERIOD

Address	22_{HEX}
Default value	22_{HEX}
Register access	R/W

Bit	7	6	5	4	3	2	1	0
22_{HEX}	0	LS_ Resolution			0	LS_Measurement_Period		

Note: Bits shown as '0' or '1' must be programmed as shown.

Bit[6:4] *LS_Resolution:*
The resolution sets the measurement time and the precision of the measurement.

000_{BIN}	20 bit, 400ms
001_{BIN}	19 bit, 200ms
010_{BIN}	18 bit, 100ms **(default)**
011_{BIN}	17 bit, 50ms
100_{BIN}	16 bit, 25ms
101_{BIN}	13 bit, 3.125ms
110_{BIN}	Reserved
111_{BIN}	Reserved

Bit[2:0] *LS_Measurement_Period:*
This register controls the timing between LS measurements.

000_{BIN}	25ms
001_{BIN}	50ms
010_{BIN}	100ms **(default)**
011_{BIN}	200ms
100_{BIN}	500ms
101_{BIN}	1000ms
110_{BIN}	2000ms
111_{BIN}	2000ms

Note: When the measurement period is programmed to be shorter than possible for the specified ADC measurement time, the period will be longer than programmed (maximum speed).

Note: Writing to this register resets the LS state machine and starts new measurements.

7.9.19 LS_GAIN

Address	23_{HEX}
Default value	01_{HEX}
Register access	R/W

Bit	7	6	5	4	3	2	1	0
23_{HEX}	0	0	0	0	0	0	LS_gain_range	

Notes: Bits shown as '0' or '1' must be programmed as shown.

Note: The following LS detection ranges apply to the default resolution of 18-bit (measurement time = 100ms); see Table 7 for details. All channels of the Light Sensor run on the same range setting. Sensitivity settings correlate between the channels as shown in Table 7.

Bit[1:0] *LS / Green Channel detection range*:

00_{BIN}	Gain Mode 1	$6Lx_{min}$	to	Lx_{max}
01_{BIN}	Gain Mode 3 (**default**)	$2Lx_{min}$	to	Lx_{max} / 3
10_{BIN}	Gain Mode 6	Lx_{min}	to	Lx_{max} / 6

Lx_{min}: smallest detectable lux level, depending on type of light source.

Lx_{max}: largest detectable lux level, depending on type of light source.

Note: Writing to this register resets the LS state machine and starts new measurements.

7.9.20 LS_THRES_UP

Address	24_{HEX}, 25_{HEX}, and 26_{HEX}
Default value	FF_{HEX}, FF_{HEX}, and $0F_{HEX}$
Register access	R/W

Bit	7	6	5	4	3	2	1	0
24_{HEX}	LS_THRES_UP_0							
25_{HEX}	LS_THRES_UP_1							
26_{HEX}	0	0	0	0	LS_THRES_UP_2			

Note: Bits shown as ‘0’ or ‘1’ must be programmed as shown.

LS_THRES_UP sets the upper threshold value for the LS interrupt. The Interrupt Controller compares the value in *LS_THRES_UP* against measured data in the *_DATA* registers of the selected LS interrupt channel. It generates an interrupt event if *_DATA* exceeds the threshold level.

The data format for *LS_THRES_UP* matches that of the *_DATA* registers.

Reg 24_{HEX}	Bit[7:0]	LS upper interrupt threshold value, LSB
Reg 25_{HEX}	Bit[7:0]	LS upper interrupt threshold value, middle byte
Reg 26_{HEX}	Bit[3:0]	LS upper interrupt threshold value, MSB

Note: Writing to this register resets the LS state machine and starts new measurements.

7.9.21 LS_THRES_LOW

Address	27_{HEX}, 28_{HEX}, and 29_{HEX}
Default value	00_{HEX}, 00_{HEX}, and 00_{HEX}
Register access	R/W

Bit	7	6	5	4	3	2	1	0
27_{HEX}	LS_THRES_LOW_0							
28_{HEX}	LS_THRES_LOW_1							
29_{HEX}	0	0	0	0	LS_THRES_LOW_2			

Note: Bits shown as '0' or '1' must be programmed as shown.

LS_THRES_LOW sets the lower threshold value for the LS interrupt. The Interrupt Controller compares the value in *LS_THRES_LOW* against measured data in the *_DATA* registers of the selected LS interrupt channel. It generates an interrupt event if *_DATA* is below the threshold level.

The data format for *LS_THRES_LOW* matches that of the *_DATA* registers.

Reg 27_{HEX}	Bit[7:0]	LS lower interrupt threshold value, LSB
Reg 28_{HEX}	Bit[7:0]	LS lower interrupt threshold value, middle byte
Reg 29_{HEX}	Bit[3:0]	LS lower interrupt threshold value, MSB

Note: Writing to this register resets the LS state machine and starts new measurements.

7.9.22 LS_THRES_VAR

Address	$2A_{HEX}$
Default value	00_{HEX}
Register access	R/W

Bit	7	6	5	4	3	2	1	0
$2A_{HEX}$	0	0	0	0	0	LS_THRES_VAR		

Note: Bits shown as '0' or '1' must be programmed as shown.

Bit[2:1] *LS variance threshold*:

See section 7.6.1 for further details.

Code	Interrupt generated when…
000_{BIN}	New LS_DATA varies by ± 8 counts compared to previous result.
001_{BIN}	New LS_DATA varies by ± 16 counts compared to previous result.
010_{BIN}	New LS_DATA varies by ± 32 counts compared to previous result.
011_{BIN}	New LS_DATA varies by ± 64 counts compared to previous result.
100_{BIN}	New LS_DATA varies by ± 128 counts compared to previous result.
101_{BIN}	New LS_DATA varies by ± 256 counts compared to previous result.
110_{BIN}	New LS_DATA varies by ± 512 counts compared to previous result.
111_{BIN}	New LS_DATA varies by ± 1024 counts compared to previous result.

Note: Writing to this register resets the LS state machine and starts new measurements.

7.9.23 INT_CFG_0

Address	$2B_{HEX}$
Default value	10_{HEX}
Register access	R/W

Bit	7	6	5	4	3	2	1	0
$2B_{HEX}$	0	0	LS_INT_SEL		0	0	LS_VAR_MODE	LS_INT_EN

Note: Bits shown as ‘0’ or ‘1’ must be programmed as shown.

Bit[5:4]	*Light sensor interrupt source select:*	
	00_{BIN}	Clear channel
	01_{BIN}	LS / Green channel (**default**)
	10_{BIN}	Red channel
	11_{BIN}	Blue channel
Bit[1]	*Light sensor variation interrupt mode:*	
	0	LS Threshold Interrupt Mode (**default**)
	1	LS Variation Interrupt Mode
Bit[0]	*Light sensor interrupt enable:*	
	0	LS interrupt output pin disabled (**default**)
	1	LS interrupt output pin enabled

7.9.24 INT_CFG_1

Address 2C$_{HEX}$

Default value 00$_{HEX}$

Register access R/W

Bit	7	6	5	4	3	2	1	0
2C$_{HEX}$	0	0	A_FULL_INT_EN	PPG_INT_EN	0	0	PS_LOGIC_MODE	PS_INT_EN

Note: Bits shown as ‘0’ or ‘1’ must be programmed as shown.

Bit[5] *FIFO almost full interrupt enable:*

0 FIFO almost full interrupt disabled (**default**).

1 FIFO almost full interrupt enabled.

Bit[4] *PPG data interrupt enable:*

0 PPG data interrupt disabled (**default**).

1 PPG data interrupt enabled.

Bit[1] *Proximity sensor logic output mode:*

0 Normal interrupt function: After an interrupt event, the INT pin maintains an active level until the *STATUS_1* register is read (**default**).

1 PS Logic Output Mode: The INT pin is updated after every measurement and maintains an output state between measurements. This disables all other interrupts.

Bit[0] *Proximity sensor interrupt enable:*

0 PS interrupt pin output disabled (**default**).

1 PS interrupt pin output enabled.

7.9.25 INT_PST

Address 2D_{HEX}

Default value 00HEX

Register access R/W

Bit	7	6	5	4	3	2	1	0
2DHEX	LS_PERSIST				PS_PERSIST			

Bit[7:4] These bits set the number of similar consecutive LS interrupt events that must occur before the interrupt is asserted.

0000BIN Every LS value that is out of the threshold range (**default**) asserts an interrupt.

0001BIN 2 consecutive LS values that are out of the threshold range assert an interrupt.

…

1111BIN 16 consecutive LS values that are out of the threshold range assert an interrupt.

Bit[3:0] These bits set the number of similar consecutive PS interrupt events that must occur before the interrupt is asserted.

0000BIN Every PS value that is out of the threshold range (**default**) asserts an interrupt.

0001BIN 2 consecutive PS values that are out of the threshold range assert an interrupt.

…

1111BIN 16 consecutive PS values that are out of the threshold range assert an interrupt.

7.9.26 PPG_PS_GAIN

Address 2EHEX

Default value 09HEX

Register access R/W

Bit	7	6	5	4	3	2	1	0
2EHEX	0	0	PPG/PS_gain_range		1	0	0	1

Note: Bits shown as ‘0’ or ‘1’ must be programmed as shown.

Bit[5:4] *PPG/PS_gain_range*:

Gain scales the ADC output and noise.

00BIN Gain Mode 1 (**default**)

01BIN Gain Mode 1.5

10BIN Gain Mode 2

11BIN Gain Mode 4

7.9.27 PPG_PS_CFG

Address	$2F_{HEX}$
Default value	40_{HEX}
Register access	R/W

Bit	7	6	5	4	3	2	1	0
$2F_{HEX}$	0	PPG_POW_SAVE	0	0	LED_FLIP	0	0	0

Note: Bits shown as ‘0’ or ‘1’ must be programmed as shown.

Bit[6] *PPG power save mode*:

On Power Save Mode, some analog circuitry powers down between individual PPG measurements if the idle time $t_{PPG\_idle} \geq 50\mu s$.

0	Power save mode disabled
1	Power save mode enabled (**default**)

Bit[3] *LED_flip*:

Controls which LED is activated (PS, PPG1) or in which order the LEDs are activated (PPG2)

0	Standard LED operation: PS, PPG1 and the first PPG2 sample will be measured with IR LED (LED1 pin) and second PPG2 sample with Red LED (LED2 pin) (**default**).
1	LEDs are flipped. PS, PPG1 and the first PPG2 sample will be measured with red LED source and second PPG2 sample with IR LED source.

7.9.28 PPG_IRLED_CURR

Address	30_{HEX} and 31_{HEX}
Default value	00_{HEX} and 00_{HEX}
Register access	R/W

Bit	7	6	5	4	3	2	1	0
30_{HEX}	PPG_IRLED_CURR_0							
31_{HEX}	0	0	0	0	0	0	PPG_IRLED_CURR_1	

Bits shown as '0' or '1' must be programmed as shown.

Reg 30_{HEX}	Bit[7:0]	PPG IR LED current least significant data byte; bit 0 is the LSB of the data word.
Reg 31_{HEX}	Bit[1:0]	PPG IR LED current most significant data byte; bit 1 is MSB.

PPG IR LED current:

The PPG IR LED (LED1 pin) current is adjustable in 1024 steps between 0 and nominal 250mA.

BIN Code	HEX Code	State
0000000000_{BIN}	000_{HEX}	LED off (0mA) **(default)**
0000000001_{BIN}	001_{HEX}	LED nominal pulsed current level = 0.24mA
0000000010_{BIN}	002_{HEX}	LED nominal pulsed current level = 0.49mA
…	…	…
0111111111_{BIN}	$1FF_{HEX}$	LED nominal pulsed current level = 125mA
…		…
1111111111_{BIN}	$3FF_{HEX}$	LED nominal pulsed current level = 250mA

7.9.29 PPG_RLED_CURR

Address	32_{HEX} and 33_{HEX}
Default value	00_{HEX} and 00_{HEX}
Register access	R/W

Bit	7	6	5	4	3	2	1	0
32_{HEX}	PPG_RLED_CURR_0							
33_{HEX}	0	0	0	0	0	0	0	PPG_RLED_CURR_1

Note: Bits shown as ‘0’ or ‘1’ must be programmed as shown.

Reg 32_{HEX}	Bit[7:0]	PPG Red LED current least significant data byte; bit 0 is the LSB of the data word.
Reg 33_{HEX}	Bit[0]	PPG Red LED current most significant data bit; bit 0 is the MSB.

PPG Red LED current:

The PPG Red LED current is adjustable in 512 steps between 0 and nominal 125mA.

BIN Code	HEX Code	State
000000000_{BIN}	000_{HEX}	LED off (0mA) **(default)**
000000001_{BIN}	001_{HEX}	LED nominal pulsed current level = 0.24mA
000000010_{BIN}	002_{HEX}	LED nominal pulsed current level = 0.49mA
…	…	…
111111110_{BIN}	$1FE_{HEX}$	LED nominal pulsed current level = 124.76mA
111111111_{BIN}	$1FF_{HEX}$	LED nominal pulsed current level = 125mA

7.9.30 PPG_CAN_ANA

Address	34_{HEX}
Default value	00_{HEX}
Register access	R/W

Bit	7	6	5	4	3	2	1	0
34_{HEX}	0	0	0	0	0	PPG_CH1_CAN_ANA	0	PPG_CH2_CAN_ANA

Note: Bits shown as ‘0’ or ‘1’ must be programmed as shown.

Bit[2] *PPG analog cancellation* level for LED1:
PPG_CH1_CAN_ANA determines the amount of the cancellation that is applied during the integration phase of the PPG measurement with the IR LED (LED1 pin). The following offsets apply in respect to the full-scale value of the FIFO data.

0_{BIN}	No offset cancellation (**default**)
1_{BIN}	50% offset of the full-scale value

Bit[0] *PPG analog cancellation* level for LED2:
PPG_CH2_CAN_ANA determines the amount of the cancellation that is applied during the integration phase of the PPG measurement with the Red LED (LED2 pin). The following offsets apply in respect to the full-scale value of the FIFO data.

0_{BIN}	No offset cancellation (**default**)
1_{BIN}	50% offset of the full-scale value

7.9.31 PPG_AVG

Address	35_{HEX}
Default value	$0A_{HEX}$
Register access	R/W

Bit	7	6	5	4	3	2	1	0
35_{HEX}	0	PPG_AVG			1	0	1	0

Note: Bits shown as ‘0’ or ‘1’ must be programmed as shown.

Bit[6:4] *Number of averaged PPG samples:*

Before PPG samples are written to the FIFO, an averaging function can be applied to increase accuracy and reduce the data rate. The number of averaged PPG samples influences the measurement resolution; see Table 14. For example, averaging 16 samples reduces the data rate by a factor of 16.

000_{BIN}	1 (no averaging) (**default**).
001_{BIN}	2 consecutives samples are averaged.
010_{BIN}	4 consecutives samples are averaged.
011_{BIN}	8 consecutives samples are averaged.
100_{BIN}	16 consecutives samples are averaged.
101_{BIN}	32 consecutives samples are averaged.
110_{BIN}	32 consecutives samples are averaged.
111_{BIN}	32 consecutives samples are averaged.

7.9.32 PPG_PWIDTH_PERIOD

Address	36_{HEX}
Default value	42_{HEX}
Register access	R/W

Bit	7	6	5	4	3	2	1	0
36_{HEX}	0	PPG_pulse_width			0	PPG_measurement_period		

Note: Bits shown as '0' or '1' must be programmed as shown.

Bit[6:4] *PPG_pulse_width:*

The pulse width will have an effect on the measurement time. The pulse width and the number of averaged PPG samples determine the measurement resolution (see Table 14). Table 15 and Table 16 show which combinations of PPG pulse width and measurement period are allowed.

000_{BIN}	Reserved
001_{BIN}	Reserved
010_{BIN}	Reserved
011_{BIN}	130µs
100_{BIN}	247µs (default)
101_{BIN}	481µs
110_{BIN}	949µs
111_{BIN}	949µs

Bit[2:0] *PPG_measurement_period:*

For PPG1 one sample is measured during the measurement period. In PPG2 Mode, two samples are measured, one for each LED. Table 15 and Table 16 show which combinations of PPG pulse width and measurement period are allowed.

Code	Measurement Period
000_{BIN}	0.3125ms
001_{BIN}	0.625ms
010_{BIN}	1ms (default)
011_{BIN}	1.25ms
100_{BIN}	2.5ms
101_{BIN}	5ms
110_{BIN}	10ms
111_{BIN}	20ms

Table 14. PPG Measurement Output Resolution

Pulse Width in µs	Number of Averaged Samples					
	1	2	4	8	16	32
130	16 bit	17 bit	18 bit	18 bit	18 bit	18 bit
247	18 bit	18 bit	18 bit	18 bit	18 bit	18 bit
481	18 bit	18 bit	18 bit	18 bit	18 bit	18 bit
949	18 bit	18 bit	18 bit	18 bit	18 bit	18 bit

Table 15. PPG1 Mode Parameter

Measurement Period t_{PPG} in ms	Pulse Width t_{PPG_pw} in µs			
	130	247	481	949
0.312 Register 36hex setting	✓ b: 0011 0000			
0.625 Register 36hex setting	✓ b: 0011 0001	✓ b: 0100 0001		
1 Register 36hex setting	✓ b: 0011 0010	✓ b: 0100 0010	✓ b: 0101 0010	
1.25 Register 36hex setting	✓ b: 0011 0011	✓ b: 0100 0011	✓ b: 0101 0011	
2.5 Register 36hex setting	✓ b: 0011 0100	✓ b: 0100 0100	✓ b: 0101 0100	✓ b: 0110 0100
5 Register 36hex setting	✓ b: 0011 0101	✓ b: 0100 0101	✓ b: 0101 0101	✓ b: 0110 0101
10 Register 36hex setting	✓ b: 0011 0110	✓ b: 0100 0110	✓ b: 0101 0110	✓ b: 0110 0110
20 Register 36hex setting	✓ b: 0011 0111	✓ b: 0100 0111	✓ b: 0101 0111	✓ b: 0110 0111

Table 16. PPG2 Mode Parameter

Measurement Period t_{PPG} in ms	Pulse Width t_{PPG_pw} in µs			
	130	247	481	949
0.312				
0.625 Register 36hex setting	✓ b: 0011 0001			
1 Register 36hex setting	✓ b: 0011 0010	✓ b: 0100 0010		
1.25 Register 36hex setting	✓ b: 0011 0011	✓ b: 0100 0011		
2.5 Register 36hex setting	✓ b: 0011 0100	✓ b: 0100 0100	✓ b: 0101 0100	
5 Register 36hex setting	✓ b: 0011 0101	✓ b: 0100 0101	✓ b: 0101 0101	✓ b: 0110 0101
10 Register 36hex setting	✓ b: 0011 0110	✓ b: 0100 0110	✓ b: 0101 0110	✓ b: 0110 0110
20 Register 36hex setting	✓ b: 0011 0111	✓ b: 0100 0111	✓ b: 0101 0111	✓ b: 0110 0111

7.9.33 FIFO_CFG

Address	37_{HEX}
Default value	00_{HEX}
Register access	R/W

Bit	7	6	5	4	3	2	1	0
37_{HEX}	0	0	0	FIFO_ROLLOVER_EN	FIFO_A_FULL			

Note: Bits shown as '0' or '1' must be programmed as shown.

Bit[4] *FIFO Rollover Enable*:

0	In the event of a full FIFO, no more samples of PPG data are written into the FIFO; the samples from new measurements are lost. (**default**).
1	New PPG data will always be written to the FIFO, and the FIFO Write Pointer is incremented (rollover). If the FIFO is full, old data will be overwritten. The FIFO Overflow Counter counts the number of lost (overwritten) and respectively the number of new samples. The FIFO Read Pointer remains unchanged.

Bit[3:0] *FIFO Almost Full Value*:
FIFO_A_FULL determines the number of empty FIFO words when the FIFO almost full interrupt is issued. In PPG2 Mode only even values of FIFO_A_FULL should be used. Larger values are useful for a controller with a longer latency.

Code	Number of Empty FIFO Words	Number of Unread PPG1 Samples	Number of Unread PPG2 Sample Pairs
0000_{BIN}	0 (FIFO is full) (**default**)	32 (**default**)	16 (**default**)
0001_{BIN}	1	31	–
0010_{BIN}	2	30	15
0011_{BIN}	3	29	–
…			
1110_{BIN}	14	18	9
1111_{BIN}	15	17	–

7.9.34 FIFO_WR_PTR

Address	38_{HEX}
Default value	00_{HEX}
Register access	R/(W)

Bit	7	6	5	4	3	2	1	0
38_{HEX}	0	0	0	FIFO_WR_PTR				

Note: Bits shown as ‘0’ or ‘1’ must be programmed as shown.

Bit[4:0] *FIFO Write Pointer:*

The FIFO write pointer contains the FIFO index where the next sample of PPG data will be written in the FIFO. After a sample is written into the corresponding FIFO register, the FIFO write pointer is automatically incremented. The FIFO write pointer should be reset to 0 before enabling measurements through *MAIN_CTRL_1*. Otherwise there is no defined state and the PPG data will be written to the FIFO at the current index of the FIFO write pointer. The FIFO write pointer should not be overwritten at other times to ensure consistent data.

00000_{BIN}	FIFO register index 00_{DEC}
00001_{BIN}	FIFO register index 01_{DEC}
…	…
11110_{BIN}	FIFO register index 30_{DEC}
11111_{BIN}	FIFO register index 31_{DEC}

7.9.35 FIFO_RD_PTR

Address	39_{HEX}
Default value	00_{HEX}
Register access	R/(W)

Bit	7	6	5	4	3	2	1	0
39_{HEX}	0	0	0	FIFO_RD_PTR				

Note: Bits shown as '0' or '1' must be programmed as shown.

Bit[4:0] *FIFO Read Pointer:*
The FIFO read pointer contains the index of the next sample to be read from the *FIFO_DATA* register (see section 7.9.37). After the 3-byte sample from the *FIFO_DATA* register has been read, the FIFO read pointer is automatically incremented. The FIFO read pointer can be written to re-read a sample in the event of a communication error. It should always be reset to 0 before enabling measurements through the *MAIN_CTRL_1* register (see section 7.9.10).

00000_{BIN}	FIFO register index 00_{DEC}
00001_{BIN}	FIFO register index 01_{DEC}
…	…
11110_{BIN}	FIFO register index 30_{DEC}
11111_{BIN}	FIFO register index 31_{DEC}

7.9.36 FIFO_OVF_CNT

Address	$3A_{HEX}$
Default value	00_{HEX}
Register access	R/(W)

Bit	7	6	5	4	3	2	1	0
$3A_{HEX}$	0	0	0	0	FIFO_OVF_CNT			

Note: Bits shown as '0' or '1' must be programmed as shown.

Bit[3:0] *FIFO Overflow Counter:*
If the FIFO Rollover Enable bit is set, the FIFO overflow counter counts the number of old samples (up to 15) which are overwritten by new data. The FIFO overflow counter should always be reset to 0 before enabling measurements through the *MAIN_CTRL_1* register (see section 7.9.10).

7.9.37 FIFO_DATA

Address	$3B_{HEX}$
Default value	00_{HEX}
Register access	R

Bit	7	6	5	4	3	2	1	0
$3B_{HEX}$	FIFO_DATA							

FIFO Data:
FIFO_DATA contains the data at the index value of the FIFO read pointer. Reading the *FIFO_DATA* register does not increment the I2C register address. A block read from this register reads this address again and again. However the *FIFO_RD_PTR* register (see section 7.9.35) is incremented after reading a sample of 3 bytes (block read). For example, the entire FIFO can be read out by a block read of 96 bytes. The PPG conversion result is written MSB-aligned into the FIFO. The result must always be treated as 18-bit value regardless of the measurement resolution resulting from the pulse width setting selected in the *PPG_PWIDTH_PERIOD* register (see section 7.9.32). One PPG sample can be read like this:

1st read byte FIFO_DATA	Bit[7:0]	PPG measurement least significant data byte; bit 0 is always the LSB of the data word.
2nd read byte FIFO_DATA	Bit[7:0]	PPG measurement middle data byte.
3rd read byte FIFO_DATA	Bit[1:0]	PPG measurement most significant data byte; bit 1 is always the MSB of the data word.

7.9.38 PART_ID

Address	$3D_{HEX}$
Default value	TBD
Register access	R

Bit	7	6	5	4	3	2	1	0
$3D_{HEX}$	Part_Number_ID							

Bit[7:0] *Part_Number_ID* (reserved)

8. Package Outline Drawings

The package outline drawings are appended at the end of this document. The package information is the most current data available.

9. Reflow Profile

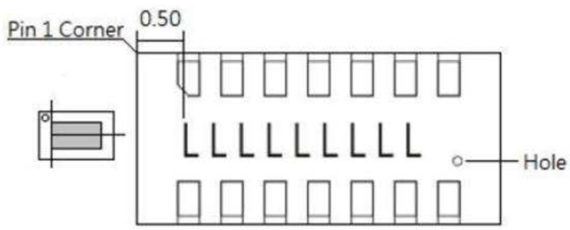
Table 17. Recommended Reflow Profile

Profile Feature	Sn-Pb Assembly	Pb-free Assembly
Average Ramp-up Rate (T_L to T_P)	3°C/sec max	3°C/sec max
Preheat/Soak		
Minimum Temp (Ts_{min})	100°C	150°C
Maximum Temp (Ts_{max})	150°C	200°C
Time (t_S) from (Ts_{min} to Ts_{max})	60-120 seconds	60-180 seconds
Time Maintained Above		
Temperature (T_L)	183°C	217°C
Time (t_L)	60-150 seconds	60-150 seconds
Peak Package Body Temperature (T_P)	T_P must not exceed the classification temperature Tc = 260ºC.	T_P must not exceed the classification temperature Tc = 260ºC.
Time within 5°C of Actual Peak Temperature (T_p)	20 seconds	30* seconds
Ramp-down Rate (T_P to T_L)	6°C/sec maximum	6°C/sec maximum
Time Peak Temperature to 25°C	6 min maximum	8 min maximum

Refer to the JEDEC specification for an illustration of the reflow profile chart.

10. Marking Diagram: Bottom of Part Only

Pin 1 notch



Character 1-4 : Product Description
Character 5-9 : Last 5 digit of Assembly Lot No

Height	Width	Space	Max Width	Max chars
0.40 mm	0.23 mm	0.09 mm	2.79 mm	9

Product	Character 1-4
OB1203SD-C4 Z LJG14	1203

11. Ordering Information

Orderable Part Number	Description and Package	MSL Rating	Shipping Packaging	Temperature
OB1203SD-C4V	4.2 × 2.0 × 1.2 mm 14-OSIP	3	Tray	-40°C to +85°C
OB1203SD-C4R	4.2 × 2.0 × 1.2 mm 14-OSIP	3	Reel	-40°C to +85°C
OB1203SD-U-EVK	OB1203 Integrated Concept Engine (ICE) Health Sensor Evaluation Kit – USB including OB1203 Sensor Board, ST Nucleo I2C USB Communication Board, USB Cable and USB Stick with GUI.			
OB1203SD-BT-EVK	OB1203 ICE Health Sensor Evaluation Kit – Bluetooth including OB1203 Sensor Board with Bluetooth Chip, Rechargeable Battery. Android app is downloadable.			

12. Glossary

Term	Description
ADC	Analog-to-Digital Converter
AOI	Angle of Incidence
Comp.	Temperature Compensation (Dark Channel for Light Sensor)
CS	Color Sensor Function using the Red, Green, Blue, Clear and Comp. Sensors
FIFO	First-In-First-Out Register Bank
FSM	Finite State Machine
HP	High Precision (Oscillator)
ICE	Integrated Concept Engine

Term	Description
JEDEC	Joint Electron Device Engineering Council
LP	Low Power (Oscillator)
LS	Light Sensor Function using the Clear, Green and Comp Sensors in the OB1203
LSB	Least Significant Bit
MCU	Microcontroller Unit
MSB	Most Significant Bit
NVM	Nonvolatile Memory
OSIP	Optical System in Package
POR	Power-on Reset
PPG	Photoplethysmography
RGB	Red, Green, Blue
SDA	Serial Data
SCL	Serial Clock
SW	Software

13. Revision History

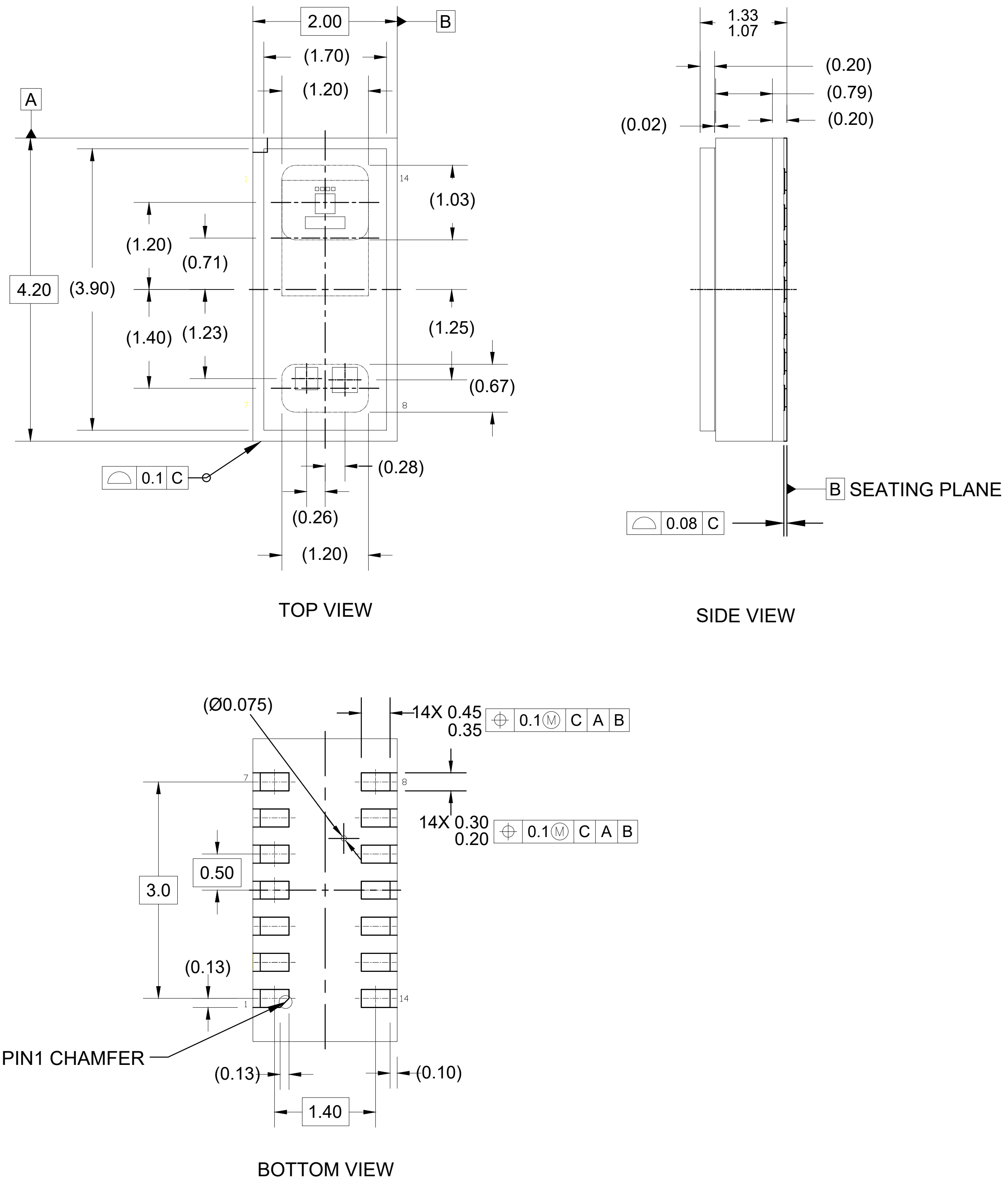
Revision Date	Description of Change
January 12, 2021	Updated the STATUS_1 register description.
November 2, 2020	Updated the description of Peak Package Body Temperature (T_P) in Table 17.
May 29, 2020	Initial release.

Package Outline Drawing

Package Code: LJGD2

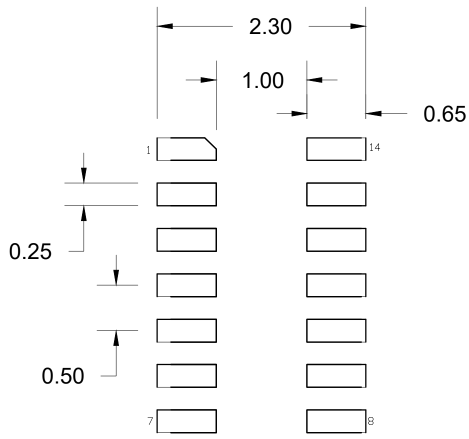
14-LGA 2.00 x 4.20 x 1.20 mm Body, 0.50mm Pitch

PSC-4748-02, Revision: 01, Date Created: April 20, 2022



NOTES:

1. All dimensions are in mm. .
2. ±0.05 tolerance applies where no tolerance is indicated.



RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. All dimensions are in mm. angles in degrees.
2. Top down view as viewed on PCB.
3. Land pattern recommendation per IPC-7351B generic requirement for surface mount design and land pattern.

ASSEMBLY RECOMMENDATIONS:

1. Use low-flux solder paste to avoid excess flux being siphoned into vent hole on bottom of package
2. Do not wash after soldering; liquid can enter the optical cavities via the vent hole.
3. If liquid appears inside the optical cavity, dry at 100 C for 8 hrs.

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Contact Information

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