MCP6N16
Zero-Drift Instrumentation Amplifier

Features:
- High DC Precision:
  - $V_{OS}$: $\pm 17 \mu V$ (maximum, $G_{MIN} = 100$)
  - $TC_1$: $\pm 60$ nV/°C (maximum, $G_{MIN} = 100$)
  - CMRR: 112 dB (minimum, $G_{MIN} = 100$, $V_{DD} = 5.5V$)
  - PSRR: 110 dB (minimum, $G_{MIN} = 100$, $V_{DD} = 5.5V$)
  - $g_E$: $\pm 0.15\%$ (maximum, $G_{MIN} = 10, 100$)
- Flexible:
  - Minimum Gain ($G_{MIN}$) Options: 1, 10 and 100 V/V
  - Rail-to-Rail Input and Output
  - Gain Set by Two External Resistors
- Bandwidth: 500 kHz (typical, $Gain = G_{MIN} = 1, 10$)
- Power Supply:
  - $V_{DD}$: 1.8V to 5.5V
  - $I_Q$: 1.1 mA (typical)
  - Power Savings (Enable) Pin: EN
- Enhanced EMI Protection:
  - Electromagnetic Interference Rejection Ratio (EMIRR): 111 dB at 2.4 GHz
- Extended Temperature Range: -40°C to +125°C

Typical Applications:
- High-Side Current Sensor
- Wheatstone Bridge Sensors
- Difference Amplifier with Level Shifting
- Power Control Loops

Design Aids:
- SPICE Macro Model
- Microchip Advanced Part Selector (MAPS)
- Application Notes

Description:
Microchip Technology Inc. offers the single Zero-Drift MCP6N16 instrumentation amplifier (INA) with Enable pin (EN) and three minimum gain options ($G_{MIN}$). The internal offset correction gives high DC precision: it has very low offset and offset drift, and negligible 1/f noise.

Two external resistors set the gain, minimizing gain error and drift over temperature. The reference voltage ($V_{REF}$) shifts the output voltage ($V_{OUT}$).

The MCP6N16 is designed for single-supply operation, with rail-to-rail input (no common mode crossover distortion) and output performance. The supply voltage range (1.8V to 5.5V) is low enough to support many portable applications. All devices are fully specified from -40°C to +125°C. Each part has EMI filters at the input pins, for good EMI rejection (EMIRR).

These parts have three minimum gain options (1, 10 and 100 V/V). This allows the user to optimize the input offset voltage and input noise for different applications.

Typical Application Circuit

![Typical Application Circuit](image)

Package Types

<table>
<thead>
<tr>
<th>MCP6N16</th>
<th>MCP6N16</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSOP</td>
<td>3×3 DFN *</td>
</tr>
</tbody>
</table>

* Includes Exposed Thermal Pad (EP); see Table 3-1.
Minimum Gain Options

Table 1 shows key specifications that differentiate between the different minimum gain (GMIN) options. See Section 1.0 “Electrical Characteristics”, Section 6.0 “Packaging Information” and Product Identification System for further information on GMIN.

TABLE 1: KEY DIFFERENTIATING SPECIFICATIONS

<table>
<thead>
<tr>
<th>Part No.</th>
<th>GMIN (V/V) Nom.</th>
<th>VOS (±μV) Max.</th>
<th>TC1 (±nV/°C) Max.</th>
<th>CMRR (dB) Min.</th>
<th>PSRR (dB) Min.</th>
<th>VDMH (V) Min.</th>
<th>GBWP (MHz) Typ.</th>
<th>Eni (μVp-p) Typ.</th>
<th>eni (nV/√Hz) Typ.</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCP6N16-001</td>
<td>1</td>
<td>85</td>
<td>1800</td>
<td>89</td>
<td>91</td>
<td>2.7</td>
<td>0.50</td>
<td>19</td>
<td>900</td>
</tr>
<tr>
<td>MCP6N16-010</td>
<td>10</td>
<td>22</td>
<td>180</td>
<td>103</td>
<td>104</td>
<td>0.27</td>
<td>5.0</td>
<td>2.2</td>
<td>105</td>
</tr>
<tr>
<td>MCP6N16-100</td>
<td>100</td>
<td>17</td>
<td>60</td>
<td>112</td>
<td>110</td>
<td>0.027</td>
<td>35</td>
<td>0.93</td>
<td>45</td>
</tr>
</tbody>
</table>

Note 1: GMIN is the minimum stable gain (GDM), for a given part option. In other words, GDM ≥ GMIN.

Figures 1 to 3 show input offset voltage versus temperature for the three gain options (GMIN = 1, 10, 100 V/V).

**FIGURE 1:** Input Offset Voltage vs. Temperature, with GMIN = 1.

**FIGURE 2:** Input Offset Voltage vs. Temperature, with GMIN = 10.

**FIGURE 3:** Input Offset Voltage vs. Temperature, with GMIN = 100.
1.0 ELECTRICAL CHARACTERISTICS

1.1 Absolute Maximum Ratings †

- \( V_{DD} - V_{SS} \).............................................................................................................. 6.5V
- Current at Input Pins (Note 1) .............................................................................................................. ±2 mA
- Analog Inputs (\( V_{IP} \) and \( V_{IM} \)) (Note 1) ........................................................................... \( V_{SS} - 1.0 \text{V to } V_{DD} + 1.0 \text{V} \)
- All Other Inputs and Outputs ............................................................................................................. \( V_{SS} - 0.3 \text{V to } V_{DD} + 0.3 \text{V} \)
- Difference Input Voltage ......................................................................................................................... \( |V_{DD} - V_{SS}| \)
- Output Short-Circuit Current ............................................................................................................. Continuous
- Current at Output and Supply Pins ...................................................................................................... ±30 mA
- Storage Temperature ..................................................................................................................... -65°C to +150°C
- Maximum Junction Temperature .................................................................................................... +150°C
- ESD protection on all pins (HBM, MM)................................................................................................... ≥ 4 kV, 400V

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: See Section 4.3.1.2 “Input Voltage Limits” and Section 4.3.1.3 “Input Current Limits”. 
## 1.2 Specifications

**TABLE 1-1: DC ELECTRICAL SPECIFICATIONS**

*Electrical Characteristics:* Unless otherwise indicated, $T_A = +25°C$, $V_{DD} = 1.8V$ to 5.5V, $V_{SS} = GND$, $V_{CM} = V_{DD}/2$, $V_{DM} = 0V$, $V_{REF} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10$ kΩ to $V_L$, $G_{DM} = G_{MIN}$ and $EN = V_{DD}$; see Figures 1-7 and 1-8 (Note 1).

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym.</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>$G_{MIN}$</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Offset Voltage</td>
<td>$V_{OS}$</td>
<td>-85</td>
<td>—</td>
<td>+85</td>
<td>µV</td>
<td>1</td>
<td>$T_A = +25°C$</td>
</tr>
<tr>
<td>Input Offset Voltage</td>
<td></td>
<td>-22</td>
<td>—</td>
<td>+22</td>
<td></td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>Input Offset Voltage</td>
<td></td>
<td>-17</td>
<td>—</td>
<td>+17</td>
<td></td>
<td>100</td>
<td></td>
</tr>
<tr>
<td>Input Offset Voltage Drift – Linear Temp. Co.</td>
<td>$TC_1$</td>
<td>-1800</td>
<td>—</td>
<td>+1800</td>
<td>nV/°C</td>
<td>1</td>
<td>$T_A = -40°C$ to $+125°C$ (Note 2)</td>
</tr>
<tr>
<td>Input Offset Voltage Drift – Quadratic Temp. Co.</td>
<td>$TC_2$</td>
<td>—</td>
<td>±560</td>
<td>—</td>
<td>pV/°C²</td>
<td>1</td>
<td>$T_A = -40°C$ to $+125°C$</td>
</tr>
<tr>
<td>Input Offset Aging</td>
<td>$\Delta V_{OS}$</td>
<td></td>
<td>±1.0</td>
<td>—</td>
<td>µV</td>
<td>1</td>
<td>408 hr Life Test at $+150°C$, measured at $+25°C$</td>
</tr>
<tr>
<td>Power Supply Rejection Ratio</td>
<td>PSRR</td>
<td>91</td>
<td>109</td>
<td></td>
<td>dB</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>104</td>
<td>122</td>
<td></td>
<td>10</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>110</td>
<td>128</td>
<td></td>
<td>100</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Offset</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Offset Voltage</td>
<td>$V_{OSO}$</td>
<td>0</td>
<td></td>
<td></td>
<td>µV</td>
<td>all</td>
<td></td>
</tr>
</tbody>
</table>

**Input Current and Impedance (Note 3)**

| Input Bias Current | | | | | | | |
| Across Temperature | $I_B$ | -100 | ±2 | +100 | pA | all | $T_A = +85°C$ |
| Across Temperature | | 20 | | | | | $T_A = +125°C$ |

**Note 1:** $V_{CM} = (V_{IP} + V_{IM})/2$, $V_{DM} = (V_{IP} - V_{IM})$ and $G_{DM} = 1 + R_F/R_G$.

**2:** For Design Guidance only; not tested.

**3:** These specifications apply to the $V_{IP}$, $V_{IM}$ input pair (use $V_{CM}$) and to the $V_{REF}$, $V_{FG}$ input pair (use $V_{REF}$ instead).

**4:** This specification applies to the $V_{IP}$, $V_{IM}$, $V_{REF}$ and $V_{FG}$ pins individually.

**5:** Figures 2-52 and 2-53 show the $V_{IVL}$, $V_{IVH}$, $V_{DML}$ and $V_{DMH}$ variation over temperature.

**6:** See Section 1.5 “Explanation of DC Error Specifications”.

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*Note 1:* $V_{CM} = (V_{IP} + V_{IM})/2$, $V_{DM} = (V_{IP} - V_{IM})$ and $G_{DM} = 1 + R_F/R_G$.

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*6:* See Section 1.5 “Explanation of DC Error Specifications”. 
### TABLE 1-1: DC ELECTRICAL SPECIFICATIONS (CONTINUED)

**Electrical Characteristics:** Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = 1.8$V to 5.5V, $V_{SS} = GND$, $V_{CM} = V_{DD}/2$, $V_{DM} = 0$V, $V_{REF} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10$ k$\Omega$ to $V_L$, $G_{DM} = G_{MIN}$ and $EN = V_{DD}$; see Figures 1-7 and 1-8 (Note 1).

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym.</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>$G_{MIN}$</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Offset Current</td>
<td>$I_{\text{OS}}$</td>
<td>-800</td>
<td>±300</td>
<td>+800</td>
<td>pA</td>
<td>all</td>
<td>$T_A = +85^\circ C$</td>
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<tr>
<td>Across Temperature</td>
<td>—</td>
<td>±320</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>$T_A = +125^\circ C$</td>
<td></td>
</tr>
<tr>
<td>Across Temperature</td>
<td>-1500</td>
<td>±350</td>
<td>+1500</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
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<tr>
<td>Common Mode Input Impedance</td>
<td>$Z_{\text{CM}}$</td>
<td>—</td>
<td>$10^{13}$</td>
<td></td>
<td>10</td>
<td>—</td>
<td>Ω</td>
</tr>
<tr>
<td>Differential Input Impedance</td>
<td>$Z_{\text{DIFF}}$</td>
<td>—</td>
<td>$10^{13}$</td>
<td></td>
<td>4</td>
<td>—</td>
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</table>

**Input Common Mode Voltage ($V_{CM}$ or $V_{REF}$) (Note 3)**

<table>
<thead>
<tr>
<th>Input Voltage Range (Note 4, Note 5)</th>
<th>$V_{\text{INL}}$</th>
<th>$V_{\text{SS}} - 0.25$</th>
<th>$V_{\text{SS}} - 0.15$</th>
<th>$V_{\text{IH}}$</th>
<th>$V_{DD} + 0.15$</th>
<th>$V_{DD} + 0.30$</th>
<th>$V_{\text{REF}}$</th>
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<tbody>
<tr>
<td>Common Mode Rejection Ratio</td>
<td>CMRR</td>
<td>80</td>
<td>98</td>
<td>—</td>
<td>VCM = $V_{\text{INL}}$ to $V_{\text{IH}}$, $V_{DD} = 1.8$V</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>94</td>
<td>112</td>
<td>—</td>
<td>10</td>
<td>100</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>103</td>
<td>121</td>
<td>—</td>
<td>1</td>
<td>$V_{CM} = V_{\text{INL}}$ to $V_{\text{IH}}$, $V_{DD} = 5.5$V</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>89</td>
<td>107</td>
<td>—</td>
<td>10</td>
<td>100</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>103</td>
<td>121</td>
<td>—</td>
<td>100</td>
<td>100</td>
<td>—</td>
</tr>
<tr>
<td>Common Mode Rejection Ratio at $V_{\text{REF}}$</td>
<td>CMRR2</td>
<td>83</td>
<td>101</td>
<td>—</td>
<td>VREF = 0.2V to $V_{DD} - 0.2$V, $V_{DD} = 1.8$V</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>98</td>
<td>116</td>
<td>—</td>
<td>10</td>
<td>100</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>102</td>
<td>120</td>
<td>—</td>
<td>100</td>
<td>100</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>94</td>
<td>112</td>
<td>—</td>
<td>1</td>
<td>$V_{REF} = 0.2V$ to $V_{DD} - 0.2$V, $V_{DD} = 5.5$V</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>109</td>
<td>127</td>
<td>—</td>
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<td>100</td>
<td>—</td>
</tr>
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<td></td>
<td></td>
<td>115</td>
<td>133</td>
<td>—</td>
<td>100</td>
<td>100</td>
<td>—</td>
</tr>
</tbody>
</table>

**Note 1:** $V_{CM} = (V_{IP} + V_{IM})/2$, $V_{DM} = (V_{IP} - V_{IM})$ and $G_{DM} = 1 + R_F/R_G$.

**Note 2:** For Design Guidance only; not tested.

**Note 3:** These specifications apply to the $V_{IP}$ $V_{IM}$ input pair (use $V_{CM}$) and to the $V_{REF}$ $V_{FG}$ input pair (use $V_{REF}$ instead).

**Note 4:** This specification applies to the $V_{IP}$ $V_{IM}$, $V_{REF}$ and $V_{FG}$ pins individually.

**Note 5:** Figures 2-52 and 2-53 show the $V_{\text{INL}}$, $V_{\text{IH}}$, $V_{\text{DM}}$ and $V_{\text{DM}}$ variation over temperature.

**Note 6:** See Section 1.5 “Explanation of DC Error Specifications”.

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### TABLE 1-1: DC ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = 1.8V$ to 5.5V, $V_{SS} = GND$, $V_{CM} = V_{DD}/2$, $V_{DM} = 0V$, $V_{REF} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10 \, k\Omega$ to $V_L$, $G_{DM} = G_{MIN}$ and $EN = V_{DD}$; see Figures 1-7 and 1-8 (Note 1).

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym.</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>$G_{MIN}$</th>
<th>Conditions</th>
</tr>
</thead>
</table>
| Common Mode Nonlinearity (Note 6) | $INL_{CM}$ | -550 | — | +550 | ppm | 1 | $V_{CM} = V_{IVL}$ to $V_{IVH}$, $V_{DD} = 1.8V$
| | | -75 | — | +75 | | 10 | |
| | | -20 | — | +20 | | 100 | |
| | | -310 | — | +310 | | 1 | $V_{CM} = V_{IVL}$ to $V_{IVH}$, $V_{DD} = 5.5V$
| | | -35 | — | +35 | | 10 | |
| | | -10 | — | +10 | | 100 | |
| Input Differential Voltage ($V_{DM}$) (Note 3) | $V_{DML}$ | — | -3.4/$G_{MIN}$ | -2.7/$G_{MIN}$ | $V$ | all | $V_{DD} \geq 2.9V$, $V_{REF} = V_{DD}$, $V_{OUT}$ within $\pm0.2\%$
| | | | | | | | $V_{DD} \geq 2.9V$, $V_{REF} = 0V$, $V_{OUT}$ within $\pm2\%$
| | $V_{DMH}$ | +2.7/$G_{MIN}$ | +3.4/$G_{MIN}$ | — | | | |
| Differential Gain Error (Note 6) | $g_E$ | — | ±0.03 | — | % | 1 | $V_{DD} = 1.8V$, $V_{REF} = V_{DD}/2$, $V_{DM} = \pm(0.7V)/G_{MIN}$
| | | — | ±0.02 | — | % | 10, 100 | |
| | | — | ±0.03 | — | % | 10, 100 | |
| | | — | ±0.02 | — | % | 10, 100 | |
| | | -0.25 | ±0.04 | +0.25 | % | 1 | $V_{DD} = 5.5V$, $V_{REF} = V_{DD}/2$, $V_{DM} = \pm(2.55V)/G_{MIN}$
| | | -0.15 | ±0.02 | +0.15 | % | 10, 100 | |
| | | -0.25 | ±0.04 | +0.25 | % | 1 | $V_{DD} = 5.5V$, $V_{REF} = 0.2V$, $V_{DM} = 0$ to (2.7V)/$G_{MIN}$
| | | -0.15 | ±0.02 | +0.15 | % | 10, 100 | |

Note 1: $V_{CM} = (V_{IP} + V_{IM})/2$, $V_{DM} = (V_{IP} - V_{IM})$ and $G_{DM} = 1 + R_{F}/R_{G}$.

2: For Design Guidance only; not tested.

3: These specifications apply to the $V_{IP}$, $V_{IM}$ input pair (use $V_{CM}$) and to the $V_{REF}$, $V_{FG}$ input pair (use $V_{REF}$ instead).

4: This specification applies to the $V_{IP}$, $V_{IM}$, $V_{REF}$ and $V_{FG}$ pins individually.

5: Figures 2-52 and 2-53 show the $V_{IVL}$, $V_{IVH}$, $V_{DML}$ and $V_{DMH}$ variation over temperature.

6: See Section 1.5 “Explanation of DC Error Specifications”.

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### Differential Gain Drift (Note 6)

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym.</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>G\textsubscript{MIN}</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Δg\textsubscript{E}/ΔT\textsubscript{A}</td>
<td>—</td>
<td>±3</td>
<td>—</td>
<td>—</td>
<td>ppm/°C</td>
<td>all</td>
<td>V\textsubscript{DD} = 1.8V, V\textsubscript{REF} = V\textsubscript{DD}/2, V\textsubscript{DM} = ±(0.7V)/G\textsubscript{MIN}</td>
</tr>
<tr>
<td></td>
<td>—</td>
<td>±4</td>
<td>—</td>
<td>—</td>
<td></td>
<td></td>
<td>V\textsubscript{DD} = 5.5V, V\textsubscript{REF} = V\textsubscript{DD}/2, V\textsubscript{DM} = ±(2.55V)/G\textsubscript{MIN}</td>
</tr>
<tr>
<td></td>
<td>—</td>
<td>±4</td>
<td>—</td>
<td>—</td>
<td></td>
<td></td>
<td>V\textsubscript{DD} = 5.5V, V\textsubscript{REF} = 0.2V, V\textsubscript{DM} = 0 to (2.7V)/G\textsubscript{MIN}</td>
</tr>
<tr>
<td></td>
<td>—</td>
<td>±3</td>
<td>—</td>
<td>—</td>
<td></td>
<td></td>
<td>V\textsubscript{DD} = 5.5V, V\textsubscript{REF} = 5.3V, V\textsubscript{DM} = 0 to (-2.7V)/G\textsubscript{MIN}</td>
</tr>
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</table>

### Differential Nonlinearity (Note 6)

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym.</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>G\textsubscript{MIN}</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>INL\textsubscript{DM}</td>
<td>—</td>
<td>±300</td>
<td>—</td>
<td>—</td>
<td>ppm</td>
<td>all</td>
<td>V\textsubscript{DD} = 1.8V, V\textsubscript{REF} = V\textsubscript{DD}/2, V\textsubscript{DM} = ±(0.7V)/G\textsubscript{MIN}</td>
</tr>
<tr>
<td></td>
<td>—</td>
<td>±150</td>
<td>—</td>
<td>—</td>
<td></td>
<td></td>
<td>V\textsubscript{DD} = 5.5V, V\textsubscript{REF} = V\textsubscript{DD}/2, V\textsubscript{DM} = ±(2.55V)/G\textsubscript{MIN}</td>
</tr>
<tr>
<td></td>
<td>—</td>
<td>±300</td>
<td>—</td>
<td>—</td>
<td></td>
<td></td>
<td>V\textsubscript{DD} = 5.5V, V\textsubscript{REF} = 0.2V, V\textsubscript{DM} = 0 to (2.7V)/G\textsubscript{MIN}</td>
</tr>
<tr>
<td></td>
<td>—</td>
<td>±300</td>
<td>—</td>
<td>—</td>
<td></td>
<td></td>
<td>V\textsubscript{DD} = 5.5V, V\textsubscript{REF} = 5.3V, V\textsubscript{DM} = 0 to (-2.7V)/G\textsubscript{MIN}</td>
</tr>
</tbody>
</table>

### DC Open-Loop Gain

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym.</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>G\textsubscript{MIN}</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>A\textsubscript{OL}</td>
<td>84</td>
<td>102</td>
<td>—</td>
<td>—</td>
<td>dB</td>
<td>1</td>
<td>V\textsubscript{DD} = 1.8V, V\textsubscript{OUT} = 0.2V to 1.6V</td>
</tr>
<tr>
<td></td>
<td>100</td>
<td>118</td>
<td>—</td>
<td>—</td>
<td></td>
<td>10</td>
<td></td>
</tr>
<tr>
<td></td>
<td>108</td>
<td>126</td>
<td>—</td>
<td>—</td>
<td></td>
<td>100</td>
<td></td>
</tr>
<tr>
<td></td>
<td>95</td>
<td>113</td>
<td>—</td>
<td>—</td>
<td></td>
<td>1</td>
<td>V\textsubscript{DD} = 5.5V, V\textsubscript{OUT} = 0.2V to 5.3V</td>
</tr>
<tr>
<td></td>
<td>111</td>
<td>129</td>
<td>—</td>
<td>—</td>
<td></td>
<td>10</td>
<td></td>
</tr>
<tr>
<td></td>
<td>119</td>
<td>137</td>
<td>—</td>
<td>—</td>
<td></td>
<td>100</td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** V\textsubscript{CM} = (V\textsubscript{IP} + V\textsubscript{IM})/2, V\textsubscript{DM} = (V\textsubscript{IP} – V\textsubscript{IM}) and G\textsubscript{DM} = 1 + R\textsubscript{F}/R\textsubscript{G}.

**2:** For Design Guidance only; not tested.

**3:** These specifications apply to the V\textsubscript{IP}, V\textsubscript{IM} input pair (use V\textsubscript{CM}) and to the V\textsubscript{REF}, V\textsubscript{FG} input pair (use V\textsubscript{REF} instead).

**4:** This specification applies to the V\textsubscript{IP}, V\textsubscript{IM}, V\textsubscript{REF} and V\textsubscript{FG} pins individually.

**5:** Figures 2-52 and 2-53 show the V\textsubscript{VIL}, V\textsubscript{IVH}, V\textsubscript{DMH} and V\textsubscript{DML} variation over temperature.

**6:** See Section 1.5 “Explanation of DC Error Specifications”.

---

**Electrical Characteristics:** Unless otherwise indicated, T\textsubscript{A} = +25°C, V\textsubscript{DD} = 1.8V to 5.5V, V\textsubscript{SS} = GND, V\textsubscript{CM} = V\textsubscript{DD}/2, V\textsubscript{DM} = 0V, V\textsubscript{REF} = V\textsubscript{DD}/2, V\textsubscript{L} = V\textsubscript{DD}/2, R\textsubscript{L} = 10 kΩ to V\textsubscript{L}, G\textsubscript{DM} = G\textsubscript{MIN} and EN = V\textsubscript{DD}; see Figures 1-7 and 1-8 (Note 1).
**TABLE 1-1: DC ELECTRICAL SPECIFICATIONS (CONTINUED)**

Electrical Characteristics: Unless otherwise indicated, \(T_A = +25^\circ C, V_{DD} = 1.8V\) to 5.5V, \(V_{SS} = GND, V_{CM} = V_{DD}/2, V_{DM} = 0V, V_{REF} = V_{DD}/2, V_L = V_{DD}/2, R_L = 10k\ \Omega\) to \(V_L, G_{DM} = G_{MIN}\) and \(EN = V_{DD}\); see Figures 1-7 and 1-8** *(Note 1).*

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym.</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>(G_{MIN})</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Output</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Minimum Output Voltage Swing</td>
<td>(V_{OL})</td>
<td>—</td>
<td>(V_{SS} + 3)</td>
<td>—</td>
<td>mV</td>
<td>all</td>
<td>(R_L = 10\ \Omega, V_{DD} = 1.8V, V_{DM} = V_{DD}/2G_{MIN}, V_{REF} = V_{DD}/2 – 0.9V)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>(R_L = 10\ \Omega, V_{DD} = 5.5V, V_{DM} = V_{DD}/2G_{MIN}, V_{REF} = V_{DD}/2 – 1V)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>(R_L = 1\ \Omega, V_{DD} = 5.5V, V_{DM} = V_{DD}/2G_{MIN}, V_{REF} = V_{DD}/2 – 1V)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Maximum Output Voltage Swing</td>
<td>(V_{OH})</td>
<td>—</td>
<td>(V_{DD} – 3)</td>
<td>—</td>
<td>mV</td>
<td></td>
<td>(R_L = 10\ \Omega, V_{DD} = 1.8V, V_{DM} = V_{DD}/2G_{MIN}, V_{REF} = V_{DD}/2 + 0.9V)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>(R_L = 10\ \Omega, V_{DD} = 5.5V, V_{DM} = V_{DD}/2G_{MIN}, V_{REF} = V_{DD}/2 + 1V)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>(R_L = 1\ \Omega, V_{DD} = 5.5V, V_{DM} = V_{DD}/2G_{MIN}, V_{REF} = V_{DD}/2 + 1V)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Short-Circuit Current</td>
<td>(I_{SC})</td>
<td>—</td>
<td>±10</td>
<td>—</td>
<td>mA</td>
<td></td>
<td>(V_{DD} = 1.8V)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>±35</td>
<td>—</td>
<td></td>
<td></td>
<td>(V_{DD} = 5.5V)</td>
</tr>
</tbody>
</table>

**Power Supply**

<table>
<thead>
<tr>
<th></th>
<th>(V_{DD})</th>
<th>1.8</th>
<th></th>
<th>5.5</th>
<th>V</th>
<th>all</th>
</tr>
</thead>
<tbody>
<tr>
<td>Quiescent Current per Amplifier</td>
<td>(I_O)</td>
<td>0.5</td>
<td>1.1</td>
<td>1.6</td>
<td>mA</td>
<td>(I_O = 0)</td>
</tr>
<tr>
<td>POR Trip Voltage</td>
<td>(V_{PRL})</td>
<td>0.9</td>
<td>1.27</td>
<td>—</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(V_{PRH})</td>
<td></td>
<td>1.33</td>
<td>1.6</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** \(V_{CM} = (V_{IP} + V_{IM})/2, V_{DM} = (V_{IP} – V_{IM})\) and \(G_{DM} = 1 + R_F/R_G\).

**2:** For Design Guidance only; not tested.

**3:** These specifications apply to the \(V_{IP}, V_{IM}\) input pair (use \(V_{CM}\)) and to the \(V_{REF}, V_{FG}\) input pair (use \(V_{REF}\) instead).

**4:** This specification applies to the \(V_{IP}, V_{IM}, V_{REF}\) and \(V_{FG}\) pins individually.

**5:** Figures 2-52 and 2-53 show the \(V_{IVL}, V_{IVH}, V_{DML}\) and \(V_{DMH}\) variation over temperature.

**6:** See Section 1.5 “Explanation of DC Error Specifications.”
### TABLE 1-2: AC ELECTRICAL SPECIFICATIONS

**Electrical Characteristics:** Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = 1.8V$ to $5.5V$, $V_{SS} = GND$, $V_{CM} = V_{DD}/2$, $V_{DM} = 0V$, $V_{REF} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10 \, k\Omega$ to $V_L$, $C_L = 60 \, pF$, $G_{DM} = G_{MIN}$ and $EN = V_{DD}$; see Figures 1-7 and 1-8.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym.</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>$G_{MIN}$</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Gain-Bandwidth Product</strong></td>
<td>GBWP</td>
<td>—</td>
<td>0.5</td>
<td>—</td>
<td>MHz</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>5</td>
<td>—</td>
<td></td>
<td>10</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>35</td>
<td>—</td>
<td></td>
<td>100</td>
<td></td>
</tr>
<tr>
<td><strong>Phase Margin</strong></td>
<td>PM</td>
<td>—</td>
<td>70</td>
<td>—</td>
<td>°</td>
<td>all</td>
<td></td>
</tr>
<tr>
<td><strong>Open-Loop Output Impedance</strong></td>
<td>$R_{OL}$</td>
<td>—</td>
<td>80</td>
<td>—</td>
<td>kΩ</td>
<td>1</td>
<td>$f = 1 , kHz$</td>
</tr>
<tr>
<td><strong>Power Supply Rejection Ratio</strong></td>
<td>PSRR</td>
<td>—</td>
<td>98</td>
<td>—</td>
<td>dB</td>
<td>10</td>
<td>$f = 1 , kHz$</td>
</tr>
<tr>
<td><strong>Common Mode Rejection Ratio at $V_{CM}$ and $V_{REF}$</strong></td>
<td>CMRR, CMRR2</td>
<td>—</td>
<td>123</td>
<td>—</td>
<td></td>
<td>100</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>90</td>
<td>—</td>
<td></td>
<td>100</td>
<td></td>
</tr>
<tr>
<td><strong>Step Rate (see Section 4.1.4 “AC Performance”)</strong></td>
<td>Note 1</td>
<td>—</td>
<td>83</td>
<td>—</td>
<td>dB</td>
<td>1</td>
<td>$f = 10 , kHz$</td>
</tr>
<tr>
<td><strong>Overdrive Recovery, Input Common Mode</strong></td>
<td>$t_{IRC}$</td>
<td>—</td>
<td>80</td>
<td>—</td>
<td></td>
<td>10</td>
<td></td>
</tr>
<tr>
<td><strong>Overdrive Recovery, Input Differential Mode</strong></td>
<td>$t_{IRD}$</td>
<td>—</td>
<td>140</td>
<td>—</td>
<td></td>
<td>100</td>
<td></td>
</tr>
<tr>
<td><strong>Overdrive Recovery, Output</strong></td>
<td>$t_{OR}$</td>
<td>—</td>
<td>180</td>
<td>—</td>
<td></td>
<td>100</td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** The slew rate is limited by the GBWP; the large signal step response is dominated by the small signal bandwidth.

**Note 2:** These parameters were characterized using the circuit in Figure 1-8. In Figures 2-75 and 2-76, there is an IMD tone at DC, a residual tone at 100 Hz and other IMD tones and clock tones.

**Note 3:** High gains behave differently; see Section 4.4.4 “Offset at Power-Up”.

**Note 4:** $t_{STR}$, $t_{STL}$, $t_{IRC}$, $t_{IRD}$ and $t_{OR}$ include some uncertainty due to clock edge timing.
TABLE 1-2: AC ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, \( T_A = +25^\circ C, V_{DD} = 1.8V \) to 5.5V, \( V_{SS} = GND, V_{CM} = V_{DD/2}, V_{DM} = 0V, V_{REF} = V_{DD/2}, V_L = V_{DD/2}, R_L = 10 \text{ k}\Omega \) to \( V_L, C_L = 60 \text{ pF}, G_{DM} = G_{\text{MIN}} \) and \( EN = V_{DD}; \) see Figures 1-7 and 1-8.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym.</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>( G_{\text{MIN}} )</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Noise Voltage Density</td>
<td>( e_{ni} )</td>
<td>— 900 —</td>
<td>— 105 —</td>
<td>— 45 —</td>
<td>nV/( \sqrt{Hz} )</td>
<td>1</td>
<td>f = 500 Hz</td>
</tr>
<tr>
<td>Input Noise Voltage</td>
<td>( E_{ni} )</td>
<td>— 19 —</td>
<td>— 2.2 —</td>
<td>— 0.93 —</td>
<td>( \mu V_{P-P} )</td>
<td>1</td>
<td>f = 0.1 Hz to 10 Hz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>10</td>
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<td></td>
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<td>100</td>
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<td>100</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>100</td>
<td></td>
</tr>
<tr>
<td>Input Current Noise Density</td>
<td>( i_{ni} )</td>
<td>— 7 —</td>
<td>— 0.69 —</td>
<td>— 0.30 —</td>
<td>fA/( \sqrt{Hz} )</td>
<td>all</td>
<td>f = 1 kHz</td>
</tr>
<tr>
<td>Output Noise Voltage Density</td>
<td>( e_{no} )</td>
<td>0</td>
<td>nV/( \sqrt{Hz} )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Noise Voltage</td>
<td>( E_{no} )</td>
<td>0</td>
<td>( \mu V_{P-P} )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Amplifier Distortion (Note 2)**

| Intermodulation Distortion (AC) | IMD | — 5 — | \( \mu V_{PK} \) | all | \( V_{CM} \) tone = 100 mV_{PK} at 100 Hz |

**EMI Protection**

<table>
<thead>
<tr>
<th>EMI Rejection Ratio</th>
<th>EMIRR</th>
<th>— 103 —</th>
<th>— 106 —</th>
<th>— 106 —</th>
<th>— 111 —</th>
<th>dB</th>
<th>all</th>
<th>( V_{IN} = 0.1 V_{PK}, f = 400 \text{ MHz} )</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>( V_{IN} = 0.1 V_{PK}, f = 900 \text{ MHz} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>( V_{IN} = 0.1 V_{PK}, f = 1800 \text{ MHz} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>( V_{IN} = 0.1 V_{PK}, f = 2400 \text{ MHz} )</td>
</tr>
</tbody>
</table>

**Note 1:** The slew rate is limited by the GBWP; the large signal step response is dominated by the small signal bandwidth.

**Note 2:** These parameters were characterized using the circuit in Figure 1-8. In Figures 2-75 and 2-76, there is an IMD tone at DC, a residual tone at 100 Hz and other IMD tones and clock tones.

**Note 3:** High gains behave differently; see Section 4.4.4 “Offset at Power-Up”.

**Note 4:** \( t_{\text{STR}}, t_{\text{STL}}, t_{\text{IRC}}, t_{\text{IRD}} \) and \( t_{\text{OR}} \) include some uncertainty due to clock edge timing.
## TABLE 1-3: DIGITAL ELECTRICAL SPECIFICATIONS

**Electrical Characteristics:** Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = 1.8V$ to $5.5V$, $V_{SS} = GND$, $V_{CM} = V_{DD}/2$, $V_{DM} = 0V$, $V_{REF} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10$ kΩ to $V_L$, $C_L = 60$ pF, $G_{DM} = G_{MIN}$ and $EN = V_{DD}$; see Figures 1-7 and 1-8.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym.</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>EN Low Specifications</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EN Logic Threshold, Low</td>
<td>$V_{IL}$</td>
<td>—</td>
<td>—</td>
<td>0.2$V_{DD}$</td>
<td>$V$</td>
<td>all EN = 0V</td>
</tr>
<tr>
<td>EN Input Current, Low</td>
<td>$I_{ENL}$</td>
<td>—</td>
<td>-10</td>
<td>—</td>
<td>pA</td>
<td>$EN = 0V$</td>
</tr>
<tr>
<td>GND Current</td>
<td>$I_{SS}$</td>
<td>-8</td>
<td>-2</td>
<td>—</td>
<td>µA</td>
<td>$EN = 0V, V_{DD} = 5.5V$</td>
</tr>
<tr>
<td>Amplifier Output Leakage</td>
<td>$I_{O(LEAK)}$</td>
<td>—</td>
<td>-1</td>
<td>—</td>
<td>nA</td>
<td>$EN = 0V$</td>
</tr>
<tr>
<td><strong>EN High Specifications</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EN Logic Threshold, High</td>
<td>$V_{IH}$</td>
<td>0.8$V_{DD}$</td>
<td>—</td>
<td>—</td>
<td>$V$</td>
<td>all $EN = V_{DD}$</td>
</tr>
<tr>
<td>EN Input Current, High</td>
<td>$I_{ENH}$</td>
<td>—</td>
<td>10</td>
<td>—</td>
<td>pA</td>
<td>$EN = V_{DD}$</td>
</tr>
<tr>
<td><strong>EN Dynamic Specifications</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EN Input Hysteresis</td>
<td>$V_{HYST}$</td>
<td>—</td>
<td>0.16$V_{DD}$</td>
<td>—</td>
<td>$V$</td>
<td>all $EN = 0V$ to $V_{OUT} = 0.1(V_{DD}/2)$, $V_L = 0V$</td>
</tr>
<tr>
<td>EN Input Resistance</td>
<td>$R_{PD}$</td>
<td>—</td>
<td>$10^{13}$</td>
<td>—</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>EN Low to Amplifier Output High Z Turn-Off Time</td>
<td>$t_{OFF}$</td>
<td>—</td>
<td>0.1</td>
<td>2</td>
<td>µs</td>
<td>$EN = 0V$ to $V_{OUT} = 0.1(V_{DD}/2)$, $V_L = 0V$</td>
</tr>
<tr>
<td>EN High to Amplifier Output On Time</td>
<td>$t_{ON}$</td>
<td>—</td>
<td>12</td>
<td>100</td>
<td></td>
<td>$V_{DD} = 1.8V$, $EN = 0.8V_{DD}$ to $V_{OUT} = 0.9(V_{DD}/2)$, $V_L = 0V$</td>
</tr>
<tr>
<td>EN Low to EN High hold time</td>
<td>$t_{ENLH}$</td>
<td>50</td>
<td>—</td>
<td>—</td>
<td></td>
<td>Minimum time before releasing EN (Note 1)</td>
</tr>
<tr>
<td>EN High to EN Low setup time</td>
<td>$t_{ENHL}$</td>
<td>50</td>
<td>—</td>
<td>—</td>
<td></td>
<td>Minimum time before exerting EN (Note 1)</td>
</tr>
<tr>
<td><strong>POR Dynamic Specifications</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{DD} \downarrow$ to Output Off</td>
<td>$t_{PHL}$</td>
<td>—</td>
<td>10</td>
<td>—</td>
<td>µs</td>
<td>all $V_L = 0V$, $V_{DD} = 1.8V$ to $V_{PRL} = 0.1V$ step, 90% of $V_{OUT}$ change</td>
</tr>
<tr>
<td>$V_{DD} \uparrow$ to Output On</td>
<td>$t_{PLH}$</td>
<td>—</td>
<td>100</td>
<td>—</td>
<td></td>
<td>$V_L = 0V$, $V_{DD} = 0V$ to $V_{PRH} + 0.1V$ step, 90% of $V_{OUT}$ change</td>
</tr>
</tbody>
</table>

**Note 1:** For design guidance only; not tested.
### TABLE 1-4: TEMPERATURE SPECIFICATIONS

**Electrical Characteristics**: Unless otherwise indicated, all limits are specified for: \( V_{DD} = 1.8V \) to 5.5V, \( V_{SS} = GND \).

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym.</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature Ranges</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Specified Temperature Range</td>
<td>( T_A )</td>
<td>-40</td>
<td>—</td>
<td>+125</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>( T_A )</td>
<td>-40</td>
<td>—</td>
<td>+125</td>
<td></td>
<td><strong>Note 1</strong></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>( T_A )</td>
<td>-65</td>
<td>—</td>
<td>+150</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Thermal Package Resistances**

<table>
<thead>
<tr>
<th>Parameters</th>
<th>( \theta_{JA} )</th>
<th>—</th>
<th>57</th>
<th>—</th>
<th>°C/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal Resistance, 8L-DFN (3×3)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal Resistance, 8L-MSOP</td>
<td></td>
<td></td>
<td>211</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note 1**: Operation must not cause \( T_J \) to exceed the Absolute Maximum Junction Temperature specification (+150°C).
1.3 Timing Diagrams

**FIGURE 1-1:** Amplifier Start-Up Timing Diagram.

**FIGURE 1-2:** Common Mode Input Overdrive Recovery Timing Diagram.

**FIGURE 1-3:** Differential Mode Input Overdrive Recovery Timing Diagram.

**FIGURE 1-4:** Output Overdrive Recovery Timing Diagram.

**FIGURE 1-5:** POR Timing Diagram.

**FIGURE 1-6:** EN Timing Diagram.
1.4 DC Test Circuits

1.4.1 INPUT OFFSET TEST CIRCUIT

Figure 1-7 is a simple circuit that can test the INA's input offset errors and input voltage range (V_E, V_{IVL} and V_{IVH}; see Section 1.5.1 “Input Offset Related Errors” and Section 1.5.2 “Input Offset Common Mode Nonlinearity”). U_2 is part of a control loop that forces V_{OUT} to equal V_{CNT}; U_1 can be set to any bias point.

![Figure 1-7: Simple Test Circuit for Common Mode (Input Offset).](image)

When MCP6N16 is in its normal range of operation, the DC output voltages are (where V_E is the sum of input offset errors and g_E is the gain error):

**EQUATION 1-1:**

\[
G_{DM} = I + R_F/R_G
\]

\[
V_{OUT} = V_{REF} + G_{DM}(I + g_E)(V_{DM} + V_E)
\]

\[
V_M = V_{REF} + G_{DM}(I + g_E)(V_{DM} + V_E)
\]

Table 1-5 shows the resulting behavior for different G_{MIN} options.

**TABLE 1-5: RESULTS**

<table>
<thead>
<tr>
<th>G_{MIN} (V/V)</th>
<th>R_F (kΩ)</th>
<th>G_{DM} (kV/V)</th>
<th>G_{DM} V_{OS} (±mV)</th>
<th>BW (kHz) Typ. at V_{OUT}</th>
<th>BW (Hz) Typ. at V_M</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>100</td>
<td>1.00</td>
<td>85</td>
<td>0.50</td>
<td>0.50</td>
</tr>
<tr>
<td>10</td>
<td>402</td>
<td>4.02</td>
<td>88</td>
<td>1.2</td>
<td></td>
</tr>
<tr>
<td>100</td>
<td></td>
<td>68</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1.4.2 DIFFERENTIAL GAIN TEST CIRCUIT

Figure 1-8 is a simple circuit that can test the INA's differential gain error, nonlinearity and input voltage range (g_E, INL_{DM}, V_{DM L} and V_{DM H}; see Section 1.5.3 “Differential Gain Error and Nonlinearity”). R_F and R_G are 0.01% for accurate gain error measurements. The output voltages are (where V_E is the sum of input offset errors and g_E is the gain error):

**EQUATION 1-2:**

\[
G_{DM} = I + R_F/R_G
\]

\[
V_{OUT} = V_{REF} + G_{DM}(I + g_E)(V_{DM} + V_E)
\]

\[
V_M = V_{REF} + G_{DM}(I + g_E)(V_{DM} + V_E)
\]

![Figure 1-8: Simple Test Circuit for Differential Mode.](image)

For different values of V_{REF}, V_{DM} sweeps over different ranges to keep V_{REF}, V_{FG} and V_{OUT} within their ranges.

Table 1-6 shows the recommended R_F and R_G; they produce a 10 kΩ load. V_L can usually be left open.

**TABLE 1-6: SELECTING R_F AND R_G**

<table>
<thead>
<tr>
<th>G_{MIN} (V/V)</th>
<th>R_F (kΩ)</th>
<th>R_G (kΩ)</th>
<th>G_{DM} (V/V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>100</td>
<td>1.00</td>
<td>85</td>
</tr>
<tr>
<td>10</td>
<td>402</td>
<td>4.02</td>
<td>88</td>
</tr>
<tr>
<td>100</td>
<td>68</td>
<td>8.7</td>
<td></td>
</tr>
</tbody>
</table>

1.4.3 DYNAMIC TESTING OF INPUT BEHAVIOR

The circuit in Figure 1-8 can test the input’s dynamic behavior (i.e., IMD, t_{STR}, t_{STL}, t_{IRC}, t_{IRD} and t_{OR}); measure the output at V_{OUT}, instead of at V_M.
1.5 Explanation of DC Error Specifications

1.5.1 INPUT OFFSET RELATED ERRORS

The input offset error (VE) is extracted from input offset measurements (see Section 1.4.1 “Input Offset Test Circuit”), based on Equation 1-1:

\[ V_E = (V_M - V_{REF})/(G_{DM}(1 + g_E)) \]

VE has several terms, which assume a linear response to changes in VDD, VSS, VCM, VOUT and TA (all of which are in their specified ranges):

\[ V_E = V_{OS} + \frac{\Delta V_{DD} - \Delta V_{SS}}{PSRR} + \frac{\Delta V_{CM}}{CMRR} + \frac{\Delta V_{REF}}{CMRR2} \]

\[ + \frac{\Delta V_{OUT}}{A_{OL}} + \Delta T_A \cdot TC_1 \]

Where:

- PSRR, CMRR, CMRR2 and A_{OL} are in units of V/V
- \Delta T_A is in units of °C
- TC_1 is in units of V/°C
- V_{DM} = 0

Equation 1-2 shows how VE affects VOUT.

1.5.2 INPUT OFFSET COMMON MODE NONLINEARITY

The input offset error (VE) changes nonlinearly with VCM. Figure 1-9 shows VE vs. VCM, as well as a linear fit line (VE_LIN) based on VOS and CMRR. The INA is in standard conditions (\( \Delta V_{OUT} = 0, \Delta V_{DM} = 0 \), etc.). VCM is swept from V_{IVL} to V_{IVH}. The test circuit is in Section 1.4.1 “Input Offset Test Circuit” and VE is calculated using Equation 1-3.

\[ \Delta V_E = V_E - V_{E, LIN} \]

Based on the measured VE data, we obtain the following linear fit:

\[ V_{E, LIN} = V_{OS} + (V_{CM} - V_{DD}/2)/CMRR \]

\[ I/CMRR = (V_2 - V_1)/(V_{IVH} - V_{IVL}) \]

The remaining error (\( \Delta V_E \)) is described by the Common Mode Nonlinearity spec:

\[ INL_{CMH} = \max (\Delta V_E)/(V_{IVH} - V_{IVL}) \]

\[ INL_{CML} = \min (\Delta V_E)/(V_{IVH} - V_{IVL}) \]

\[ INL_{CM} = INL_{CMH}, \quad \text{if } |INL_{CMH}| > |INL_{CML}| \]

\[ = INL_{CML}, \quad \text{otherwise} \]

Where:

\[ \Delta V_E = V_E - V_{E, LIN} \]

The same common mode behavior applies to VE when VREF is swept, instead of VCM, since both input stages are designed the same:

\[ V_{E, LIN2} = V_{OS} + (V_{REF} - V_{DD}/2)/CMRR2 \]

\[ INL_{CMH2} = \max (\Delta V_{E2})/(V_{IVH} - V_{IVL}) \]

\[ INL_{CML2} = \min (\Delta V_{E2})/(V_{IVH} - V_{IVL}) \]

\[ INL_{CM2} = INL_{CMH2}, \quad \text{if } |INL_{CMH2}| > |INL_{CML2}| \]

\[ = INL_{CML2}, \quad \text{otherwise} \]

Where:

\[ \Delta V_{E2} = V_E - V_{E, LIN2} \]
1.5.3 DIFFERENTIAL GAIN ERROR AND NONLINEARITY

The differential errors are extracted from differential gain measurements (see Section 1.4.2 “Differential Gain Test Circuit”), based on Equation 1-2. These errors are the differential gain error ($g_E$) and the input offset error ($V_E$, which changes nonlinearly with $V_{DM}$):

**EQUATION 1-8:**

$$G_{DM} = I + R_F/R_G$$
$$V_M = G_{DM}(1 + g_E)(V_{DM} + V_E)$$

These errors are adjusted for the expected output, then referred back to the input, giving the differential input error ($V_{ED}$) as a function of $V_{DM}$:

**EQUATION 1-9:**

$$V_{ED} = V_M/G_{DM} - V_{DM}$$

Figure 1-10 shows $V_{ED}$ vs. $V_{DM}$, as well as a linear fit line ($V_{ED\_LIN}$) based on $V_{ED}$ and $g_E$. The INA is in standard conditions ($\Delta V_{OUT} = 0$, etc.). $V_{DM}$ is swept from $V_{DML}$ to $V_{DMH}$.

**FIGURE 1-10:** Differential Input Error vs. Differential Input Voltage.

Based on the measured $V_{ED}$ data, we obtain the following linear fit:

**EQUATION 1-10:**

$$V_{ED\_LIN} = (1 + g_E)V_E + g_E V_{DM}$$

Where:

$$g_E = (V_3 - V_1)/(V_{DMH} - V_{DML}) - 1$$
$$V_E = V_2/(1 + g_E)$$

Note that the $V_E$ value measured here is not as accurate as the one obtained in Section 1.5.1 “Input Offset Related Errors”.

The remaining error ($\Delta V_{ED}$) is described by the Differential Nonlinearity spec:

**EQUATION 1-11:**

$$INL_{DMH} = \max(\Delta V_{ED})/(V_{DMH} - V_{DML})$$
$$INL_{DML} = \min(\Delta V_{ED})/(V_{DMH} - V_{DML})$$

Where:

$$\Delta V_{ED} = V_{ED} - V_{ED\_LIN}$$

$$|INL_{DMH}| \geq |INL_{DML}|$$

otherwise
2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, $T_A = +25^\circ\text{C}$, $V_{DD} = 1.8\text{V}$ to 5.5V, $V_{SS} = \text{GND}$, $V_{CM} = V_{DD}/2$, $V_{DM} = 0\text{V}$, $V_{REF} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10\text{k}\Omega$ to $V_L$, $C_L = 60\text{pF}$, $G_{DM} = G_{\text{MIN}}$ and $EN = V_{DD}$; see Figures 1-7 and 1-8.

2.1 DC Precision

FIGURE 2-1: Input Offset Voltage, with $G_{\text{MIN}} = 1$.

FIGURE 2-2: Input Offset Voltage, with $G_{\text{MIN}} = 10$.

FIGURE 2-3: Input Offset Voltage, with $G_{\text{MIN}} = 100$.

FIGURE 2-4: Input Offset Voltage Drift, with $G_{\text{MIN}} = 1$.

FIGURE 2-5: Input Offset Voltage Drift, with $G_{\text{MIN}} = 10$.

FIGURE 2-6: Input Offset Voltage Drift, with $G_{\text{MIN}} = 100$. 
Note: Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = 1.8V$ to $5.5V$, $V_{SS} = GND$, $V_{CM} = V_{DD}/2$, $V_{DM} = 0V$, $V_{REF} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10\ 0\Omega$ to $V_L$, $C_L = 60\ \mu F$, $G_{DM} = G_{MIN}$ and $EN = V_{DD}$; see Figures 1-7 and 1-8.
**Note:** Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = 1.8V$ to $5.5V$, $V_{SS} = GND$, $V_{CM} = V_{DD}/2$, $V_{DM} = 0V$, $V_{REF} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10\, k\Omega$ to $V_L$, $C_L = 60\, pF$, $G_{DM} = G_{MIN}$ and $EN = V_{DD}$; see Figures 1-7 and 1-8.

**FIGURE 2-13:** Input Offset Voltage vs. Power Supply Voltage, with $V_{CM} = 0V$ and $G_{MIN} = 1$.

**FIGURE 2-14:** Input Offset Voltage vs. Power Supply Voltage, with $V_{CM} = 0V$ and $G_{MIN} = 10$.

**FIGURE 2-15:** Input Offset Voltage vs. Power Supply Voltage, with $V_{CM} = 0V$ and $G_{MIN} = 100$.

**FIGURE 2-16:** Input Offset Voltage vs. Power Supply Voltage, with $V_{CM} = V_{DD}$ and $G_{MIN} = 1$.

**FIGURE 2-17:** Input Offset Voltage vs. Power Supply Voltage, with $V_{CM} = V_{DD}$ and $G_{MIN} = 10$.

**FIGURE 2-18:** Input Offset Voltage vs. Power Supply Voltage, with $V_{CM} = V_{DD}$ and $G_{MIN} = 100$. 
Note: Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = 1.8V$ to 5.5V, $V_{SS} = GND$, $V_{CM} = V_{DD}/2$, $V_{DM} = 0V$, $V_{REF} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10 \, k\Omega$ to $V_L$, $C_L = 60 \, pF$, $G_{DM} = G_{MIN}$ and $EN = V_{DD}$; see Figures 1-7 and 1-8.

**FIGURE 2-19:** Input Offset Voltage vs. Common Mode Voltage, with $V_{DD} = 1.8V$ and $G_{MIN} = 1$.

**FIGURE 2-20:** Input Offset Voltage vs. Common Mode Voltage, with $V_{DD} = 1.8V$ and $G_{MIN} = 10$.

**FIGURE 2-21:** Input Offset Voltage vs. Common Mode Voltage, with $V_{DD} = 1.8V$ and $G_{MIN} = 100$.

**FIGURE 2-22:** Input Offset Voltage vs. Common Mode Voltage, with $V_{DD} = 5.5V$ and $G_{MIN} = 1$.

**FIGURE 2-23:** Input Offset Voltage vs. Common Mode Voltage, with $V_{DD} = 5.5V$ and $G_{MIN} = 10$.

**FIGURE 2-24:** Input Offset Voltage vs. Common Mode Voltage, with $V_{DD} = 5.5V$ and $G_{MIN} = 100$. 
Note: Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = 1.8V$ to 5.5V, $V_{SS} = GND$, $V_{CM} = V_{DD}/2$, $V_{DM} = 0V$, $V_{REF} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10$ kΩ to $V_L$, $C_L = 60$ pF, $G_{DM} = G_{MIN}$ and $EN = V_{DD}$; see Figures 1-7 and 1-8.

**FIGURE 2-25:** Input Offset Voltage vs. Reference Voltage, with $G_{MIN} = 1$.

**FIGURE 2-26:** Input Offset Voltage vs. Reference Voltage, with $G_{MIN} = 10$.

**FIGURE 2-27:** Input Offset Voltage vs. Reference Voltage, with $G_{MIN} = 100$.

**FIGURE 2-28:** CMRR, with $G_{MIN} = 1$.

**FIGURE 2-29:** CMRR, with $G_{MIN} = 10$.

**FIGURE 2-30:** CMRR, with $G_{MIN} = 100$. 
Note: Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = 1.8V$ to $5.5V$, $V_{SS} = $ GND, $V_{CM} = V_{DD}/2$, $V_{DM} = 0V$, $V_{REF} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10 \, k\Omega$ to $V_L$, $C_L = 60 \, pF$, $G_{DM} = G_{MIN}$ and $EN = V_{DD}$; see Figures 1-7 and 1-8.

**FIGURE 2-31:** CMRR2, with $G_{MIN} = 1$.

**FIGURE 2-32:** CMRR2, with $G_{MIN} = 10$.

**FIGURE 2-33:** CMRR2, with $G_{MIN} = 100$.

**FIGURE 2-34:** PSRR, with $G_{MIN} = 1$.

**FIGURE 2-35:** PSRR, with $G_{MIN} = 10$.

**FIGURE 2-36:** PSRR, with $G_{MIN} = 100$. 
Note: Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = 1.8V$ to 5.5V, $V_{SS} = GND$, $V_{CM} = V_{DD}/2$, $V_{DM} = 0V$, $V_{REF} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10 \, k\Omega$, $C_L = 60 \, pF$, $G_{DM} = G_{MIN}$ and $EN = V_{DD}$; see Figures 1-7 and 1-8.

**FIGURE 2-37:** DC Open-Loop Gain, with $G_{MIN} = 1$.

**FIGURE 2-38:** DC Open-Loop Gain, with $G_{MIN} = 10$.

**FIGURE 2-39:** DC Open-Loop Gain, with $G_{MIN} = 100$.

**FIGURE 2-40:** CMRR vs. Ambient Temperature.

**FIGURE 2-41:** CMRR2 vs. Ambient Temperature.

**FIGURE 2-42:** PSRR vs. Ambient Temperature.
Note: Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = 1.8V$ to 5.5V, $V_{SS} = GND$, $V_{CM} = V_{DD}/2$, $V_{DM} = 0V$, $V_{REF} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10k\Omega$ to $V_L$, $C_L = 60pF$, $G_{DM} = G_{MIN}$ and $EN = V_{DD}$; see Figures 1-7 and 1-8.

FIGURE 2-43: DC Open-Loop Gain vs. Ambient Temperature.

FIGURE 2-44: Input Bias and Offset Currents vs. Common Mode Input Voltage, with $T_A = +85^\circ C$.

FIGURE 2-45: Input Bias and Offset Currents vs. Common Mode Input Voltage, with $T_A = +125^\circ C$.

FIGURE 2-46: Input Bias and Offset Currents vs. Ambient Temperature, with $V_{DD} = 5.5V$.

FIGURE 2-47: Input Bias Current Magnitude vs. Input Voltage (below $V_{SS}$).

FIGURE 2-48: Gain Error vs. Ambient Temperature.
Note: Unless otherwise indicated, $T_A = +25°C$, $V_{DD} = 1.8V$ to $5.5V$, $V_{SS} = GND$, $V_{CM} = V_{DD}/2$, $V_{DM} = 0V$, $V_{REF} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10\, k\Omega$ to $V_L$, $C_L = 60\, pF$, $G_{DM} = G_{MIN}$ and $EN = V_{DD}$; see Figures 1-7 and 1-8.

**FIGURE 2-49:** Gain Error, with $G_{MIN} = 1$.

**FIGURE 2-50:** Gain Error, with $G_{MIN} = 10$.

**FIGURE 2-51:** Gain Error, with $G_{MIN} = 100$. 
Note: Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = 1.8V$ to 5.5V, $V_{SS} = GND$, $V_{CM} = V_{DD}/2$, $V_{DM} = 0V$, $V_{REF} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10 \, k\Omega$ to $VL$, $C_L = 60 \, pF$, $G_{DM} = G_{MIN}$ and $EN = V_{DD}$; see Figures 1-7 and 1-8.

2.2 Other DC Voltages and Currents

FIGURE 2-52:  Input Voltage Range Headroom vs. Ambient Temperature.

FIGURE 2-53:  Normalized Differential Input Voltage Range vs. Ambient Temperature.

FIGURE 2-54:  Output Voltage Headroom vs. Output Current Magnitude.

FIGURE 2-55:  Output Voltage Headroom vs. Ambient Temperature.

FIGURE 2-56:  Supply Current vs. Power Supply Voltage.

FIGURE 2-57:  Supply Current vs. Common Mode Input Voltage.
Note: Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = 1.8V$ to 5.5V, $V_{SS} = GND$, $V_{CM} = V_{DD}/2$, $V_{DM} = 0V$, $V_{REF} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10 \, k\Omega$ to $V_L$, $C_L = 60 \, pF$, $G_{DM} = G_{MIN}$ and $EN = V_{DD}$; see Figures 1-7 and 1-8.

**FIGURE 2-58:** Output Short-Circuit Current vs. Power Supply Voltage.

**FIGURE 2-59:** Power-On Reset Trip Voltages.

**FIGURE 2-60:** Power-On Reset Trip Voltages vs. Temperature.
Note: Unless otherwise indicated, \( T_A = +25^\circ C \), \( V_{DD} = 1.8V \) to 5.5V, \( V_{SS} = GND \), \( V_{CM} = V_{DD}/2 \), \( V_{DM} = 0V \), \( V_{REF} = V_{DD}/2 \), \( V_L = V_{DD}/2 \), \( R_L = 10 \Omega \) to \( V_L \), \( C_L = 60 \mu F \), \( G_{DM} = G_{MIN} \) and \( EN = V_{DD} \); see Figures 1-7 and 1-8.

2.3 Frequency Response

**FIGURE 2-61:** CMRR vs. Frequency.

**FIGURE 2-62:** PSRR vs. Frequency.

**FIGURE 2-63:** Open-Loop Gain vs. Frequency.

**FIGURE 2-64:** Normalized Gain-Bandwidth Product vs. Ambient Temperature.

**FIGURE 2-65:** Phase Margin vs. Ambient Temperature.

**FIGURE 2-66:** Closed-Loop Output Impedance vs. Frequency.
Note: Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = 1.8$V to 5.5V, $V_{SS} = GND$, $V_{CM} = V_{DD}/2$, $V_{DM} = 0$V, $V_{REF} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10$ k$\Omega$ to $V_L$, $C_L = 60$ pF, $G_{DM} = G_{MIN}$ and $EN = V_{DD}$; see Figures 1-7 and 1-8.

**FIGURE 2-67:** Gain Peaking vs. Normalized Capacitive Load.

**FIGURE 2-68:** EMIRR vs. Frequency, with $V_{IN} = 100$ mVPK.

**FIGURE 2-69:** EMIRR vs. Input Voltage, with $f = 400$ MHz.

**FIGURE 2-70:** EMIRR vs. Input Voltage, with $f = 900$ MHz.

**FIGURE 2-71:** EMIRR vs. Input Voltage, with $f = 1800$ MHz.

**FIGURE 2-72:** EMIRR vs. Input Voltage, with $f = 2400$ MHz.
Note: Unless otherwise indicated, $T_A = +25°C$, $V_{DD} = 1.8V$ to 5.5V, $V_{SS} = GND$, $V_{CM} = V_{DD}/2$, $V_{DM} = 0V$, $V_{REF} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10\,kΩ$ to $V_L$, $C_L = 60\,pF$, $G_{DM} = G_{MIN}$ and $EN = V_{DD}$; see Figures 1-7 and 1-8.

2.4 Noise

**FIGURE 2-73:** Input Noise Voltage Density and Integrated Input Noise Voltage vs. Frequency.

**FIGURE 2-74:** Input Noise Voltage Density vs. Input Common Mode Voltage.

**FIGURE 2-75:** Intermodulation Distortion vs. Frequency with $V_{CM}$ Disturbance (see Figure 1-8).

**FIGURE 2-76:** Intermodulation Distortion vs. Frequency with $V_{DD}$ Disturbance (see Figure 1-8).

**FIGURE 2-77:** Input Noise Voltage vs. Time, with 1 Hz and 10 Hz Filters and $G_{MIN} = 1$.

**FIGURE 2-78:** Input Noise Voltage vs. Time, with 1 Hz and 10 Hz Filters and $G_{MIN} = 10$. 

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Note: Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = 1.8V$ to 5.5V, $V_{SS} = \text{GND}$, $V_{CM} = V_{DD}/2$, $V_{DM} = 0V$, $V_{REF} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10 \text{ k}\Omega$ to $V_L$, $C_L = 60 \text{ pF}$, $G_{DM} = G_{MIN}$ and $EN = V_{DD}$; see Figures 1-7 and 1-8.

**FIGURE 2-79:** Input Noise Voltage vs. Time, with 1 Hz and 10 Hz Filters and $G_{MIN} = 100$. 
Note: Unless otherwise indicated, \( T_A = +25^\circ \text{C} \), \( V_{\text{DD}} = 1.8 \text{V to 5.5V} \), \( V_{\text{SS}} = \text{GND} \), \( V_{\text{CM}} = V_{\text{DD}}/2 \), \( V_{\text{DM}} = 0 \text{V} \), \( V_{\text{REF}} = V_{\text{DD}}/2 \), \( V_L = V_{\text{DD}}/2 \), \( R_L = 10 \text{k}\Omega \) to \( V_L \), \( C_L = 60 \text{pF} \), \( G_{\text{DM}} = G_{\text{MIN}} \) and \( \text{EN} = V_{\text{DD}} \); see Figures 1-7 and 1-8.

### 2.5 Time Response

**FIGURE 2-80:** Input Offset Voltage vs. Time with Temperature Change.

**FIGURE 2-81:** Input Offset Voltage vs. Time at Power-Up.

**FIGURE 2-82:** The MCP6N16 Shows No Phase Reversal vs. Common Mode Input Overdrive, with \( V_{\text{DD}} = 5.5\text{V} \).

**FIGURE 2-83:** The MCP6N16 Shows No Phase Reversal vs. Differential Input Overdrive, with \( V_{\text{DD}} = 5.5\text{V} \).

**FIGURE 2-84:** The MCP6N16 Shows No Phase Reversal vs. Output Overdrive to \( V_{\text{SS}} \).

**FIGURE 2-85:** The MCP6N16 Shows No Phase Reversal vs. Output Overdrive to \( V_{\text{DD}} \).
Note: Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = 1.8V$ to $5.5V$, $V_{SS} = GND$, $V_{CM} = V_{DD}/2$, $V_{DM} = 0V$, $V_{REF} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10 \, k\Omega$ to $V_L$, $C_L = 60 \, pF$, $G_{DM} = G_{MIN}$ and $EN = V_{DD}$; see Figures 1-7 and 1-8.
Note: Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = 1.8V$ to 5.5V, $V_{SS} = GND$, $V_{CM} = V_{DD}/2$, $V_{DM} = 0V$, $V_{REF} = V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10 \, k\Omega$ to $V_L$, $C_L = 60 \, pF$, $G_{DM} = G_{MIN}$ and $EN = V_{DD}$; see Figures 1-7 and 1-8.

FIGURE 2-92: Power Supply On and Off and Output Voltage vs. Time.
**Note:** Unless otherwise indicated, \( T_A = +25^\circ C \), \( V_{DD} = 1.8V \) to 5.5V, \( V_{SS} = \text{GND} \), \( V_{CM} = V_{DD}/2 \), \( V_{DM} = 0V \), \( V_{REF} = V_{DD}/2 \), \( V_L = V_{DD}/2 \), \( R_L = 10\,k\Omega \) to \( V_L \), \( C_L = 60\,pF \), \( G_{DM} = G_{MIN} \) and \( EN = V_{DD} \); see Figures 1-7 and 1-8.

### 2.6 Enable Response

**FIGURE 2-93:** Enable and Output Voltages vs. Time, with \( V_{DD} = 1.8V \).

**FIGURE 2-94:** Enable and Output Voltages vs. Time, with \( V_{DD} = 5.5V \).

**FIGURE 2-95:** Normalized Enable Input Trip and Hysteresis Voltages vs. Ambient Temperature.

**FIGURE 2-96:** Enable Turn-On Time vs. Ambient Temperature.

**FIGURE 2-97:** Power Supply Current in Shutdown vs. Power Supply Voltage.

**FIGURE 2-98:** Output Leakage Current in Shutdown vs. Output Voltage.
3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1.

### TABLE 3-1: PIN FUNCTION TABLE

<table>
<thead>
<tr>
<th>MCP6N16</th>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSOP</td>
<td>DFN</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>EN</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>VIM</td>
</tr>
<tr>
<td>3</td>
<td>3</td>
<td>VIP</td>
</tr>
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<td>4</td>
<td>4</td>
<td>VSS</td>
</tr>
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<td>VREF</td>
</tr>
<tr>
<td>6</td>
<td>6</td>
<td>VFG</td>
</tr>
<tr>
<td>7</td>
<td>7</td>
<td>VOUT</td>
</tr>
<tr>
<td>8</td>
<td>8</td>
<td>VDD</td>
</tr>
<tr>
<td>—</td>
<td>9</td>
<td>EP</td>
</tr>
</tbody>
</table>

3.1 Digital Enable Input (EN)

This input (EN) is a CMOS, Schmitt-triggered input. When it is low, it puts the part in a low-power state. When high, the part operates normally. The EN pin must not be left floating.

3.2 Analog Signal Inputs (VIP, VIM)

The non-inverting and inverting inputs (VIP and VIM) are high-impedance CMOS inputs with low bias currents.

3.3 Power Supply Pins (VSS, VDD)

The positive power supply (VDD) is 1.8V to 5.5V higher than the negative power supply (VSS). For normal operation, the other pins are between VSS and VDD.

Typically, these parts are used in a single (positive) supply configuration. In this case, VSS is connected to ground and VDD is connected to the supply; VDD will need bypass capacitors.

3.4 Analog Reference Input (VREF)

The analog reference input (VREF) is the non-inverting input of the second input stage; it shifts VOUT to its desired range. The external gain resistor (RG) is connected to this pin. It is a high-impedance CMOS input with low bias current.

3.5 Analog Feedback Input (VFG)

The analog feedback input (VFG) is the inverting input of the second input stage. The external feedback components (RF and RG) are connected to this pin. It is a high-impedance CMOS input with low bias current.

3.6 Analog Output (VOUT)

The analog output (VOUT) is a low impedance voltage output. It represents the differential input voltage (VDM = VIP - VIM), with gain GDM and is shifted by VREF. The external feedback resistor (RF) is connected to this pin.

3.7 Exposed Thermal Pad (EP)

There is an internal connection between the exposed thermal pad (EP) and the VSS pin; they must be connected to the same potential on the printed circuit board (PCB).

This pad can be connected to a PCB ground (VSS) plane region to provide a larger heat sink. This improves the package thermal resistance (θJA).
4.0 APPLICATIONS

The MCP6N16 instrumentation amplifier (INA) is manufactured using Microchip’s state of the art CMOS process. Its low cost, low power and high speed make it ideal for battery-powered applications.

4.1 Basic Performance

4.1.1 STANDARD CIRCUIT

Figure 4-1 shows the standard circuit configuration for these INAs. When the inputs and output are in their specified ranges, the output voltage is approximately:

\[ V_{OUT} \approx V_{REF} + G_{DM} V_{DM} \]

Where:

\[ G_{DM} = 1 + \frac{R_F}{R_G} \]

The negative feedback loop includes \( G_{M2}, R_{M4}, R_F \) and \( R_G \). These blocks set the DC open-loop gain \( (A_{OL}) \) and the nominal differential gain \( (G_{DM}) \):

\[ A_{OL} = G_{M2} R_{M4} \]
\[ G_{DM} = 1 + \frac{R_F}{R_G} \]

A_{OL} is very high, so \( I_4 \) is very small and \( I_1 + I_2 \approx 0 \). This makes the differential inputs to \( G_{M1} \) and \( G_{M2} \) equal in magnitude and opposite in polarity. Ideally, this gives:

\[ (V_{FG} - V_{REF}) = V_{DM} \]
\[ V_{OUT} = V_{DM} G_{DM} + V_{REF} \]

For an ideal part, changing \( V_{CM}, V_{SS} \) or \( V_{DD} \) produces no change in \( V_{OUT} \). \( V_{REF} \) shifts \( V_{OUT} \) as needed.

The different \( G_{MIN} \) options change \( G_{M1}, G_{M2} \) and the internal compensation capacitor. This results in the performance trade-offs shown in Table 1.

4.1.3 DC ERRORS

Section 1.5 “Explanation of DC Error Specifications” defines some of the DC error specifications. These errors are internal to the INA, and can be summarized as follows:

\[ V_{OUT} = V_{REF} + G_{DM}(I + g_E)(V_{DM} + \Delta V_{ED}) + G_{DM}(I + g_E)(V_E + \Delta V_E) \]

Where:

\[ V_E = V_{OS} + \frac{\Delta V_{DD} - \Delta V_{SS}}{PSRR} + \frac{\Delta V_{CM}}{CMRR} + \frac{\Delta V_{REF}}{CMRR2} \]
\[ \Delta V_E = I_{NLDM}(V_{DMH} - V_{DML}) \]
\[ \Delta V_{ED} = I_{NLCM}(V_{IVH} - V_{IVL}) \]

Where:

\[ PSRR, CMRR, CMRR2 \] and \( A_{OL} \) are in units of V/V
\[ \Delta T_A \text{ is in units of } ^\circ C \]
\[ TC_I \text{ is in units of V/}^\circ C \]
\[ V_{DM} = 0 \]
The nonlinearity specifications (INL_CM and INL_DM) describe errors that are nonlinear functions of V_CM and V_DM, respectively. They give the maximum excursion from linear response over the entire common mode and differential ranges.

The input bias current and offset current specifications (I_B and I_OS), together with a circuit’s external input resistances, give an additional DC error. Figure 4-3 shows the resistors that set the DC bias point.

**FIGURE 4-3:** DC Bias Resistors.

The resistors at the main input (R_IP and R_IM) and its input bias currents (I_BP and I_BM) give the following changes in the INA's bias voltages:

**EQUATION 4-6:**

\[
\Delta V_{IP} = -I_{BP}R_{IP} = -(I_B + I_{OS}/2)R_{IP} \\
\Delta V_{IM} = -I_{BM}R_{IM} = -(I_B - I_{OS}/2)R_{IM} \\
\Delta V_{CM} = (\Delta V_{IP} + \Delta V_{IM})/2 \\
\quad = -I_B(R_{IP} + R_{IM})/2 - I_{OS}(R_{IP} - R_{IM})/4 \\
\Delta V_{DM} = \Delta V_{IP} - \Delta V_{IM} \\
\quad = -I_B(R_{IP} - R_{IM}) - I_{OS}(R_{IP} + R_{IM})/2 \\
\Delta V_{OUT} = G_{DM}(\Delta V_{DM} + \Delta V_{CM}/CMRR) \\
\]

Where:
- CMRR is in units of V/V

The change in V_CM (\Delta V_{CM}) can affect the input range, for large R_IP or R_IM. The best design results when R_IP and R_IM are equal and small.

**EQUATION 4-7:**

\[
\Delta V_{OUT} \approx G_{DM}\Delta V_{DM} \\
\approx G_{DM}(\pm 2I_B\varepsilon_{RTOL} - I_{OS})R_{IP} \\
\]

Where:
- R_IP = R_IM
- \varepsilon_{RTOL} = tolerance of R_IP and R_IM

The resisters at the feedback input (R_R, R_F and R_G) and its input bias currents (I_BR and I_BF) give the following changes in the INA's bias voltages:

**EQUATION 4-8:**

\[
\Delta V_{REF} = -I_{BR}R_{R} = -(I_B + I_{OS}/2)R_{R} \\
\Delta V_{FG} \approx \Delta V_{REF} \quad \text{due to high A_{OL}} \\
\Delta V_{OUT} \approx I_{BR}(R_F - G_{DM}R_{R}) + I_{OS}(R_F + G_{DM}R_{R})/2 \\
\]

Where:
- I_B meets the I_B specification
- I_{OS2} meets the I_{OS} specification
- I_B \neq I_B, in general
- I_{OS2} \neq I_{OS}, in general

The change in V_{REF} (\Delta V_{REF}) can affect the input range, for large R_R or R_F. The best design results when G_{DM}R_R and R_F are equal (i.e., R_R = R_F|R_G) and small.

**EQUATION 4-9:**

\[
\Delta V_{OUT} \approx (\pm (2I_B\varepsilon_{RTOL} + I_{OS})R_F \\
\]

Where:
- G_{DM}R_R = R_F
- \varepsilon_{RTOL} = tolerance of R_R, R_F and R_G

4.1.4 AC PERFORMANCE

The bandwidth of these amplifiers depends on G_{DM} and G_{MIN}:

**EQUATION 4-10:**

\[
f_{BW} \approx f_{GBWP}/G_{DM} \approx (0.50 \text{ MHz})(G_{MIN}/G_{DM}), \quad G_{MIN} = 1, 10 \approx (0.35 \text{ MHz})(G_{MIN}/G_{DM}), \quad G_{MIN} = 100 \\
\]

Where:
- f_{BW} = -3 dB bandwidth
- f_{GBWP} = Gain-Bandwidth product

The bandwidth at the maximum output swing is called the Full Power Bandwidth (f_{FPBW}). It is limited by the Slew Rate (SR) for many amplifiers, but is close to f_{BW} for these parts.

**EQUATION 4-11:**

\[
f_{FPBW} \approx SR/(\pi V_{O}) \approx f_{BW}, \quad \text{for these parts} \\
\]

Where:
- V_O = Maximum output voltage swing
- \approx V_{OH} - V_{OL}
4.1.5 NOISE PERFORMANCE
As shown in Figure 2-73, the noise density is white at low frequencies; the 1/f noise is negligible for almost all applications. As a result, the time domain data in Figures 2-77, 2-78 and 2-79 is well behaved.

4.2 Overview of Zero-Drift Operation
Figure 4-4 shows a simplified diagram of the MCP6N16 zero-drift INAs. This diagram will be used to explain how low voltage errors are reduced in this architecture (much better $V_{OS}$, $TC_1 (\Delta V_{OS}/\Delta T_A)$, CMRR, CMRR2, PSRR, $A_{OL}$ and 1/f noise).

4.2.1 BUILDING BLOCKS
The Main Amplifiers ($G_{M1}$ and $G_{M2}$) are designed for high gain and bandwidth, with a differential topology. The main input pairs (+ and - pins at the top left) are for the higher frequency portion of the input signal. The auxiliary input pair (+ and - pins at the bottom left of $G_{M1}$) is for the low frequency portion of the input signal and corrects the INA's input offset voltage. Both inputs are added together internally.

The Auxiliary Amplifiers ($G_{A1}$ and $G_{A2}$), the Chopper Input Switches and the Chopper Output Switches provide a high DC gain to the input signal. DC errors are modulated to higher frequencies and white noise to low frequencies.

The Low-Pass Filter reduces high-frequency content, including harmonics of the Chopping Clock.

The Output Buffer ($R_{M4}$) converts current to voltage and drives external loads at the $V_{OUT}$ pin.

The Oscillator runs at $f_{CLK} = 200$ kHz. Its output is divided by 8, to produce the Chopping Clock rate of $f_{CHOP} = 25$ kHz.

The internal POR part starts the part in a known good state, protecting against power supply brown-outs. The Digital Control block outputs clocks and POR events.

4.2.2 CHOPPING ACTION
Figure 4-5 shows the amplifier connections for the first phase of the Chopping Clock and Figure 4-6 shows them for the second phase. The slow voltage errors alternate in polarity, making the average error small.
4.2.3 INTERMODULATION DISTORTION (IMD)

These INAs will show intermodulation distortion (IMD) products when an AC signal is present. The signal and clock can be decomposed into sine wave tones (Fourier series components). These tones interact with the zero-drift circuitry’s nonlinear response to produce IMD tones at sum and difference frequencies. Each of the square wave clock’s harmonics has a series of IMD tones centered on it. See Figures 2-75 and 2-76.

4.3 Other Functional Blocks

4.3.1 RAIL-TO-RAIL INPUTS

Each input stage uses one PMOS differential pair at the input. The output of each differential pair is processed using current mode circuitry. The inputs show no crossover distortion vs. common mode voltage.

With this topology, the inputs (\(V_{IP}\) and \(V_{IM}\)) operate normally down to \(V_{SS} – 0.15V\) and up to \(V_{DD} + 0.15V\) at room temperature (see Figure 2-52). The input offset voltage (\(V_{DS}\)) is measured at \(V_{CM} = V_{SS} – 0.15V\) and \(V_{DD} + 0.15V\) (at +25°C) to ensure proper operation.

4.3.1.1 Phase Reversal

The input devices are designed to not exhibit phase inversion when the input pins exceed the supply voltages. Figure 2-82 shows an input voltage exceeding both supplies with no phase inversion.

The input devices also do not exhibit phase inversion when the differential input voltage exceeds its limits; see Figure 2-83.

4.3.1.2 Input Voltage Limits

In order to prevent damage and/or improper operation of these amplifiers, the circuit must limit the voltages at the input pins (see Section 1.1 “Absolute Maximum Ratings†”). This requirement is independent of the current limits discussed later on.

The ESD protection on the inputs can be depicted as shown in Figure 4-7. This structure was chosen to protect the input transistors against many (but not all) overvoltage conditions, and to minimize input bias current (\(I_{B}\)).

The input ESD diodes clamp the inputs when they try to go more than one diode drop below \(V_{SS}\). They also clamp any voltages that go too far above \(V_{DD}\); their breakdown voltage is high enough to allow normal operation, but not low enough to protect against slow over-voltage (beyond \(V_{DD}\)) events. Very fast ESD events (that meet the specification) are limited so that damage does not occur.
In some applications, it may be necessary to prevent excessive voltages from reaching the INA inputs. Figure 4-8 shows one approach to protecting these inputs. D1 and D2 may be small signal silicon diodes, Schottky diodes for lower clamping voltages or diode-connected FETs for low leakage.

**FIGURE 4-8:** Protecting the Analog Inputs Against High Voltages.

### 4.3.1.3 Input Current Limits

In order to prevent damage and/or improper operation of these amplifiers, the circuit must limit the currents into the input pins (see Section 1.1 “Absolute Maximum Ratings†”). This requirement is independent of the voltage limits previously discussed.

Figure 4-9 shows one approach to protecting these inputs. The resistors R1 and R2 limit the possible current in or out of the input pins (and into D1 and D2). The diode currents will dump onto VDD.

**FIGURE 4-9:** Protecting the Analog Inputs Against High Currents.

\[
\text{min}(R_1, R_2) > \frac{V_{SS} - \min(V_1, V_2)}{2 \, mA}
\]

\[
\text{min}(R_1, R_2) > \frac{\max(V_1, V_2) - V_{DD}}{2 \, mA}
\]

### 4.3.1.4 Input Voltage Ranges

Figure 4-10 shows possible input voltage values (VSS = 0V). Lines with a slope of +1 have constant VDM (e.g., the VDM = 0 line). Lines with a slope of -1 have constant VCM (e.g., the VCM = VDD/2 line).

For normal operation, VIP and VIM must be kept within the region surrounded by the thick blue lines. The horizontal and vertical blue lines show the limits on the individual inputs. The blue lines with a slope of +1 show the limits on VDM, the larger GMIN is, the closer they are to the VDM = 0 line.

The input voltage range specifications (VIVL and VIVH) change with the supply voltages (VSS and VDD, respectively). The differential input range specifications (VDML and VDMH) change with minimum gain (GMIN). Temperature also affects these specifications.

**FIGURE 4-10:** Input Voltage Ranges.

To take full advantage of VDML and VDMH, set VREF (see Figures 1-7 and 1-8) so that the output (VOUT) is centered between the supplies (VSS and VDD). Also set the gain (GDM) to keep VOUT within its range.
4.3.2 ENABLE
This input (EN) is a CMOS, Schmitt-triggered input. When it is low, it puts the part in a low-power state and the output is put into a high-impedance state. When high, the part operates normally.
If the EN pin is left floating, the amplifier will not operate properly.

4.3.3 RAIL-TO-RAIL OUTPUT
The Minimum Output Voltage (V_{OL}) and Maximum Output Voltage (V_{OH}) specifications describe the widest output swing that can be achieved under the specified load conditions.
The output can also be limited when V_{IP} or V_{IM} exceeds V_{IVL} or V_{IVH} or when V_{DM} exceeds V_{DML} or V_{DMH}.

4.4 Applications Tips
4.4.1 INPUT OFFSET VOLTAGE OVER TEMPERATURE
Table 1 gives both the linear and quadratic temperature coefficients (TC_{1} and TC_{2}) of input offset voltage. The input offset voltage can be estimated as follows:

\[
V_{OS}(T_A) = V_{OS} + TC_{1}\Delta T + TC_{2}\Delta T^2
\]

Where:
- \( T_A = -40°C \) to +125°C
- \( \Delta T = T_A - 25°C \)
- \( V_{OS}(T_A) = \) Input offset voltage at \( T_A \)
- \( V_{OS} = \) Input offset voltage at +25°C
- \( TC_{1} = \) Linear temperature coefficient
- \( TC_{2} = \) Quadratic temperature coefficient

These specifications show these INA's intrinsic performance. The plots of input offset voltage versus temperature on the second page (Figures 1 to 3) show the typical behavior for a few parts from the first wafer lot.

In most designs, other effects will dominate the circuit temperature performance; see Section 4.4.13 “PCB Design for DC Precision” for more details.

4.4.2 NOISE EFFECT ON OFFSET VOLTAGE
The input noise (e_{in}) makes measured offset values (V_{OS}) vary in a random manner. Lower noise requires a lower noise power bandwidth (NPBW; see AN1228, mentioned in 5.3 “Application Notes”), which increases measurement time. In the offset-related specifications (A_{OL}, CMRR, CMRR2 and PSRR) and plots, the various values of NPBW were chosen to trade off time versus accuracy of results.

4.4.3 DC GAIN PLOTS
Figures 2-28 to 2-39 are histograms of the reciprocals (in units of \( \mu \)V/V) of CMRR, PSRR and A_{OL}, respectively. They represent the change in input offset voltage (V_{OS}) with a change in common mode input voltage (V_{CM}), power supply voltage (V_{DD}) and output voltage (V_{OUT}).
The 1/A_{OL} histogram is centered near 0 \( \mu \)V/V because the measurements are dominated by the INA's input noise. The negative values shown represent noise and tester limitations, not unstable behavior. Production tests make multiple V_{OS} measurements, which validates an INA's stability; an unstable part would show greater V_{OS} variability, or the output would stick at one of the supply rails.

4.4.4 OFFSET AT POWER-UP
When these parts power up, the input offset (V_{OS}) starts at its uncorrected value (usually less than ±10 mV). Circuits with high DC gain can cause the output to reach one of the two rails. In this case, the time to a valid output is delayed by an output overdrive time (like t_{ODR}), in addition to a start-up time (like t_{STR}).
It can be simple to avoid this extra start-up time. Reducing the gain is one method. Adding a capacitor across the feedback resistor (R_F) is another method.

4.4.5 SOURCE RESISTANCES
The input bias currents have two significant components: switching glitches that dominate at room temperature and below, and input ESD diode leakage currents that dominate at +85°C and above.
Make the resistances seen by the inputs small and equal. This minimizes the output offset caused by the input bias currents.
The inputs should see a resistance on the order of 10Ω to 1 kΩ at high frequencies (i.e., above 1 MHz). This helps minimize the impact of switching glitches, which are very fast, on overall performance. In some cases, it may be necessary to add resistors in series with the inputs to achieve this improvement in performance.
Small input resistances at the inputs may be needed for high gains. Without them, parasitic capacitances might cause positive feedback and instability.

4.4.6 SOURCE CAPACITANCE
The capacitances seen by the inputs should be small. Large input capacitances and source resistances, together with high gain, can lead to positive feedback and instability.
4.4.7 MINIMUM STABLE GAIN

There are three options for different Minimum Stable Gains (1, 10 and 100 V/V; see Table 1). The differential gain (G_{DM}) needs to be greater than or equal to G_{MIN} in order to maintain stability.

Picking a part with higher G_{MIN} has the advantages of lower input noise voltage density (e_{ni}), lower input offset voltage (V_{OS}) and increased gain-bandwidth product (GBWP). The differential input voltage range (V_{DML} and V_{DMH}) is lower for higher G_{MIN}, but supports a reasonable output voltage range.

4.4.8 CAPACITIVE LOADS

Driving large capacitive loads can cause stability problems for voltage amplifiers. As the load capacitance increases, the feedback loop’s phase margin decreases and the closed-loop bandwidth reduces. This produces gain peaking in the frequency response, with overshoot and ringing in the step response. Lower gains (G_{DM}) exhibit greater sensitivity to capacitive loads.

When driving large capacitive loads with these instrumentation amps (e.g., > 80 pF), a small series resistor at the output (R_{ISO} in Figure 4-11) improves the feedback loop’s phase margin (stability) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitive load.

![Figure 4-11: Output Resistor, R_{ISO} Stabilizes Large Capacitive Loads.](image)

**FIGURE 4-11:** Output Resistor, R_{ISO} Stabilizes Large Capacitive Loads.

Figure 4-12 gives recommended R_{ISO} values for different capacitive loads and gains. The x-axis is the normalized load capacitance (C_{L} G_{MIN}/G_{DM}), where G_{DM} is the circuit’s differential gain (1 + R_{F}/R_{G}) and G_{MIN} is the minimum stable gain.

![Figure 4-12: Recommended R_{ISO} Values for Capacitive Loads.](image)

**FIGURE 4-12:** Recommended R_{ISO} Values for Capacitive Loads.

After selecting R_{ISO} for the circuit, double check the resulting frequency response peaking and step response overshoot on the bench. Modify R_{ISO}’s value until the response is reasonable.

4.4.9 GAIN RESISTORS

Figure 4-13 shows a simple gain circuit with the INA’s input capacitances at the feedback inputs (V_{REF} and V_{FG}). These capacitances interact with R_{G} and R_{F} to modify the gain at high frequencies. The equivalent capacitance acting in parallel to R_{G} is C_{G} = C_{DM} + C_{CM} plus any board capacitance in parallel to R_{G}. C_{G} will cause an increase in G_{DM} at high frequencies, which reduces the phase margin of the feedback loop (i.e., reduce the feedback loop’s stability).

![Figure 4-13: Simple Gain Circuit with Parasitic Capacitances.](image)

**FIGURE 4-13:** Simple Gain Circuit with Parasitic Capacitances.
In this data sheet, $R_F + R_G = 10\,\Omega$ for most gains (0\,\Omega for $G_{DM} = 1$); see Table 1-6. This choice gives good phase margin. In general, $R_F$ (Figure 4-13) needs to meet the following limits to maintain stability:

**EQUATION 4-13:**

For $G_{DM} = 1$:

$$R_F = 0$$

For $G_{DM} > 1$:

$$R_F < \frac{\alpha G_{DM}^2}{2\pi f_{GBWP} C_G}$$

Where:

$$\alpha \leq 0.25$$

$$G_{DM} \geq G_{MIN}$$

$$f_{GBWP} = \text{Gain-Bandwidth Product}$$

$$C_G = C_{DM} + C_{CM} + \text{(PCB stray capacitance)}$$

### 4.4.10 EMI REJECTION RATIO (EMIRR)

Electromagnetic interference (EMI) can be coupled to an INA through electromagnetic induction or radiation, or by conduction. INAs are most sensitive to EMI at their input pins.

EMIRR describes an INA’s EMI robustness. Internal passive filters in these parts improve the EMIRR, when good PCB layout techniques are used. EMIRR is defined to be:

**EQUATION 4-14:**

$$\text{EMIRR (dB)} = 20 \cdot \log\left(\frac{V_{RF}}{\Delta V_{OS}}\right)$$

Where:

$$V_{RF} = \text{Peak Input Voltage of EMI (V}_{PK}\right)$$

$$\Delta V_{OS} = \text{Input Offset Voltage Shift (V)}$$

### 4.4.11 REDUCING UNDESIRED NOISE AND SIGNALS

Reduce undesired noise and signals with:

- Low bandwidth signal filters:
  - Minimizes random analog noise
  - Reduces interfering signals
- Good PCB layout techniques:
  - Minimizes crosstalk
  - Minimizes parasitic capacitances and inductances that interact with fast switching edges
- Good power supply design:
  - Isolation from other parts
  - Filtering of interference on supply line(s)

### 4.4.12 SUPPLY BYPASS

With these INAs, the Power Supply pin ($V_{DD}$ for single supply) should have a local bypass capacitor (i.e., 0.01 μF to 0.1 μF) within 2 mm for good high-frequency performance. Surface mount, multilayer ceramic capacitors, or their equivalent, should be used.

These INAs require a bulk capacitor (i.e., 1.0 μF or larger) within 100 mm to provide large, slow currents. This bulk capacitor can be shared with other nearby analog parts as long as crosstalk through the supplies does not prove to be a problem.

### 4.4.13 PCB DESIGN FOR DC PRECISION

In order to achieve DC precision on the order of ±1 μV, many physical errors need to be minimized. The design of the printed circuit board (PCB), the wiring, and the thermal environment have a strong impact on the precision achieved. A poor PCB design can easily be more than 100 times worse than the MCP6N16 op amps’ minimum and maximum specifications.

#### 4.4.13.1 PCB Layout

Any time two dissimilar metals are joined together, a temperature dependent voltage appears across the junction (the Seebeck or thermojunction effect). This effect is used in thermocouples to measure temperature. The following are examples of thermojunctions on a PCB:

- Components (resistors, INAs, …) soldered to a copper pad
- Wires mechanically attached to the PCB
- Jumpers
- Solder joints
- PCB vias

Typical thermojunctions have temperature to voltage conversion coefficients of 1 to 100 μV/°C (sometimes higher).

Microchip’s AN1258 (“Op Amp Precision Design: PCB Layout Techniques” – DS01258) contains in-depth information on PCB layout techniques that minimize thermojunction effects. It also discusses other effects, such as crosstalk, impedances, mechanical stresses and humidity.

#### 4.4.13.2 Crosstalk

DC crosstalk causes offsets that appear as a larger input offset voltage. Common causes include:

- Common mode noise (remote sensors)
- Ground loops (current return paths)
- Power supply coupling

Interference from the mains (usually 50 Hz or 60 Hz), and other AC sources, can also affect the DC performance. Nonlinear distortion can convert these signals to multiple tones, including a DC shift in voltage.
When the signal is sampled by an ADC, these AC signals can also be aliased to DC, causing an apparent shift in offset.

To reduce interference:
- Keep traces and wires as short as possible
- Use shielding
- Use ground plane (at least a star ground)
- Place the input signal source near to the DUT
- Use good PCB layout techniques
- Use a separate power supply filter (bypass capacitors) for these zero-drift INAs

### 4.4.13.3 Miscellaneous Effects

Keep the resistances seen by the input pins as small and as near to equal as possible, to minimize bias current-related offsets.

Make the (trace) capacitances seen by the input pins small and equal. This is helpful in minimizing switching glitch-induced offset voltages.

Bending a coax cable with a radius that is too small causes a small voltage drop to appear on the center conductor (the triboelectric effect). Make sure the bending radius is large enough to keep the conductors and insulation in full contact.

Mechanical stresses can make some capacitor types (such as some ceramics) output small voltages. Use more appropriate capacitor types in the signal path and minimize mechanical stresses and vibration.

Humidity can cause electrochemical potential voltages to appear in a circuit. Proper PCB cleaning helps, as does the use of encapsulants.

## 4.5 Typical Applications

### 4.5.1 HIGH INPUT IMPEDANCE DIFFERENCE AMPLIFIER

Figure 4-14 shows the MCP6N16 used as a difference amplifier. The inputs are high-impedance and give good CMRR performance.

![Figure 4-14: Difference Amplifier.](image)

### 4.5.2 DIFFERENCE AMPLIFIER FOR VERY LARGE COMMON MODE SIGNALS

Figure 4-15 uses the MCP6N16 INA as a difference amplifier for signals with a very large common mode component. The input resistor dividers (R1 and R2) ensure that the INA’s inputs are within their normal range of operation. The capacitors (C1 and C2) set the same voltage division ratio for high-frequency signals (e.g., a voltage step). C2 includes the INA’s CCM. R1 and R2’s tolerances affect CMRR.

![Figure 4-15: Difference Amplifier with Very Large Common Mode Component.](image)

### 4.5.3 RTD TEMPERATURE SENSOR

Figure 4-16 shows an RTD temperature sensor circuit, which measures over the -55°C to +155°C range. The sensor chosen changes from 78Ω to 159Ω over this range. The 2.49 kΩ and 4.99 kΩ resistors set the current through the RTD and 68.1Ω resistor. The INA provides a high-differential gain. The 10 µF capacitor filters common mode interference on the bridge.

![Figure 4-16: RTD Temperature Sensor.](image)
4.5.4 WHEATSTONE BRIDGE

Figure 4-17 shows the MCP6N16 INA used to condition the signal from a Wheatstone bridge (e.g., strain gage). The overall INA gain is set at 1001 V/V. The best $G_{\text{MIN}}$ option to pick, for this gain, is 100 V/V (MCP6N16-100).

4.5.5 HIGH SIDE CURRENT DETECTOR

Figure 4-18 shows the MCP6N16 INA used to detect and amplify the high side current in a power supply design. $U_1$’s low offset voltage makes it possible to reduce $R_{SH}$, which saves power and minimizes temperature effects. $U_1$’s supply current is included in the measurement. The INA’s gain is set at 101 V/V, so $V_{OUT}$ changes 1.01V for every 1A change in $I_{DD}$.

$$V_{PS} = +1.8\text{V to 5.5V}$$

$$I_{PS} = I_L + I_{DD}$$

$$I_{PS} = (V_{PS} - V_L)/(10 \text{ m}\Omega)$$

$$= (V_{OUT} - V_{REF})/((10 \text{ m}\Omega) (101 \text{ V/V}))$$
5.0 DESIGN AIDS

Microchip provides the basic design aids needed for the MCP6N16 instrumentation amplifiers.

5.1 Microchip Advanced Part Selector (MAPS)

MAPS is a software tool that helps efficiently identify Microchip devices that fit a particular design requirement. Available at no cost from the Microchip website at www.microchip.com/maps, the MAPS is an overall selection tool for Microchip’s product portfolio that includes Analog, Memory, MCUs and DSCs. Using this tool, a customer can define a filter to sort features for a parametric search of devices and export side-by-side technical comparison reports. Helpful links are also provided for Data sheets, Purchase and Sampling of Microchip parts.

5.2 Analog Demonstration Board

Microchip offers a broad spectrum of Analog Demonstration and Evaluation Boards that are designed to help customers achieve faster time to market. For a complete listing of these boards and their corresponding user’s guides and technical information, visit the Microchip web site at www.microchip.com/analog tools.

5.3 Application Notes

The following Microchip Application Notes are available on the Microchip web site at www.microchip.com/appnotes and are recommended as supplemental reference resources.

- **AN884**: “Driving Capacitive Loads With Op Amps”, DS00884
- **AN990**: “Analog Sensor Conditioning Circuits – An Overview”, DS00990
- **AN1177**: “Op Amp Precision Design: DC Errors”, DS01177
- **AN1228**: “Op Amp Precision Design: Random Noise”, DS01228
- **AN1258**: “Op Amp Precision Design: PCB Layout Techniques”, DS01258

Some of these application notes, and others, are listed in the design guide:

- “Signal Chain Design Guide”, DS21825
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

Legend:
- XXX...X Customer-specific information
- Y Year code (last digit of calendar year)
- YY Year code (last 2 digits of calendar year)
- WW Week code (week of January 1 is week ‘01’)
- NNN Alphanumeric traceability code
- @3 Pb-free JEDEC® designator for Matte Tin (Sn)
- * This package is Pb-free. The Pb-free JEDEC designator (®) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

Microchip Technology Drawing No. C04-062C Sheet 1 of 2
8-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

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Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-062C Sheet 2 of 2
8-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

RECOMMENDED LAND PATTERN

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Notes:
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2062B
8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging
8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

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<td>Molded Package Width</td>
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<td>Overall Length</td>
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<tr>
<td>Foot Length</td>
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<tr>
<td>Lead Thickness</td>
<td>c</td>
</tr>
<tr>
<td>Lead Width</td>
<td>b</td>
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**Notes:**
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.16mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.
   - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   - REF: Reference Dimension, usually without tolerance, for information purposes only.
8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

RECOMMENDED LAND PATTERN

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Notes:
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. CD4-2111A
APPENDIX A: REVISION HISTORY

Revision A (July 2014)

• Original Release of this Document.
**MCP6N16**

**PRODUCT IDENTIFICATION SYSTEM**

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

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<th>-XXX</th>
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<td>Gain Option</td>
<td>Temperature Range</td>
<td>Package</td>
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<td>Single Instrumentation Amplifier</td>
<td>001 = Minimum gain of 1 V/V</td>
<td>E = -40°C to +125°C</td>
<td>MF = Plastic Dual Flat, no lead Package - 3×3x0.9 mm Body, 8-lead (DFN)</td>
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<td>MCP6N16T</td>
<td>Single Instrumentation Amplifier (Tape and Reel)</td>
<td>010 = Minimum gain of 10 V/V</td>
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<td>MS = Plastic Micro Small Outline Package, 8-lead (MSOP)</td>
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<td></td>
<td></td>
<td>100 = Minimum gain of 100 V/V</td>
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</tr>
</tbody>
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**Examples:**

a) MCP6N16T-001E/MF: Tape and Reel, Minimum gain = 1, Extended temperature, 8LD 3×3 DFN

b) MCP6N16-010E/MS: Minimum gain = 10, Extended temperature, 8LD MSOP

**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.
Note the following details of the code protection feature on Microchip devices:

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