SPI Extender Over Rugged Differential Link

FEATURES

- **2MHz SCK Over 10m, Operation Up to 1200m**
- **Three Extended Slave Selects**
- **Protected from Overvoltage Lines Fault to ±60V**
- **±40kV HBM ESD on Link Pins**
- **IEC ESD ±6kV and EFT ±4kV on Link Pins**
- **Extended Common Mode Range: ±25V**
- Extended Interrupt
- Separate Programmable SPI Modes
- Link Galvanic Isolation Supported
- 3V to 5.5V Supply Voltage
- 1.62V to 5.5V Logic Supply
- 4mm × 5mm 20-Lead QFN package

APPLICATIONS

- Industrial Control and Sensors
- Lighting and Sound System Control

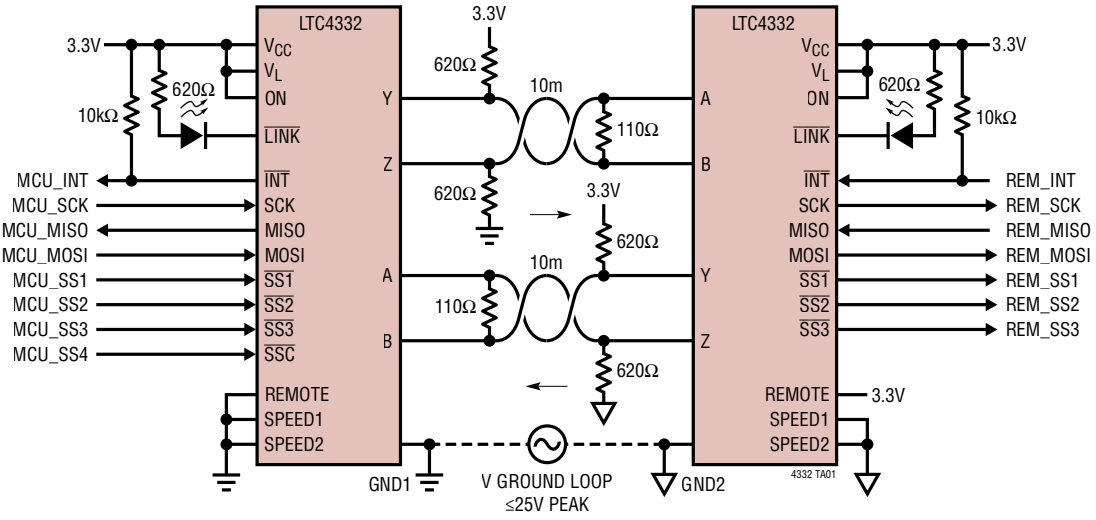
DESCRIPTION

The LTC®4332 is a point-to-point rugged SPI extender designed for operation in high noise industrial environments over long distances. Using a ±60V fault protected differential transceiver, the LTC4332 can transmit SPI data, including an interrupt signal, up to 2MHz over two twisted pair cables. The extended common mode range and high common mode rejection on the differential link provides tolerance to large ground differences between nodes. The LTC4332 also supports external galvanic isolation on the link.

The LTC4332 provides a control interface using a separate slave select for configuration and fault monitoring.

TYPICAL APPLICATION

Extended SPI Network Over 10m CAT5, 2MHz SCK



ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltages
- V_{CC} ..... –0.3V to 6V
- V_L ..... –0.3V to 6V

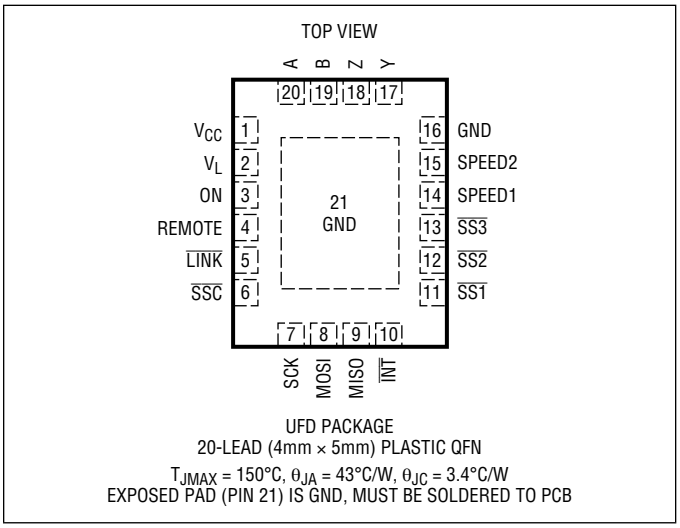
Logic Signals
- ON, $\overline{LINK}$, $\overline{INT}$, $\overline{SSC}$ ..... –0.3V to 6V
- REMOTE, SCK, MISO, MOSI, $\overline{SS1}$, $\overline{SS2}$, $\overline{SS3}$, SPEED1, SPEED2 ..... GND – 0.3V to V_L + 0.3V

Interface I/O: A, B, Y, Z ..... –60V to 60V

Operating Temperature Range (Note 11)
- LTC4332C ..... 0°C to 70°C
- LTC4332I ..... –40°C to 85°C
- LTC4332H ..... –40°C to 125°C

Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UFD PACKAGE
20-LEAD (4mm × 5mm) PLASTIC QFN
T_{JMAX} = 150°C, θ_{JA} = 43°C/W, θ_{JC} = 3.4°C/W
EXPOSED PAD (PIN 21) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4332CUFD#PBF	LTC4332CUFD#TRPBF	4332	20-Lead (4mm × 5mm) Plastic QFN	0°C to 70°C
LTC4332IUFD#PBF	LTC4332IUFD#TRPBF	4332	20-Lead (4mm × 5mm) Plastic QFN	–40°C to 85°C
LTC4332HUFD#PBF	LTC4332HUFD#TRPBF	4332	20-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, V_L = 3.3V, GND = 0V unless otherwise noted. (Note 6)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supplies							
V_{CC}	Operating Supply Range		●	3		5.5	V
I_{CC}	Operating Supply Current	Low Power: ON = 0 Idle: ON = 1, Idle SPI Active: SCK = 2MHz, SPEED INDEX = 8 (Note 7)	● ● ●		1	40 12 120	µA mA mA
V_L	Logic Interface Supply Range		●	1.62		5.5	V
I_L	Logic Supply Current		●			±140	µA
Differential Driver (Pins Y, Z)							
$\|V_{OD}\|$	Differential Driver Output Voltage	R = ∞ R = 27Ω (Figure 1)	● ●	1.5 1.5		V_{CC} 5	V V
I_{OSD}	Maximum Driver Short-Circuit Current	–60V ≤ (Y or Z) ≤ 60V (Figure 2)	●		±150	±250	mA
Differential Receiver (Pins A, B)							
R_{IN}	Receiver Input Resistance	0V ≤ V_{CC} ≤ 5.5V (Figure 3)			112		kΩ
V_{CM}	Receiver Common Mode Input Voltage		●			±25	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, V_L = 3.3V, GND = 0V unless otherwise noted. (Note 6)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{TH}	Differential Input Signal Threshold	–25V < V_{CM} < 25V (Note 2)	●			±200	mV
Logic							
V_{IH}	High Level Input Voltage (ON, SCK, MISO, MOSI, $\overline{SS1}$, $\overline{SS2}$, $\overline{SS3}$, $\overline{SSC}$, $\overline{INT}$, REMOTE)	1.62V ≤ V_L ≤ 5.5V	●	0.8 • V_L			V
V_{IH3ST}	High Level Input Voltage (SPEED1, SPEED2)		●	V_L – 0.25			V
V_{IM3ST}	Mid Level Input Voltage (SPEED1, SPEED2)		●	0.45 • V_L		0.55 • V_L	V
V_{IL3ST}	Low Level Input Voltage (SPEED1, SPEED2)		●			0.25	V
V_{IL}	Low Level Input Voltage (ON, SCK, MISO, MOSI, $\overline{SS1}$, $\overline{SS2}$, $\overline{SS3}$, $\overline{SSC}$, $\overline{INT}$, REMOTE)	1.62V ≤ V_L ≤ 5.5V	●			0.2 • V_L	V
	Digital Input Current (ON, REMOTE, SPEED1, SPEED2)	V_{IN} = 0V to V_L	●			±60	µA
	Digital Input Current (SCK, MOSI, $\overline{SS1}$, $\overline{SS2}$, $\overline{SS3}$, $\overline{SSC}$)	V_{IN} = 0V to V_L, REMOTE = 0	●			±60	µA
	Digital Input Current (MISO)	V_{IN} = 0V to V_L, REMOTE = 1	●			±60	µA
	Digital Input Current ($\overline{INT}$)	V_{IN} = 0V to V_L, REMOTE = 1	●			±5	µA
C_{IN}	Digital Input Capacitance	(Note 2)			10		pF
V_{OH}	High Level Output Voltage	I_O = –500µA, 1.62V ≤ V_L ≤ 5.5V	●	V_L – 0.2			V
V_{OL}	Low Level Output Voltage	I_O = 500µA, 1.62V ≤ V_L ≤ 5.5V	●			0.2	V
I_{OZ}	High-Z Output Leakage Current ($\overline{LINK}$, $\overline{INT}$)		●			±5	µA
	High-Z Output Leakage Current (MOSI)	REMOTE = 1	●			±60	µA
	High-Z Output Leakage Current (MISO)	REMOTE = 0	●			±60	µA
	Output Source Current (Short-Circuit)				±80		mA

SWITCHING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, V_L = 3.3V, GND = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
General							
t_{ON_LOW}	Pulse Width of ON low for Valid Reset Condition	(Figure 6)	●	1			µs
t_{READY}	ON Rise to Control Interface ($\overline{SSC}$) Ready		●	15			µs
t_{SSF_PROP}	Local Slave Select Fall to Remote Slave Select Fall Propagation Delay	(Note 3)(Figure 9)		0.4 • SF	1 • SF	13 • SF	µs
t_{SCKR_PROP}	Local SCK Rise to Remote SCK Fall and MOSI Update Propagation Delay	(CPOL, CPHA) = (1,1)			0.7 • SF		µs
	Local SCK Rise to Remote SCK Rise and MOSI Update Propagation Delay	(CPOL, CPHA) = (0,1)			0.7 • SF		µs
	Local SCK Rise to MOSI Update Propagation Delay	(CPOL, CPHA) = (0,0) or (1,0)			0.7 • SF		µs
t_{SSR_PROP}	Local Slave Select Rise to Remote SCK Fall Propagation Delay	(CPOL, CPHA) = (0,0)			0.7 • SF		µs
	Local Slave Select Rise to Remote SCK Rise Propagation Delay	(CPOL, CPHA) = (1,0)			0.7 • SF		µs
t_{INT_PROP}	Remote $\overline{INT}$ to Local $\overline{INT}$ Propagation Delay	(Note 3)		0.4 • SF	1 • SF	13 • SF	µs
t_{REMOTE_RESET}	Delay from Local ON Low for Valid Remote Reset Condition		●	180			ms
t_R, t_F	Logic Output Rise/Fall (SCK, MISO, MOSI)	C_L = 20pF	●			8	ns

SWITCHING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, V_L = 3.3V, GND = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Local Mode (REMOTE = 0)							
$f_{SCK:SLAVE}$	SCK Input Frequency	(SPEED INDEX = 8) (Table 2)	●	10		2000	kHz kHz
$t_{SCKH:SLAVE}$	SCK Input High Time	(Figure 7)	●	100			ns
$t_{SCKL:SLAVE}$	SCK Input Low Time		●	100			ns
$t_{BUF:SLAVE}$	$\overline{SSx}$ Rise to $\overline{SSx}$ Fall Delay	(Note 3)	●	2 • SF			µs
$t_{SSFSCK:SLAVE}$	$\overline{SSx}$ Fall to SCK Rise Delay	(Note 3)	●	2 • SF		168000	µs
$t_{SCKRSS:SLAVE}$	SCK Rise to $\overline{SSx}$ Rise Delay	(Note 3)	●	1 • SF		168000	µs
$t_{DMISO:SLAVE}$	MISO Data Valid from SCK Fall Delay	C_L = 20pF	●			100	ns
$t_{HMISO:SLAVE}$	MISO Data Remains Valid from SCK Fall Delay	C_L = 20pF	●	40			ns
$t_{SMOSI:SLAVE}$	MOSI Data Setup to SCK Rise		●	40			ns
$t_{HMOSI:SLAVE}$	MOSI Data Hold after SCK Rise		●	40			ns
Remote Mode (REMOTE = 1)							
$t_{SCKL:MASTER}$	SCK Low from LTC4332	(CPOL, CPHA) = (0,0) or (1,1) (Figure 9) (Note 4)	●	0.2 • SF		0.3 • SF	µs
$t_{SCKH:MASTER}$	SCK High from LTC4332	(CPOL, CPHA) = (0,1) or (1,0) (Note 4)	●	0.15 • SF		0.3 • SF	µs
$t_{SCKTSS:MASTER}$	SCK Trailing Edge to $\overline{SSx}$ High	(Note 4)	●	0.2 • SF			µs
$t_{SCKJ:MASTER}$	SCK Cycle to Cycle Jitter	(Figure 8)	●			±30	ns
$t_{DMOSI:MASTER}$	MOSI Data Valid from SCK Fall Delay	C_L = 20pF	●			15	ns
$t_{HMOSI:MASTER}$	MOSI Data Remains Valid from SCK Fall Delay	C_L = 20pF	●	–5			ns
$t_{SMISO:MASTER}$	MISO Data Setup to SCK Rise		●	40			ns
$t_{HMISO:MASTER}$	MISO Data Hold after SCK Rise		●	40			ns
$t_{TIMEOUT:MASTER}$	Active Slave Select Timeout		●	148		175	ms
Link Interface							
t_{RD}, t_{FD}	Differential Driver Rise or Fall Time	R_{DIFF} = 54Ω, C_L = 100pF	●		4	15	ns
$t_{LINK\_TIMEOUT}$	Response Time for $\overline{LINK}$ Release after Disconnection	REMOTE = 1 REMOTE = 0			168 100		ms µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Guaranteed by design, not production tested.

Note 3: SF = Speed Factor. See Table 2.

Note 4: CPOL and CPHA set using fields REM_SSx_POL and REM_SSx_PHA in the CONFIG register.

Note 5: All currents into device pins are positive; all currents out of device are negative. All voltages are referenced to their corresponding ground unless otherwise specified.

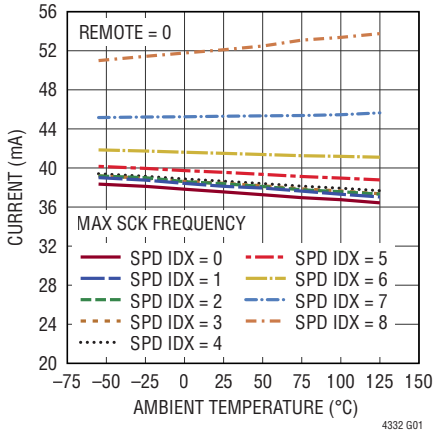
Note 6: Continuous operation above specified maximum operating junction temperature may result in device degradation or failure.

Note 7: Link network with R_B = 250Ω, R_{DIFF} = 100Ω, and C_L = 150pF from Figure 4 unless otherwise noted.

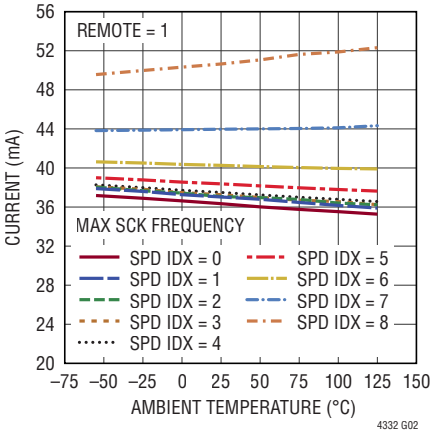
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C. V_{CC} = 5V, V_L = 3.3V, GND = 0V unless otherwise noted.

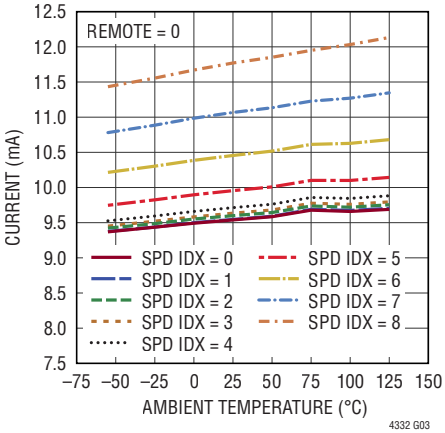
I_{CC} vs Temperature SPI Bus Active



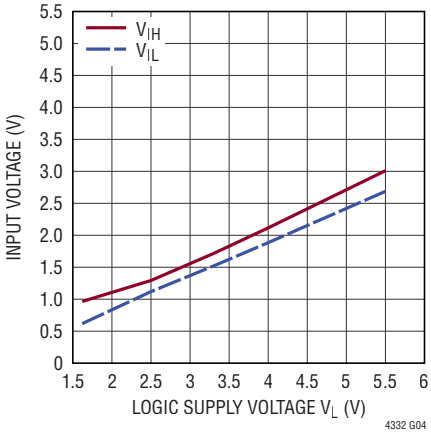
I_{CC} vs Temperature SPI Bus Active



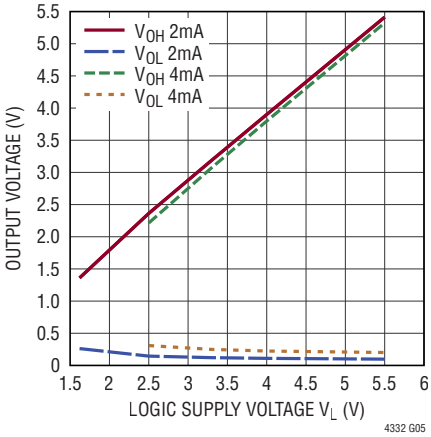
I_{CC} vs Temperature SPI Bus Idle



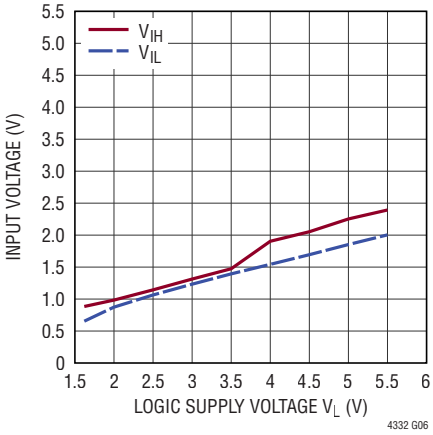
Logic Inputs V_{IL} and V_{IH} vs V_L Supply (Except SCK, MISO, and $\overline{INT}$)



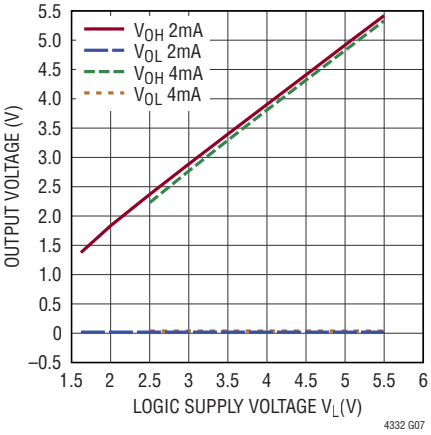
Logic Outputs V_{OL} and V_{OH} vs V_L Supply (Except SCK and MISO)



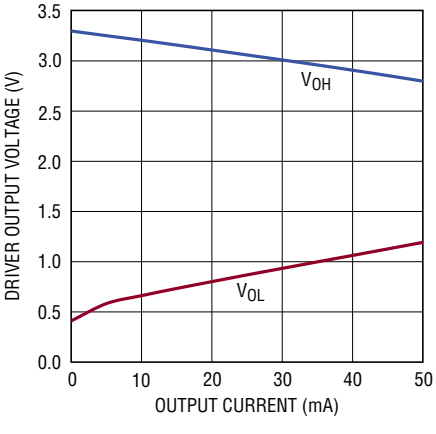
SCK, MISO, and $\overline{INT}$ Inputs V_{IL} and V_{IH} vs V_L Supply



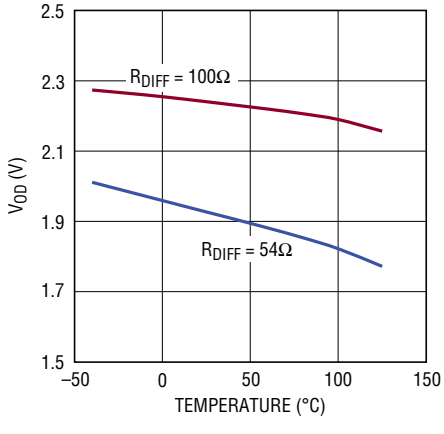
SCK and MISO Output (2mA and 4mA) V_{OL} and V_{OH} vs V_L Supply



Y/Z Driver Output Low/High Voltage vs Output Current (V_{CC} = 3.3V)



Y/Z Driver Differential Output Voltage vs Temperature (V_{CC} = 3.3V)



PIN FUNCTIONS

Logic (All Inputs and Outputs Referenced to GND and V_L)

V_{CC} (Pin 1): Main Supply Voltage. 3.0V ≤ V_{CC} ≤ 5.5V. Bypass with 4.7µF ceramic capacitor to GND.

V_L (Pin 2): Logic Interface Supply Voltage. 1.62V ≤ V_L ≤ 5.5V. Bypass with 1µF ceramic capacitor to GND.

ON (Pin 3): Enable Input. Set high for operation. Set low for low power mode, in which the internal reset is held, and outputs are disabled. Connect to V_L if unused.

REMOTE (Pin 4): Operating Mode Select Input. Set low for local SPI slave mode. Set high for SPI master mode when used on the remote side. REMOTE is weakly pulled to GND.

$\overline{\text{LINK}}$ (Pin 5): Link Status Open-Drain Output. $\overline{\text{LINK}}$ is driven low when the device establishes link communication. Connect to an external pull-up to V_L to monitor status, otherwise float or connect to GND.

$\overline{\text{SSC}}$ (Pin 6): Control Interface Select Input (Active Low). $\overline{\text{SSC}}$ enables access to the LTC4332 internal control registers. Set $\overline{\text{SSC}}$ low to initiate a SPI transfer using pins SCK, MOSI, and MISO. $\overline{\text{SSC}}$ must be set high when the SPI bus is idle. $\overline{\text{SSC}}$ is only used in local mode (REMOTE = 0). $\overline{\text{SSC}}$ is weakly pulled to V_L and can be unconnected if not used.

SCK (Pin 7): Serial Port Clock. When in local mode, SCK is an input. MOSI data is captured by the LTC4332 on the rising edge of SCK. MISO data from the LTC4332 is updated on the falling edge of SCK. When in remote mode SCK is an output providing the serial port clock to remote devices. After startup, the remote side SCK is driven low. The local side SCK contains a weak bus-hold circuit which holds the last driven value on the pin if undriven.

MOSI (Pin 8): Master Out Slave In. When in local mode, MOSI is the serial data input for each of the slave select pins. MOSI data is captured on the rising edge of SCK. When in remote mode, MOSI is the serial data output and can be connected to remote slave devices' SDI or MOSI pin. MOSI contains a weak bus-hold circuit which holds the last driven value on the pin if undriven.

MISO (Pin 9): Master In Slave Out. When in local mode, MISO is the serial data output for each of the slave select pins. MISO's output driver is disabled when $\overline{\text{SS1-3}}$ and $\overline{\text{SSC}}$ are high. A weak bus-hold circuit holds the last driven value to prevent the pin from floating.

When in remote mode, MISO is the serial data input and can be connected to a remote slave devices' SDO or MISO pin. In this mode, MISO is weakly pulled to V_L and can be unconnected if not used.

$\overline{\text{INT}}$ (Pin 10): Remote to Local Interrupt. $\overline{\text{INT}}$ is an open-drain output in local mode and an input in remote mode. Values set on the remote side $\overline{\text{INT}}$ propagate to the local side $\overline{\text{INT}}$ pin. In addition, $\overline{\text{INT}}$ is the level-sensitive active low interrupt signal for the LTC4332's control interface. Connect to an external pull-up to V_L on the local side. Do not allow $\overline{\text{INT}}$ to float on the remote side.

$\overline{\text{SS1}}$ (Pin 11): Remote Slave Select 1 (Active Low). When in local mode, $\overline{\text{SS1}}$ is an input. Set $\overline{\text{SS1}}$ low to initiate a remote SPI transfer using pins SCK, MOSI, and MISO. When in remote mode, $\overline{\text{SS1}}$ is an output and can be connected to a remote SPI device's slave or chip select input. $\overline{\text{SS1}}$ must be set high when the SPI bus is idle. $\overline{\text{SS1}}$ is weakly pulled to V_L and can be unconnected if not used.

PIN FUNCTIONS

$\overline{SS2}$ (Pin 12): Remote Slave Select 2 (Active Low). When in local mode, $\overline{SS2}$ is an input. Set $\overline{SS2}$ low to initiate a remote SPI transfer using pins SCK, MOSI, and MISO. When in remote mode, $\overline{SS2}$ is an output and can be connected to a remote SPI device's slave or chip select input. $\overline{SS2}$ must be set high when the SPI bus is idle. $\overline{SS2}$ is weakly pulled to V_L and can be unconnected if not used.

$\overline{SS3}$ (Pin 13): Remote Slave Select 3 (Active Low). When in local mode, $\overline{SS3}$ is an input. Set $\overline{SS3}$ low to initiate a remote SPI transfer using pins SCK, MOSI, and MISO. When in remote mode, $\overline{SS3}$ is an output and can be connected to a remote SPI device's slave or chip select input. $\overline{SS3}$ must be set high when the SPI bus is idle. $\overline{SS3}$ is weakly pulled to V_L and can be unconnected if not used.

SPEED1 (Pin 14): Link and Interface Timing Select 1. SPEED1 is a 3-State input and in conjunction with SPEED2 selects link baud rate and the remote SCK timing parameters. Set to high, low, or float as defined in Table 2.

SPEED2 (Pin 15): Link and Interface Timing Select 2. SPEED2 is a 3-State input and in conjunction with SPEED1 selects link baud rate and the remote SCK timing parameters. Set to high, low, or float as defined in Table 2.

GND (Pin 16, 21): Connect to GND.

Link (Referenced to GND and V_{CC})

Y (Pin 17): Non-inverting Link Driver Output. Connect to the A pin of a second LTC4332 device set to the opposite mode.

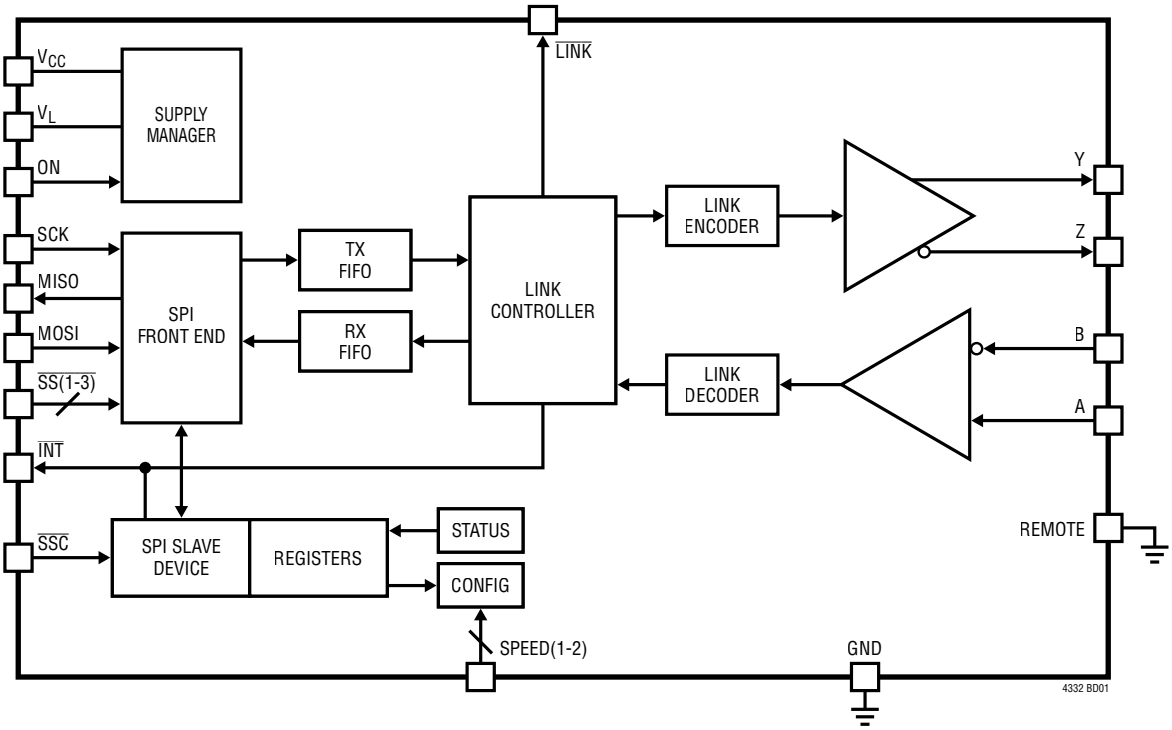
Z (Pin 18): Inverting Link Driver Output. Connect to the B pin of a second LTC4332 device set to the opposite mode.

B (Pin 19): Inverting Link Receiver Input. Connect to the Z pin of the second LTC4332 device set to the opposite mode.

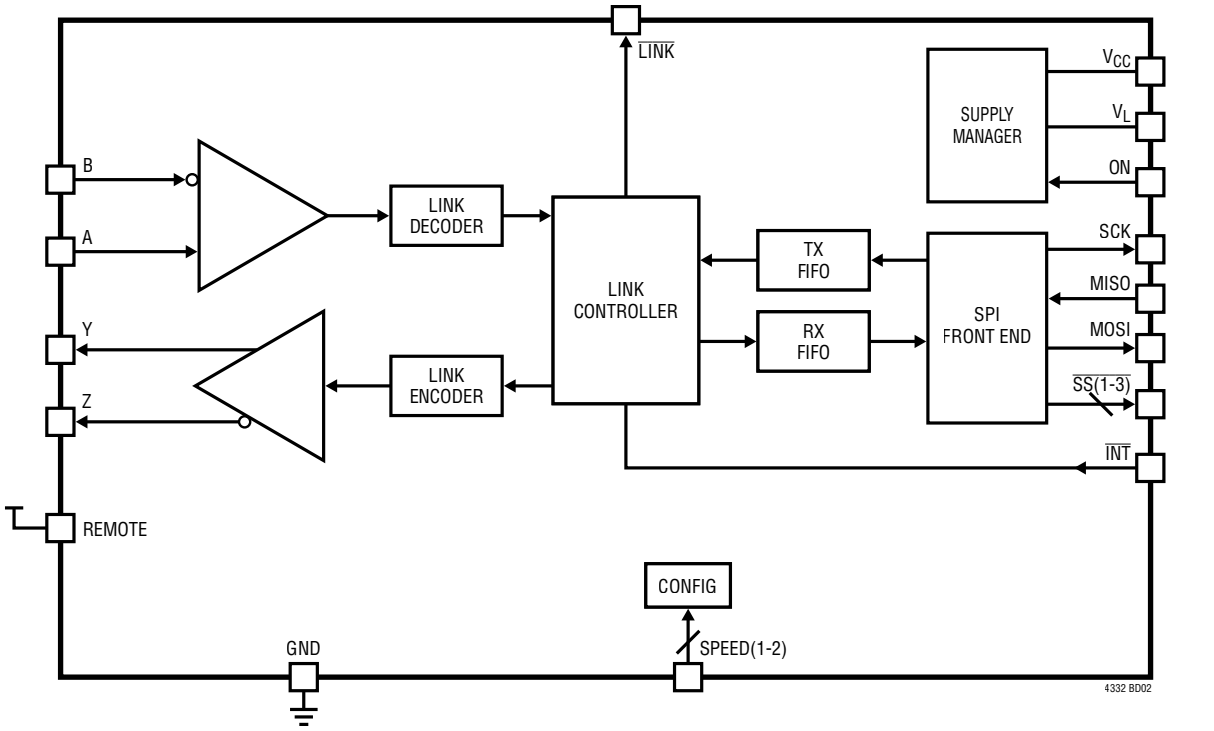
A (Pin 20): Non-inverting Link Receiver Input. Connect to the Y pin of the second LTC4332 device set to the opposite mode.

BLOCK DIAGRAM

Local Mode



Remote Mode



TEST CIRCUITS

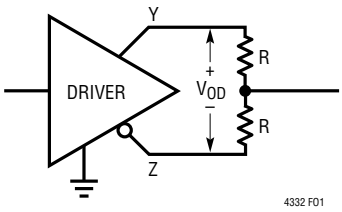


Figure 1. Driver DC Characteristics

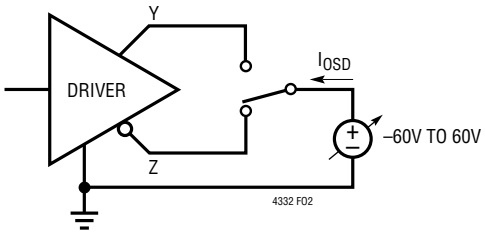


Figure 2. Driver Output Short-Circuit Current

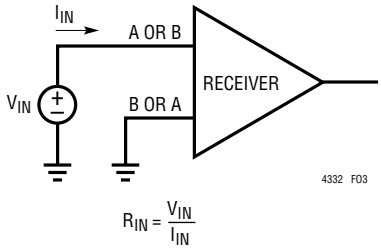


Figure 3. Receiver Input Current and Input Resistance

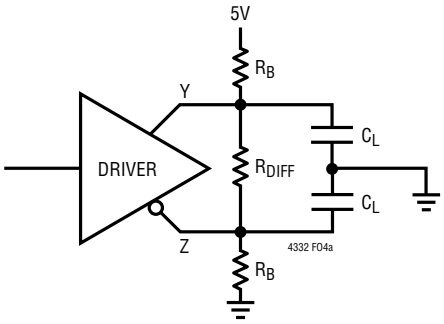


Figure 4. Driver Loading for I_{CC} Measurements

TIMING DIAGRAM

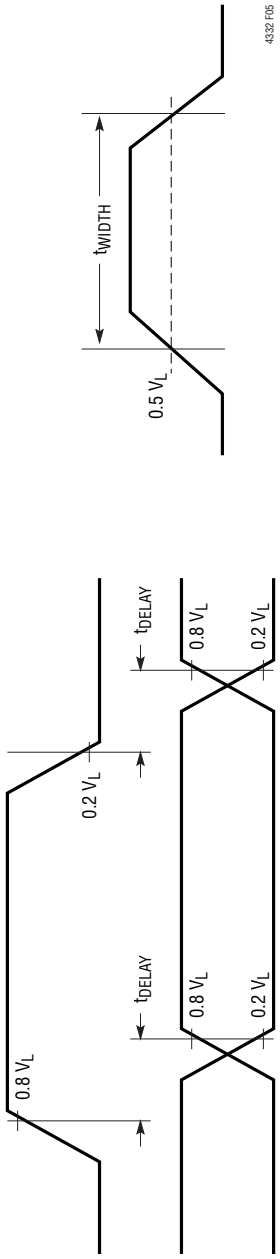


Figure 5. Logic I/O Voltage Levels for Timing Specifications

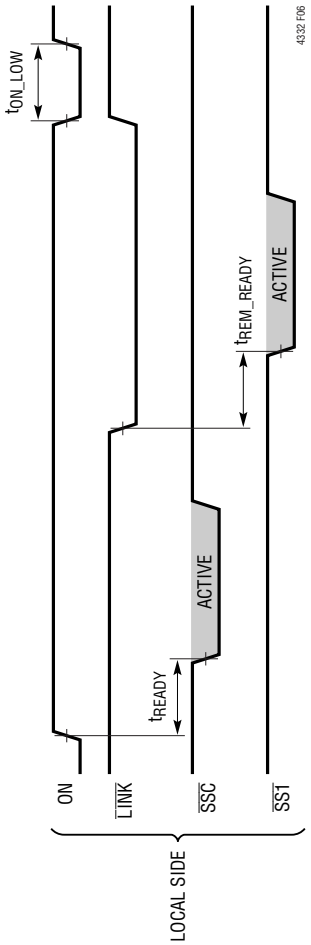


Figure 6. Startup

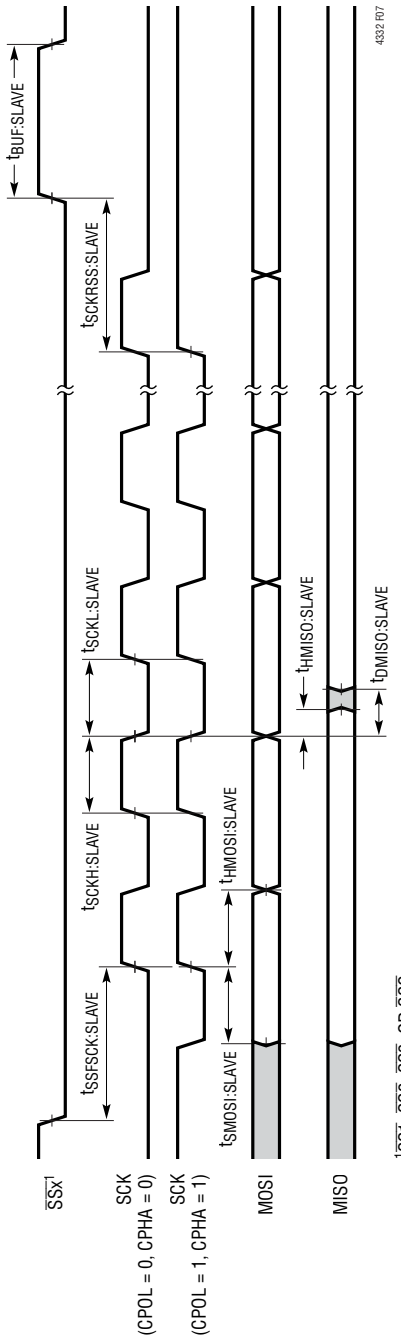


Figure 7. Local Side SPI Timing

TIMING DIAGRAM

Figure 8. Remote SCK Period

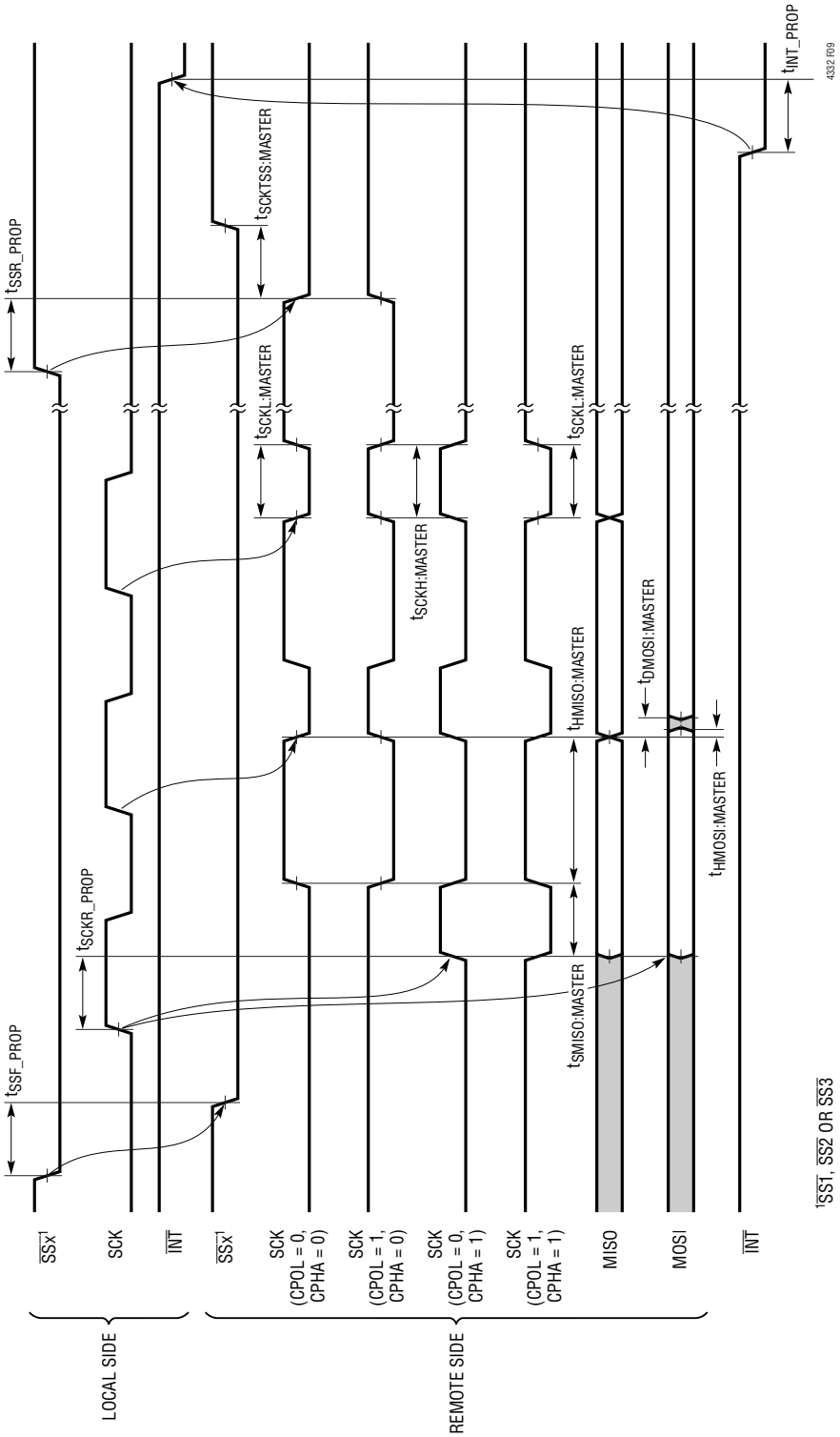


Figure 9. Remote Side Propagation and SPI Timing

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Overview

Two LTC4332 devices are required for a complete extended SPI network. On the local side, set the REMOTE pin low to set the SPI interface into slave device mode. A second LTC4332 with its REMOTE pin set high sets the SPI interface into master device mode. Three slave select pins are available to connect to slave devices on the remote side along with a shared interrupt signal.

The LTC4332 SPI extender solution supports remote slave devices with mixed SCK polarity and phase requirements. The remote side LTC4332 switches to the device's specific SPI interface mode before initiating a transfer.

Using an integrated high-performance differential transceiver for link communication, a local SPI master can access remote slave devices up to 1200m using inexpensive CAT5 or other differential-pair type cabling.

The LTC4332 SPI extender solution can be inserted into an existing SPI network with minimal impact. Write accesses to remote slave devices are software transparent; however, read accesses from remote slaves incur a one-word latency.

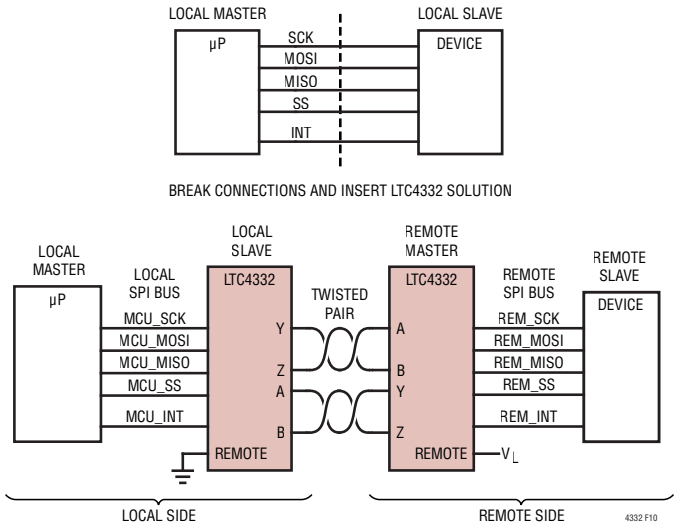

Figure 10. LTC4332 Solution Inserted Into a SPI Network

Local Mode

The LTC4332 is in slave SPI mode when the REMOTE pin is set low. Pins SCK and MOSI are inputs while pin MISO is an output. Once the link status output pin $\overline{LINK}$ is driven low, slave select pins $\overline{SS1}$, $\overline{SS2}$, $\overline{SS3}$ are available to access remote SPI slave devices. The device captures SPI data on the MOSI pin and sends it across the first differential link as an encoded bit-stream to the remote side LTC4332. Concurrently, the local side LTC4332 receives read-back data from the remote side through the second differential pair and stores it in an internal word FIFO. Read data is held in the internal word FIFO until the next word boundary is detected then is driven onto pin MISO. Therefore, MISO data is always delayed by one word. See Figure 12. An extra word appended to the existing transaction can be used to read out the last word. The word length defaults to 8 bits. Words lengths from 8 to 32 bits are supported by writing the WORD_LENGTH register in the control interface using $\overline{SSC}$. The internal FIFO is always flushed at the start of transaction.

The SPI protocol supports four unique timing configurations defined by the SCK polarity (CPOL) and clock phase (CPHA) summarized in Table 1.

Table 1. SPI Mode

CPOL	CPHA	SCK IDLE	DATA CAPTURED	DATA LAUNCHED
0	0	Low	Rising SCK	Falling SCK
0	1	Low	Falling SCK	Rising SCK
1	0	High	Falling SCK	Rising SCK
1	1	High	Rising SCK	Falling SCK

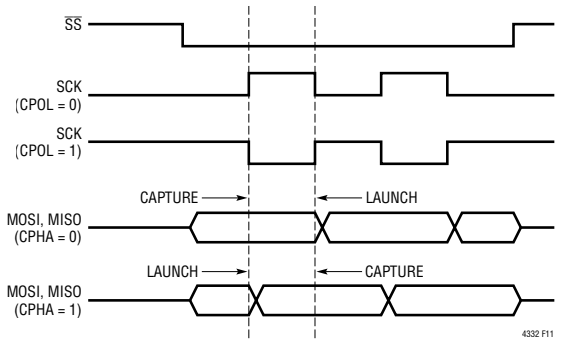

Figure 11. SPI Mode Waveform

When set to local mode, the LTC4332 SPI slave interface supports SPI modes (0,0) and (1,1) where (CPOL, CPHA). The maximum SCK frequency is limited by $f_{SCK:SLAVE}$ and Table 2 when accessing remote SPI slaves. The MISO pin is weakly held to the previously driven value when all slave select pins are high. MISO is only driven after a

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slave select pin is low and the first word is shifted by pin SCK. It is invalid to assert more than one slave select pin concurrently.

Remote Mode

The LTC4332 is in SPI master mode when the REMOTE pin is set high. Pins SCK and MOSI are outputs while pin MISO is an input. Three slave selects output pins $\overline{SS1}$, $\overline{SS2}$, $\overline{SS3}$ are available to connect to remote SPI slave devices. The remote side LTC4332 first asserts the appropriate slave select pin mirroring the event from the local side and then toggles pins SCK with MOSI data as write-data becomes available from the link. Using the same SCK edge, the LTC4332 captures data on the MISO pin from the remote slave device, encodes the data, and transmits the created bit-stream along the second differential pair to the local side.

The remote side SCK period reflects the local side SCK period offset by a jitter parameter $t_{SCKJ:MASTER}$. See Figure 8. Care must be taken to ensure that the maximum supported frequency of the remote device is not violated.

The SCK duty cycle is as follows. When the remote SPI mode is set to (0,0) or (1,1), the low time $t_{SCKL:MASTER}$ applies while SCK high time = $1/f_{SCK:SLAVE} - t_{SCKL:MASTER} + t_{SCKJ:MASTER}$. When the remote SPI mode is set to (0,1) or (1,0), the high time $t_{SCKH:MASTER}$ applies while the SCK low time = $1/f_{SCK:SLAVE} - t_{SCKH:MASTER} + t_{SCKJ:MASTER}$.

The remote SPI master device supports SPI modes (0,0), (0,1), (1,0), and (1,1) for each remote slave select. Each remote slave select SPI mode can be individually programmed by the user to match the SPI mode requirements of the remote slave device. The SPI mode is programmed by writing the CONFIG register in the control interface. SPI mode switching is handled automatically by the LTC4332. When the user asserts a remote slave select to start a transfer, the remote side LTC4332 configures its SPI interface mode to match the mode of the remote device before asserting the remote slave select signal.

Differential Link Pair

Internally, the LTC4332 utilizes a high performance transceiver to communicate over the link pair. The A, B, Y, and Z pins are fault protected to ±60V. In addition, the transceiver operates over an extended common mode range of ±25V making it suitable for noisy environments or systems with ground potential differences. Data is exchanged between the LTC4332 devices using a custom packet which has a selectable baud rate based on the configuration of the SPEED1 and SPEED2 pins. Selectable baud rates over the cable allow balancing performance with cable length specific to the application. Both sides of the link must be set to the same speed configuration to match the baud rates and allow communication. Each

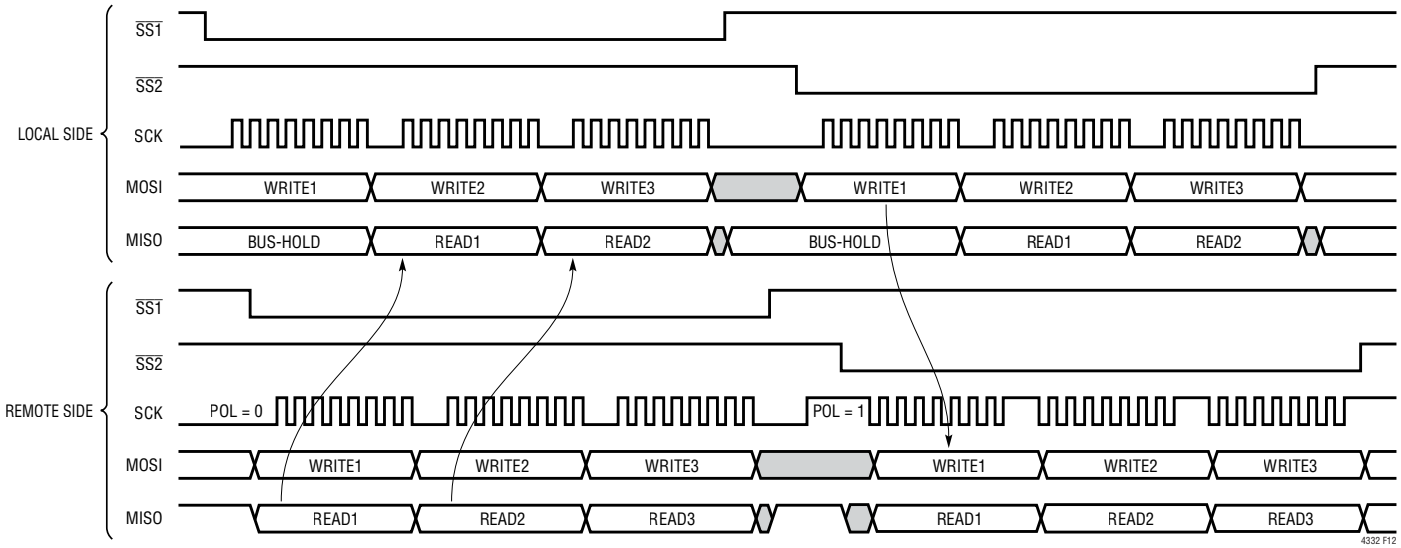

Figure 12. $\overline{SS1}$ and $\overline{SS2}$ Transfer. (REM_SS1_POL, REM_SS1_PHA) = (0,0). (REM_SS2_POL, REM_SS2_PHA) = (1,1). WORD_LENGTH = 8

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baud rate supports a maximum local SCK frequency listed in Table 2. Exceeding the listed maximum frequency results in data loss.

The LTC4332 SPI extension solution is point-to-point only. Multidrop or multipoint configurations on the differential link are not allowed.

±40kV HBM ESD Protection

The LTC4332 features exceptionally robust ESD protection. The link interface pins (A, B, Y, Z) feature protection to ±40kV HBM with respect to GND, V_{CC} (with a 4.7µF capacitor to GND), A, B, Y, or Z.

IEC ESD and EFT Protection

The improved ESD protection of the LTC4332 provides a high level of protection in the IEC ESD and EFT (Electrical Fast Transient) tests. The IEC ESD stress exceeds that of the HBM test in peak current, amplitude, and rise time, while the EFT test provides a prolonged repetitive stress.

Combined with the HBM test, the IEC tests help ensures that the LTC4332 is robust under a wide range of real world hazards. The LTC4332 passes the following tests on the A, B, Y, Z pins:

- IEC 61000-4-2 Edition 2.0 2008-12 ESD Level 3: ±6kV contact (A, B, Y, or Z to GND, direct discharge to bus pins with transceiver and protection circuit mounted on a test card with a low impedance ground discharge path from board GND to ESD gun return lead, per Figure 4 of the standard)
- IEC 61000-4-4 Second Edition 2004-07 EFT Level 4: ±4kV (line to GND, 5kHz repetition rate, 15ms burst duration, 60 second test duration, discharge coupled to bus pins through 100pF capacitor per paragraph 7.3.2 of the standard). V_{CC} pin requires 4.7µF to meet Level 4 rating.

Startup and Shutdown

Startup occurs when supply voltages are applied to pins V_{CC} and V_L and setting the ON pin high. All output pins are tri-stated during the first part of startup. After an internal initialization sequence the SPI interface and other pins are functional. The local side LTC4332 probes the differential link. After the startup time t_{READY}, a master can access the internal control interface using the $\overline{SSC}$ slave select pin. Once the device establishes link communication with a remote LTC4332, it drives pin $\overline{LINK}$ low and the remote SPI bus can be accessed (T_{REM_READY} > 0ns). See Figure 6.

The ON pin can be used to set the LTC4332 to a lower power state. By setting ON low, the LTC4332 is held in reset, all programmed configuration is set to the default value, all output drivers are disabled, and the differential transceiver is put into low power mode. If not used, tie ON to V_L.

Link Status

The LTC4332 provides the $\overline{LINK}$ pin which indicates when the remote SPI bus is ready. $\overline{LINK}$ is driven low when link communication is established. It is an open-drain output and requires an external pull-up to V_L if used. At startup, the $\overline{LINK}$ pin output driver is disabled.

Link status can also be monitored using the control interface. See section Control Interface. Ensure that the values set on local side SPEED1 and SPEED2 pins match the values set on remote side. Also, do not the exceed the cable length listed in Table 2. for the given SPEED setting. The LTC4332 will not link if these conditions are not met.

Note that the link status is indeterminate if the REMOTE pin is incorrectly configured on either the local or remote side LTC4332 device.

Interrupt

The LTC4332 supports an interrupt signal that is mirrored from the remote network to the local network using the differential link when the SPI Bus is idle. On the remote side $\overline{INT}$ is an input pin that can be connected to remote SPI devices. While on the local side $\overline{INT}$ operates as an open-drain output that can be connected to a shared local interrupt line. $\overline{INT}$ is periodically sampled and has a propagation time of t_{INT_PROP}. If enabled, the local LTC4332's control interface uses the $\overline{INT}$ pin to report link and fault events. The local side $\overline{INT}$ output is the logical AND of the remote $\overline{INT}$ and the internal endpoint interrupt signal. If

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an EVENT is triggered and its corresponding INT_EN bit is set high, $\overline{INT}$ is driven low. To clear the interrupt set the triggered event or the corresponding event enable bit to 0. Note that local $\overline{INT}$ could continue to be low due to a low value from a remote $\overline{INT}$ pin.

SPI Timeout

On the remote side, the LTC4332 acting as a SPI master resets the SPI bus if any slave select pin exceeds time $t_{TIMEOUT:MASTER}$. with the remote SCK inactive. This prevents the remote SPI bus from getting stuck active in the event of lost or corrupted link data during a trans fer.

Remote Reset

The local side LTC4332 can trigger a remote side LTC4332 reset by holding the ON pin low for a minimum of t_{REMOTE_RESET}. In addition, the remote LTC4332 is automatically reset after t_{REMOTE_RESET} if the link is disconnected. A remote reset disables all remote side outputs until link communication is reestablished.

Link Speed

The link baud rate is set using the SPEED1 and SPEED2 pins as shown in Table 2. The local SCK frequency cannot exceed the maximum SCK frequency for a given SPEED INDEX. The SPEED INDEX must be set to the same value on each side of the link.

Control Interface

The LTC4332 provides a separate slave select pin, $\overline{SSC}$, that allows a user to access the internal control interface for configuration and monitoring. The interface supports SPI modes (0,0) and (1,1) only. Read and write accesses are shown in Figure 13 and Figure 14. The bit order is MSB first. The first byte includes the register address in bits <7-1> and a read(1)/write(0) bit in the LSB. Only single data byte accesses per transfer are supported. Programmed values are retained while $V_{CC} \geq 3.0V$

An optional CRC byte can be appended to a write transfer. The CRC byte is calculated as a CRC-8 checksum over the first two bytes in the packet. The polynomial used is $x^8 + x^2 + x + 1$ initialized to zero. If the CRC byte is incomplete or incorrect, the LTC4332 will not commit the write transfer into the internal registers. Additionally, the fault bit SPI_WRITE_FAULT is asserted and local $\overline{INT}$ pin drives low if enabled.

The CRC byte is also available in a read transfer. In this case the CRC byte is calculated over the first byte written on the MOSI pin and the data byte read on the MISO pin.

Use of the CRC byte is recommended in high noise environments or high reliability systems.

Table 2. Link Speed

SPEED1 (NOTE 1)	SPEED2 (NOTE 1)	SPEED INDEX	SPEED FACTOR (NOTE 2)	MAX SCK FREQUENCY (kHz)	MAX CABLE LENGTH (m) (NOTE 3)
L	L	8	1×	2000	30
Float	L	7	2×	1000	60
H	L	6	4×	500	150
L	Float	5	8×	250	250
Float	Float	4	16×	125	500
L	H	3	24×	83	750
H	Float	2	32×	63	1000
Float	H	1	64×	31	1200
H	H	0	80×	25	1200+

Note 1. For assignments to Float, $0.5 \bullet V_L$ can also be applied to pin.

Note 2. Used for some switching parameter calculations.

Note 3. Evaluated with CAT5E Ethernet cable in a lab environment. Actual maximum cable length depends on type of cable and application environment.

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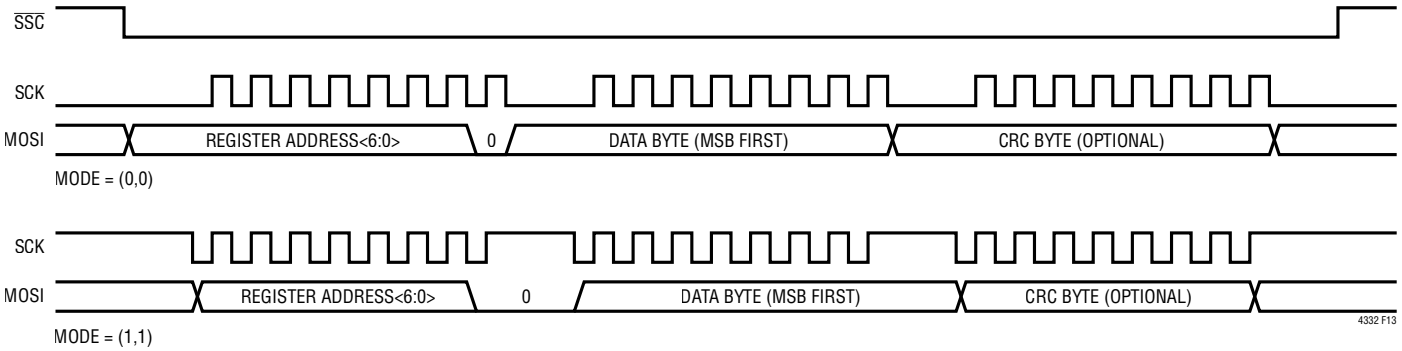

Figure 13. Control Interface Write Transfer

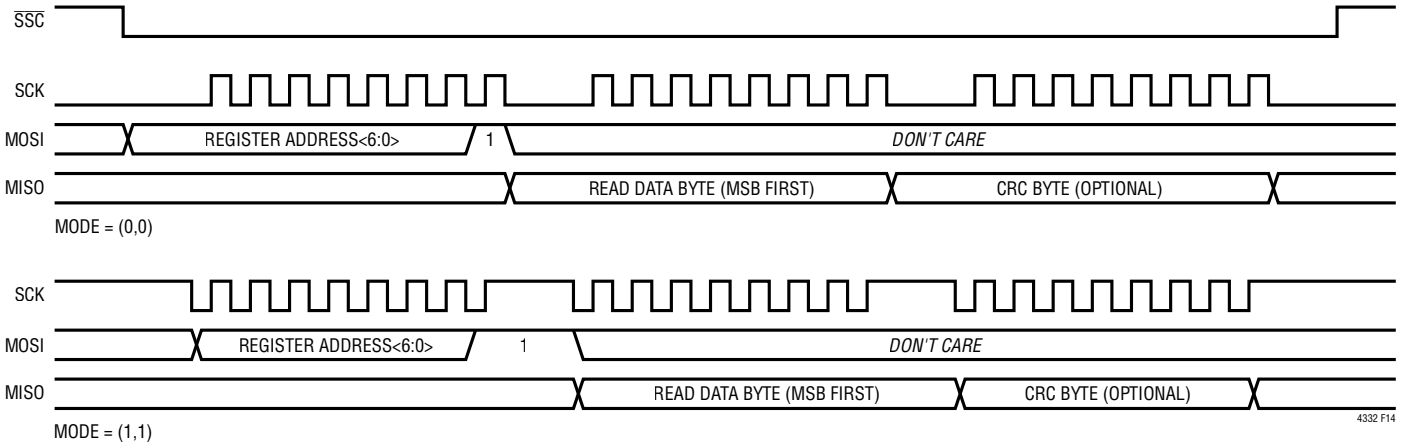

Figure 14. Control Interface Read Transfer

Register Naming Conventions

RW Read-Write

RO Read Only

W0C Write Zero to Clear

Table 3. Register Map

REGISTER	NAME	DATA								DEFAULT
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
00h	CONFIG	–	–	REM_SS3_ POL	REM_SS3_ PHA	REM_SS2_ POL	REM_SS2_ PHA	REM_SS1_ POL	REM_SS1_ PHA	0x00
01h	STATUS	SPEED_INDEX				Reserved	REM_NINT	NINT	NLINK	
02h	EVENT	–	–	–	–	–	FAULT	LINK_LOST	LINK_GOOD	0x00
03h	INT_EN	–	–	–	–	–	FAULT_EN	LINK_LOST_ EN	LINK_GOOD_ EN	0x00
04h	FAULT	–	–	–	RX_BUF_ UNDERFLOW	TX_BUF_ OVERFLOW	REM_SPI_ FAULT	LINK_FAULT	SPI_WRITE_ FAULT	0x00
05h	WORD_LENGTH	–	–	WORD_LENGTH						0x08
06h	SCRATCH	SCRATCH								0x00

Rev. 0

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CONFIG Register (RW)

FIELD	DESCRIPTION
REM_SS1_PHA	Remote Side $\overline{SS1}$ Phase. When 0, MOSI is launched on the trailing SCK edge while MISO is captured on the leading SCK edge. When 1, MISO is launched on the leading SCK edge while MISO is captured on the trailing SCK edge.
REM_SS1_POL	Remote Side $\overline{SS1}$ SCK Polarity. When 0, SCK is low when idle. When 1, SCK is high when idle.
REM_SS2_PHA	Remote Side $\overline{SS2}$ Phase.
REM_SS2_POL	Remote Side $\overline{SS2}$ SCK Polarity.
REM_SS3_PHA	Remote Side $\overline{SS3}$ Phase.
REM_SS3_POL	Remote Side $\overline{SS3}$ SCK Polarity.

STATUS (RO)

FIELD	DESCRIPTION
NLINK	The level driven by pin $\overline{LINK}$. High impedance is interpreted as 1.
NINT	The level driven by the local side pin $\overline{INT}$. High impedance is interpreted as 1.
REM_NINT	The level driven into the remote $\overline{INT}$ pin. Link must be established.
SPEED_INDEX	<0-8>. Encoded index from values set on SPEED1 and SPEED2. See Table 2. Link Speed.

EVENT (W0C): Events Are Set by the System and Cleared by the User

FIELD	DESCRIPTION
LINK_GOOD	The local and remote SPI networks are connected.
LINK_LOST	The local and remote SPI networks have lost link communication.
FAULT	Set if any field in the FAULT register is set by the system. Clearing this bit clears all bits in the FAULT register.

INT_EN (RW): Asserts $\overline{INT}$ if Corresponding EVENT Bit Is Set

FAULT (RO): If the FAULT EVENT Bit Is Set, at Least One of the Following Bits Is Set. To Clear, Clear the FAULT Event Bit

FIELD	DESCRIPTION
SPI_WRITE_FAULT	An incomplete write transfer after the register address byte or CRC error detected.
LINK_FAULT	Link communication corruption detected.
REM_SPI_FAULT	A fault or stuck bus timeout occurred on the remote SPI bus possibly due to link disconnection during transfer.
TX_BUF_OVERFLOW	The transmit buffer overflowed, SPI events lost. Indicates the local SPI frequency exceeds $f_{SCK:SLAVE:MAX}$. See Table 2.
RX_BUF_UNDERFLOW	The receive buffer overflowed, SPI events lost. Indicates the local SPI frequency exceeds $f_{SCK:SLAVE:MAX}$. See Table 2.

WORD_LENGTH (RW)

FIELD	DESCRIPTION
WORD_LENGTH	Valid Range: $8 \leq$ WORD_LENGTH ≤ 32. MISO read data from remote slave is delayed by WORD_LENGTH SCKs.

SCRATCH (RW)

FIELD	DESCRIPTION
SCRATCH	Used to test read/write access to the Control Interface.

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PCB Layout

A ground plane layout is recommended. A 4.7µF bypass capacitor should be placed no more than 7mm away from the V_{CC} pin. The PC board traces connected to signal pairs (Y, Z) and (A, B) should be symmetrical and as short as possible to maintain good differential signal integrity. Route the differential signals pairs (Y, Z) and (A, B) as an edge coupled microstrip with a differential impedance approximately matching the cable impedance.

Link Termination and Biasing

To minimize the transmission line reflections over the link, a termination resistor should be connected between pins A and B at each node. Each resistor's value should closely match the characteristic impedance of the differential cable to reduce reflections. A bias resistor network should also be inserted at each node to maintain the idle state when the drivers are disabled. For DC-coupled (non-isolated) link applications, select R_B and R_{T2} such that $200\Omega \le R_B \le 620\Omega$ and $100\Omega \le R_{T2} \le 110\Omega$. See Figure 15.

Auxiliary Protection for 5kV Surge, 5kV EFT, and 30kV IEC ESD

An interface transceiver used in an industrial setting may be exposed to extremely high levels of electrical overstress due to phenomena such as lightning surge, electrical fast transient (EFT) from switching high current inductive loads, and electrostatic discharge (ESD) from the discharge of electrically charged personnel or equipment. The LTC4332 is designed for high robustness against ESD and EFT, but the on-chip protection is not able to absorb the energy associated with the 61000-4-5 surge transients. Therefore, a properly designed external protection network is necessary to achieve a high level of surge protection, and can also extend the ESD and EFT performance of the LTC4332 to extremely high levels.

Refer to section Auxiliary Protection for IEC Surge, EFT and ESD on page 16 of Analog Devices LTC2864 data sheet for a detailed description and diagram of the external protection network.

The network provides the following protection:

- EC 61000-4-2 ESD Level 4: ±30kV contact, ±30kV air (line to GND, direct discharge to bus pins with transceiver and protection circuit mounted on a ground referenced test card per Figure 4 of the standard)
- IEC 61000-4-4 EFT Level 4: ±5kV (line to GND, 5kHz repetition rate, 15ms burst duration, 60 second test duration, discharge coupled to bus pins through 100pF capacitor per paragraph 7.3.2 of the standard)
- IEC 61000-4-5 Surge Level 4: ±5kV (line to GND, line to line, 8/20µs waveform, each line coupled to generator through 80Ω resistor per Figure 14 of the standard)

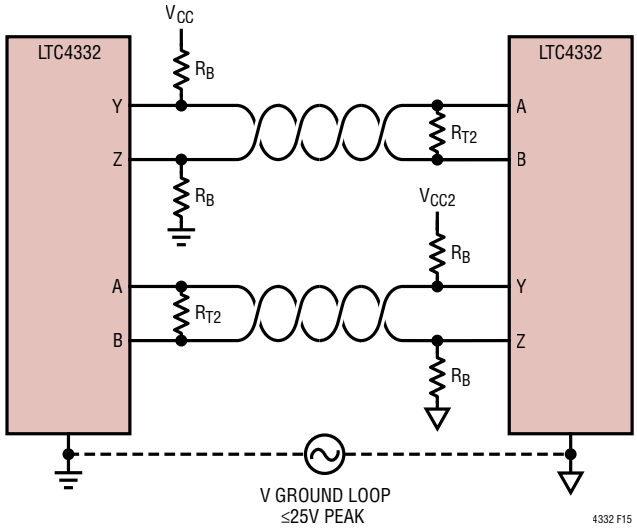
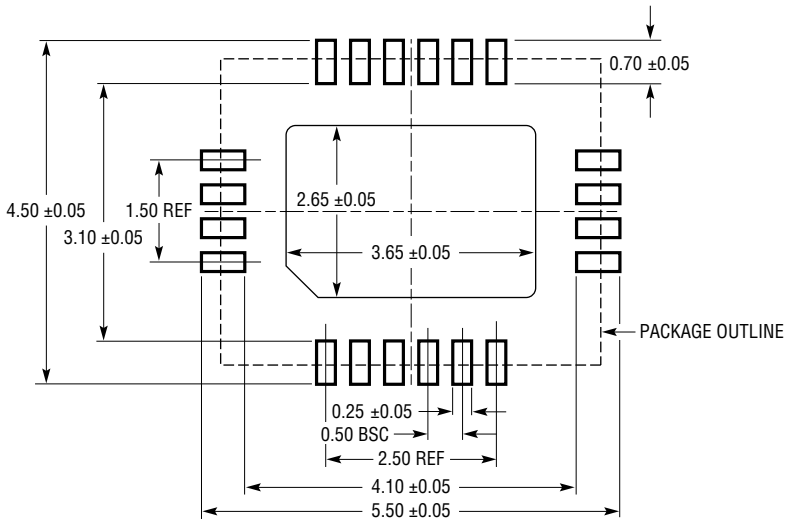


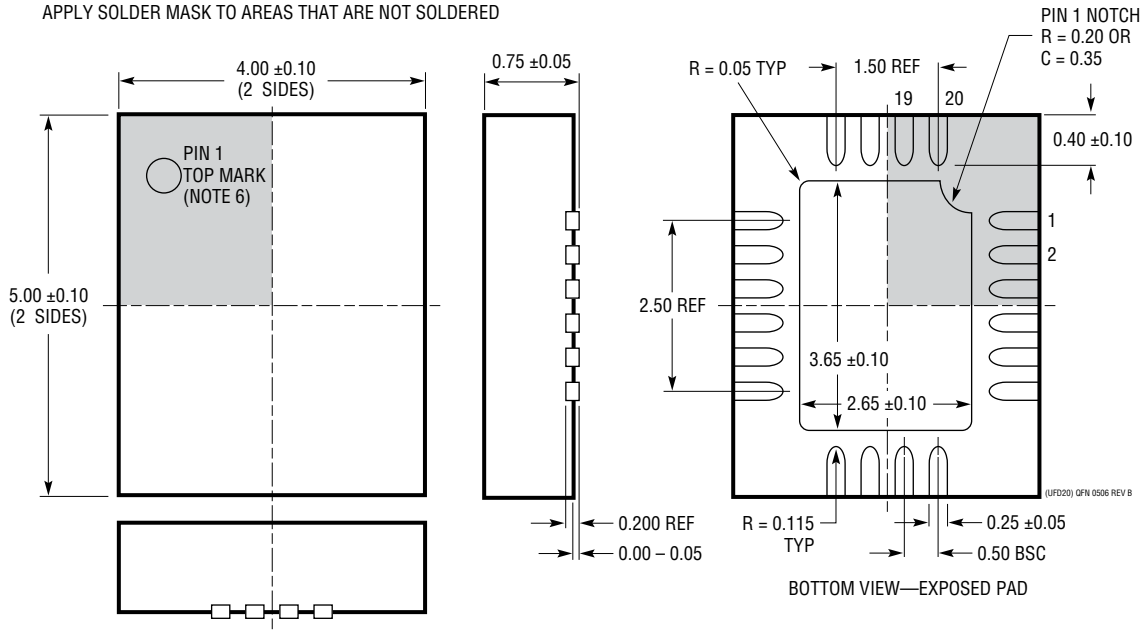
Figure 15. Resistor Bias Network

PACKAGE DESCRIPTION

UFD Package
20-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1711 Rev B)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WXXX-X).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

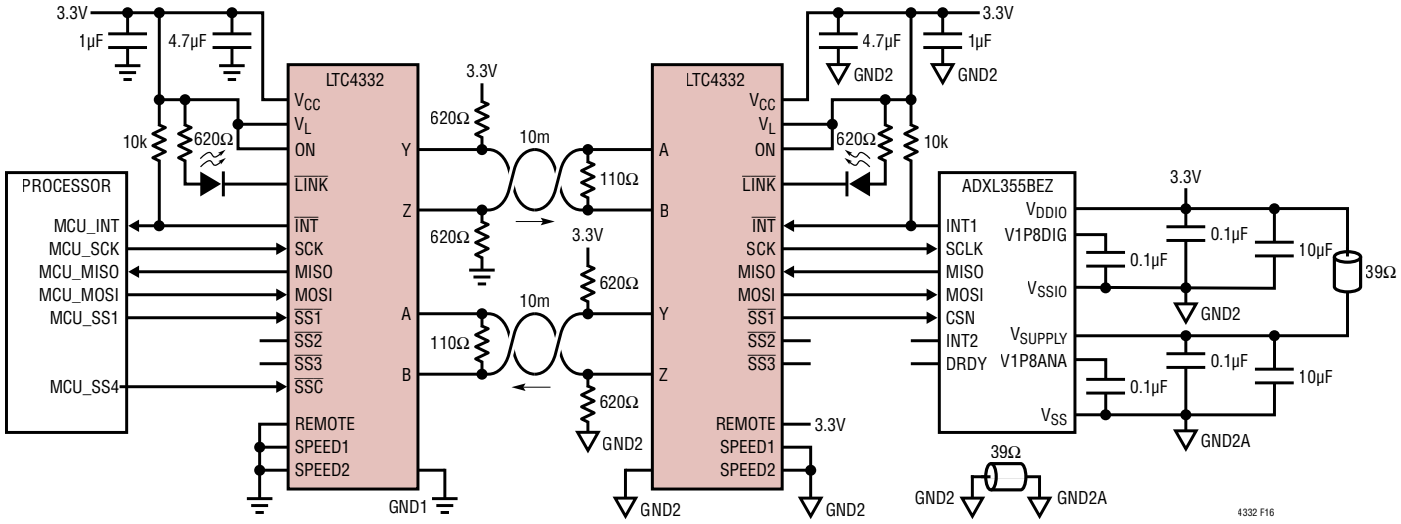


Figure 16. Extending an ADXL355BEZ Accelerometer for Remote Sensing

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC4331	I^2C/SMBus Differential Extender	1MHz SCL, ±60V Fault Protected
LTC6820	isoSPI Isolated Communications Interface	1Mbps, 100m Cable Lengths, ISO26262
LTM2895	100MHz Isolated DAC SPI Serial Interface	6kV Isolation, 2 Slaves
LTM2883	2.5kV SPI/I^2C Isolator with Power	4MHz/8MHz SPI Isolation, Adjustable DC Power
ADuM4154	5kV, 7-Channel, SPIsolator®	4 Slaves, 17MHz SPI clock